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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of March 2002.

Sincerely,

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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

The current funding allotment is running out (expenses plus liens exceed the allocation). It is not clear how long UC will allow this situation to continue. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We have negotiated a revised budget for the launch slip after a few iterations and some decreases in level of effort. We expect to submit this new budget officially soon.

1.2. *Significant System-Level Accomplishments*

- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals
- Participated in SWG meeting in Paris.
- Visited CESR, Kiel, and ESTEC with Project representatives. Addresses various technical and programmatic issues.
- Agreed on acceptable revision in PAIP wording for CESR. ESTEC to submit a revised PAIP appendix.
- Preliminary IMPACT/PLASTIC Command Format document submitted for review

1.3. *System Design Updates*

No significant changes.

1.4. *System Outstanding Issues*

- Project desires for maintenance of an "integrated IMPACT schedule" (which Project is currently building from the existing schedules) will require extra effort. We have provided a proposal to Project.

1.5. *Top 10 Risks*

Top 10 risks are attached. Some reordering of risks due to mitigation schemes, such as the backup L1 detectors. Risk UCB-10 (schedule) has percolated up onto the top-10 list due to other risks being mitigated.

IMPACT Top Ten Risks 4/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (still use VLSI in HET, LET)	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical team member could delay delivery	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Backup L1 dtectors ordered; low risk, meet requirements	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	A milestone schedule of deliveries has been set up to minimize schedule interaction and give power to control schedule to institutions while maintaining top level schedule slack; an integrated Project-level schedule is in progress. It is not clear yet if this will actually reduce risk	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status and a reworked boom schedule will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Efforts to reduce STE noise level proceeding at LBNL
- SWEA/STE schematics ready for layout, pending finalization of mechanical details.
- SWEA/STE mechanical design near completion.
- SWEA/STE FPGA specification complete; design work has started.

IDPU:

- Data Controller Board design complete and into layout.
- Data Controller Board FPGA in work.
- Flight Software: 1553 Interface Driver and FLTC decoding software written

LVPS/HVPS:

- LVPS breadboard in test.

Boom:

- Thermal model proceeding (with Eby).
- Prototype / Flight tube specifications complete, ready to put out to bid

GSE:

- IDPU Simulator complete. Instrument-specific work started (MAG first).
- Starting on work for C&T GSE (Command encoder, MOC Interface).

2.3. *Design Updates*

None

2.4. *Outstanding Problems*

- Operational heater power budget over allocation

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for March, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The L1 detector mounts underwent mechanical inspection. While the mounts did not strictly meet this inspection, the detector manufacturer (Micron) examined a sample mount and approved it for use. The HET H1 detector mount design is now 90% complete and the HET H3 mount is 60% complete. The L2 and L3 mounts are not started as of yet.

A preliminary design of the SIT electronics mechanical configuration has been completed. Preliminary outline drawings of the SIT boards show keep-out areas for mechanical mounting and SIT connector locations. A preliminary design of the SIT High Voltage Power Supply box was completed as part of this work.

Since many of the SIT telescope parts are heritage parts, we are starting to submit drawings for fabrication. Six mechanical pieces for SIT were sent out for fabrication. Some of these parts have been received and are ready to go for mechanical inspection.

A preliminary mechanical layout for the SEP Low Voltage Power Supply has been completed.

We are proceeding on the assumption that the UCB Low Voltage Power Supply will provide separate low voltage windings for SEPT.

3.2. *Major Accomplishments*

Continued work on defining HET GSE software and hardware requirements. The HET GSE is being designed such that the GSE can be at Goddard and operate HET via TCP/IP sockets wherever HET is located (Goddard, Caltech, or APL). We are in the process of integrating our ideas on this with our Caltech and UofMD colleagues. Security is an important issue, so we will be proposing a command encryption scheme.

Resolving Contamination Control issue re surface cleanliness at delivery is being deferred until Therese Erigo writes a preliminary Contamination Control Plan for IMPACT.

3.2.1. Next month

- Complete H1 and H3 detector mount designs. Begin work on the L2 and L3 designs.
- Visit Caltech to discuss various outstanding electronic and mechanical design issues.
- Continue work on the HET GSE, on-board software, and PHA ASIC test software.
- Develop preliminary front-end electronics design for SIT.

3.3. *Design Updates*

None identified this month.

3.4. *Outstanding Problems*

Contamination Control: We have previously stated our plan to deliver our instruments with the exterior surfaces cleaned to level 500 B. This is in conflict with the requirement presented by APL calling for level 300 A. This still needs to be resolved. The plan is to do this while Therese Erigo is developing the IMPACT Contamination Control Plan.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
March 2002

4.1. *Summary of Status*

1. SEPT Telescope – Incoming inspection of prototype detector stack completed, including preliminary stray light analysis. Result: energy resolution OK, leakage current OK, UV light sensitivity marginal. Hosting UCB and NASA/GSFC visitors (Dave Curtis, Don Carson, Harry Culver, Lisa Bartusek).
2. Sensor and E-Box Housing – Change of cables between sensor and E-Box from coax to triax including connector types resulting in significant weight increase: from 560 g to 640 g per SEPT and in significant cost increase for connectors.
3. SEPT Electronics – New SEPT-FPGA prototype development started at contractor with completion date end of May 2002. Significant progress in assembly of electronics boards, in software development and testing of electronics at ESTEC and at contractor site. Will be ready for first integration of detector system and associated electronics, now scheduled for mid May 2002.
4. Schedule -- A SEPT schedule is detailed for ETU and Flight units, no percent completion is given for the breadboard activities currently under way.

4.2. *Major Accomplishments*

1. First SEPT solid-state detector stack passed incoming inspection. The energy resolution is 7 keV FWHM for electrons (^{207}Bi, 481.7 keV line) and 40 keV for alphas (^{241}Am, 5.485 MeV line). The poor alpha resolution is expected, as the particles are incident from the Ohmic side. The sensitivity to UV light is acceptable, but the error margin is large both when determining the black light intensity from the UV-lamp and the photon intensity from scattered Sun light. Either better estimates with smaller error bars are achievable or a solar simulation test will be needed. Work towards a decision is in progress.
2. Switch from coax (cable type RG-178, connector type SSMC, manufacturer ITT Cannon) to triax (cable type Mil-C-17/131 RG-403, connector type NDL-T, manufacturer Sabritec). Rationale: EMI problems are expected when exposing coax connector body on analogue ground to open space. Sensor will have pigtails with right angle plugs (male), E-box will have pigtails with straight bulkhead jacks (female). The penalty is increased weight and increased costs: SSMC weight male/female: 3 g / 3 g, NDL-T weight male/female: 6 g / 3.5 g. There are 2*13 mating pairs per S/C, hence the weight delta is 26*3.5 g = 91 g for the connectors plus a few grams for the difference between RG-178 cable and RG-403 cable. Internal weight saving efforts reduce the final weight delta to 80 g per SEPT, 160 g per S/C.
3. A SEPT-FPGA Design Consultancy Service has been kicked off between a contractor (Gaissler Research) and ESTEC. Baseline modifications are: Baud rate fixed to 57600 bits/s for input and output, system clock changed to 18 MHz (core operates on 4.5 MHz), calibration pulse generation done with 18 MHz clock without clock gating, i.e. same specification as earlier, but with more precise implementation, the two binning tables are merged to one (i.e. no difference between electron and proton binning

thresholds), the pin-out between current FPGA version (000) and the new version (001) should be compatible, except for the some changes listed.

4.3. *Design Updates*

Replacement of 13 coax connectors by 13 triax connectors. A new revision of the SEPT Mechanical Interface Control Drawing is completed and distributed to Dave and Sandy.

4.4. *Outstanding Problems*

4.5. *New Problems*

Inconsistency of Kiel schedule and ESTEC schedule was detected. Will need to be resolved after completing the first integration of detector system and associated electronics, now scheduled for mid May 2002.

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

March 2002

5.1. *Summary of Status*

Activities centered on electronics development, detector development, and GSE software.

Major Accomplishments

Electronics:

- (This item inadvertently omitted from February status report.) Completed layout and all LVS and DRC checks on PHA chip. Completed digital simulations and checks. Verified analog design margins by "SPICE" simulations down to -100 C using wide-temp range spice models derived earlier in collaboration with MOSIS. Entire analog pulse processing chain found to function properly at -100 C. (Laboratory testing of prototype showed proper function from room temp up to limit of test at 50 C.) Submitted design to AMI for further DRC check and fab.
- The PHA chip was submitted to AMI at the end of February and several DRC passes were performed in early March, with final approval given for mask release in mid-March. Fabrication is proceeding ahead of schedule at AMI, with wafers expected during second week of April.
- Started preparations for layout of ASIC hybrid's ceramic substrate and realized that design guidelines were more conservative than previously thought. Search for a bigger package was successful, which allowed addition of filter networks in the package with fewer pins. This approach will help simplify front-end PCB layout, but will likely increase board's overall mass due to the fact that the new package material is kovar rather than ceramic.
- Proposed using Nanonics connectors on SEP LVPS (internal connections) and sent a sample to Peter Berg for evaluation.
- Decided to use R/2R approach for HK ADC rather than AD7664.
- Drafted SEP grounding diagram for discussion among team members.

GSE:

- Began defining the network interface between the SEP GSE and the HET and SIT GSEs being developed at GSFC.

Detectors:

- The first attempt to etch a silicon wafer that had front-side patterning for the LET L1 design was unsuccessful because the thick wafer cracked. This is attributed to mechanical stresses applied in clamping the wafer into a newly-made etching holder. Otherwise the etching went well. Etching of the second wafer is being attempted using a different holder in which some previous test etches had been done without problems.
- A prototype L1 detector mount (designed at GSFC) of the type planned for flight was sent to Micron for their inspection. They have approved the design.
- Micron reports that prototypes of the other LET and HET detectors (H1, H3, and L3, all of which are 1 mm thick and L2 which is 50 microns thick) are nearing completion.

- A meeting with Colin Wilburn, Micron's managing director, has been arranged for April 22 at Caltech. The status and schedule of the HET and LET silicon detector development will be reviewed at that time.

5.2. *Design Updates*

- No changes to mass and power estimates.

5.3. *Outstanding Problems*

None.

5.4. *New Problems*

None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See September report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary. Also, initial chip fabrication happened much faster than anticipated which is helpful if another run is needed.

5.6. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

March 2002

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.

b. SIT TOF System - Flight modifications to Prototype electronics design and layout are underway. There are still some issues on mechanical layout that need to be resolved.

c. SIT Energy/Logic System - Energy system redesigned with Amptek parts. Preliminary design and prototype layout completed. PC Board received. Working on logic design changes to accommodate new system and associated GSE. Waiting for technician to assemble board.

d. SIT HVPS - HVPS box drawing (exterior details only) generated by GSFC.

6.1.1. Schedule Changes

None. We are essentially on schedule (within 1 week) according to the schedule issued 1/22/02 and updated with latest progress 4/9/02.

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

- TOF - Sandy Shuman of GSFC generated the outline drawings for the two TOF boards.

- Energy - The prototype PC board for the energy Amptek design was received as well as the Amptek parts needed for the prototype system. The logic for operating the energy system was designed and the implementation in Xilinx was begun.

6.2.2. Next Month

- We will assemble the prototype energy system and begin testing next month.

- We will generate an update of the front-end logic requirements document including the new energy design.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 7
(April 15, 2002)

March 2002

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

- Mechanical design end 17/12/2001: completed
- Mechanical analyzer fabrication end 22/04/2002
  Quite finished for the ETU (95 % done)
- Electronics fabrication end mid April: started (50 % done)
- ETU Assembly start 06/05/2002 end 05/07/2002
- Delivery to UCB 12/07/2002

7.2. *Major accomplishments*

- Mechanical fabrication :
  - First EM analyzer and housing fabricated, small modification done on the rails attached to the grids to avoid any cable to be in space view.
  - Dummy piece to replace the pin puller done.
  - Deflector grids fabrication on the way, some difficulties found but solved. To be ready around April 25.
  - Spheres treatment and black coating will start.
  - Integration will start mid May.
  - Verification under vacuum end of May.

- Deflectors grids fabrication on the way.

- Electronics boards are designed. Resistors added on the MCP board for heating purpose. Fabrication of the 3 electronics boards on the way.
- First printed circuit board received. Should be populated and tested by the end of April.

- Pin Puller ordered.

7.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

- To be in compliance with the EMC and electromagnetic cleanliness, we are studying how to add crystal control on HV. This will be done on the ETU as well. A 100 kHz square signal will be sent to the HV from the LVPC done by Berkeley.
- AMPTEKS amplifiers quality. It will difficult for us to have the best quality for them as done for Goddard

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

1. The MAG analog front end breadboard was completed and tested over six months ago. Conversion to surface mount devices has also been completed with good results. Parts selection continues, including screening strategy, fixtures, etc. Testing of miniature coaxial cables was completed more than nine months ago.

2. The MAG-DPU digital interface design has been completed and an engineering (functional only) model is being built. Interface tests are planned for early this summer.

3. Magnetic cleanliness seminars are conducted periodically (every couple of months) at APL to address spacecraft and instrument magnetic issues. The SEPT magnet assemblies will be tested at GSFC on April 15th. to validate the analytical model and its predictions.

9. EPO at UCB

March E/PO Report:

Formal Education:

A student activity about building IMPACT booms (where they build a paper model of the boom to see how it is constructed and how it will deploy) is being planned. Students will construct a model BOOM using strips of paper and tape. The objective will be to build the longest boom possible which is still fairly rigid. Rigidity is an actual requirement for the SECCHI imager on the IMPACT BOOM. How rigidity will be tested needs to be explored in the development of this activity. Perhaps they could clip a binder clip to the end of their BOOM and see if the BOOM buckles.
A fifth grade teacher is recruited for classroom level developing and testing and there are plans to meet with the STEREO Sr. Engineer at SSL and follow him in his plans of development and take pictures of the BOOM.

Informal Education:
March 20- Sun Earth Day-: EPO Lead N. Craig visited 3 classes at Vannoy Elementary School in Castro Valley, CA. Major topic was the SUN-Earth connection and STEREO Mission was also brought up as an upcoming Solar mission; Posters and Glasses are distributed.
March 28 - UC Berkeley Science Coalition Meeting: 30 Posters/Glasses were distributed.
April 5th -The Science and Technology Evening: 50 STEREO Posters/Glasses are sent to Freedom High School's Math, Engineering, and Science Academy at Oakley, CA.

Please check the STEREO/ECLIPSE Website that was coordinated and developed by the UCB and Exploratorium during summer 2001, including the video interviews of scientist.
http://www.exploratorium.edu/eclipse/zambia/stereo/index.html

Respectfully submitted,

Nahide Craig