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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of September 2001.

Sincerely,

David Curtis
IMPACT Project Manager
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

The UCB Phase BCDE contract has been signed in late August. Subcontracts to Caltech and University of Maryland are in work (they are currently working on a no-cost extension of the Phase A/Bridge phase contract).

UCB has received a first funding allocation under this new contract. This amount is expected to last through October. It includes a significant amount for the procurement of long-lead parts. As setting up those procurements takes some time, the funding will probably last into November. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We expect a contract mod from Project shortly to modify the launch date. We are working on a corresponding revised budget and schedule.

1.2. *Major System-Level Accomplishments*

- The IMPACT PDR was completed in September. Work has started on responding to action items.
- A number of documents were submitted in the past few months leading up to the PDR, such as a Software Development Plan, Environmental Test Plan, and Configuration Management Plan.
- Work on the spacecraft ICD continues.
- Working on a number of design trades to improve reliability.
- A new draft of the IMPACT intra-instrument harness spec has been released.

1.3. *System Design Updates*

Mass and power spreadsheet update submitted separately (and provided to APL). Some change in harness mass due to new length estimates from APL.

1.4. *System Outstanding Issues*

- Waiting on Project input on IT Security requirements
- IMPACT PAIP needs to be negotiated. IMPACT is generating a response to the latest round of comments. There seems to be a trend towards requiring closer adherence to the IMAR in the latest round of comments, rather than allowing in-house practices to be used. Also the parts screening requirements are increasing. This will have cost implications.
- While Project screening requirements are increasing, screening cost quotes are also increasing drastically. Impact on cost could be several hundred thousand dollars.
- Some changes to the IMPACT configuration to improve reliability have been proposed (e.g. the separate spacecraft interface to SEP). Any changes need to be made ASAP to avoid a schedule impact.

- The current design of low voltage power distribution violates the EMC requirements (due to the break-up of STE and SEP). We are working on estimating the resource costs required to fix the system to be compliant, and at the same time, investigating if a waiver would be possible. This change goes beyond just adding extra windings to the LVPS – it affects the power distribution inside the SEP Central box, and the harness from SEP Central to the SEPT units.

1.5. *Top 10 Risks*

A copy of the top 10 risks slide for PDR is attached. Note that this list is in no particular order. The project risk management database has not been updated recently because it is currently inaccessible.

IMPACT Top Ten Risks as of PDR, 9/2001

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_2	Increasing documentation requirements distract key personnel from design tasks	MEDIUM	Negotiate documentation requirements to minimize impact	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	A milestone schedule of deliveries has been set up to minimize schedule interaction and give power to control schedule to institutions while maintaining top level schedule slack	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_16	STE Detectors are a new technology	MEDIUM	Early testing to prove design	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Working with manufacturer on process	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Work at Berkeley has slipped somewhat behind the July schedule in some areas. Delays are due primarily to continuing delays in the HESSI launch and the corresponding unavailability of personnel to work on IMPACT, and some delays in getting working STE ETU detectors from LBNL. This has resulted in under-spending at UCB. At this time IMPACT is adequately staffed, though we still share some personnel with HESSI (which gets top priority on their time). Also the LBNL STE ETU detectors have recently been delivered. None of these delays have impacted any of the top-level IMPACT schedule milestones (as presented at PDR), though it has reduced some of the slack leading up to the ETU interface tests. An updated schedule is in-work.

2.2. *Major Accomplishments*

SWEA/STE:

- The STE detectors have been mounted and connected to a breadboard preamp.
- STE detector/preamp performance tests are in progress. The detector performance appears to meet the STE goals. The preamp noise meets the requirements, but there is room for improvement. Various FETs have been tested (this is the source of the majority of the noise). More work on preamp noise next month.
- A breadboard of the SWEA/STE interface is partially built; testing to be started next month.
- STE cover actuator design has started.

IDPU:

- The serial interface specification has been updated to add a parity bit to the command
- IDPU ICD drawing has been updated. Shop drawings of the trays and circuit board form factors to start next month.

LVPS/HVPS:

- A breadboard of the latest LVPS configuration is being constructed; tests expected next month. Three non-standard parts will start screening as soon as tests verify operation.
- SWEA LVPS form factor to be determined next month so decision can be made on geometry of the UCB part of SWEA.
- SIT HVPS connector selection is an issue. A candidate (recommended by Batel) is under consideration (problem is physical size).

Boom:

- Thermal model proceeding (with Eby). Issues are minimizing SWEA operational & survival heater requirements and providing a boom model to APL for the spacecraft model.
- Working the finite element model issues with APL. Need to provide a joint stiffness K factor next month (based on measurement of existing prototype joint).

- Looking at possibility of meeting Mario's desire to get the MAG into sunlight to minimize MAG heater requirements. To generate a candidate ICD drawing change to APL/Mario next month.
- Working on piece-part drawings for ETU (2 or 3 segment) boom planned for completion by Spacecraft PDR.

GSE:

- The subcontract to develop the IDPU Simulator GSE hardware has been let and work is progressing. The circuit is designed, and the board will go to layout next month. The FPGA design should complete next month. First delivery to UCB is expected in November.
- The interface driver for the host PC is in work at UCB.

2.3. *Design Updates*

No changes.

2.4. *Outstanding Problems*

- SWEA operational heater estimate needs refining based on a better thermal model. Possible significant increase in heater power requirement.

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for September, 2001 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

Summary of Status - Summarize the current contract and schedule status. Identify any anticipated changes in schedule milestones

Mostly on-schedule. VLSI design document is incomplete, holding back analog front-end design for HET and SIT.

Major Accomplishments - Summarize achieved accomplishments versus planned accomplishments for the previous month and delineate planned accomplishments for the next month.

Participated in IMPACT/SEP PDR.

Developed VERILOG version of MISC including UARTs, interrupts, and boot-up code. Worked on rate compression algorithm.

Next Month-

Reply to PDR action items.

Develop debug monitor code for MISC. Verify MISC design.

Study SIT front-end logic specification (due from UofMD Oct 15).

Complete ICD interface drawings for SEP.

Complete L1 mount design and deliver mounts to Micron by Nov 1 (tight)

Complete initial SEP thermal design.

Release schedule.

Design Updates Summarizing changes in resource requirements (mass, power and telemetry) and any major instruments specifications.

Currently none.

Outstanding Problems - State progress toward solving major problems previously identified; state whether action is required.

No major problems. Late involvement of analog engineer due to not having the necessary VLSI specifications could be a problem.

New Problems - Discuss major problems that have been identified during the past month; state whether action is required. Identify potential work around positions if the problems will have a significant impact on the on-time completion of the contract or on critical scheduled milestones

Top Risks Identify the ten risks items for the IMPACT project. A mitigation plan and schedule shall be identified for each risk item.

No significant risks at GSFC?
Problem/Failure Quick Look Provide a list of all open problem/failure reports and those problem/failure reports closed during the month. At a minimum, the list shall include an ID number for the problem, a description,

an assignee, and the open/closed dates. This section of the technical report shall begin with the first application of power to the proto-flight and/or flight model for an electrical component (subsystem) or the first mechanical motion for a mechanical component (subsystem).

4. Kiel (SEPT) Status

IMPACT - SEPT Progress Report

Date:	08-Oct-01
Period covered:	September 2001
Activity covered:	SEPT instrument development
Institution:	University of Kiel, ESTEC
Compiled by:	R. Mueller-Mellin, P. Falkner

4.1. *Summary of Status*

Contract status:

N/A

Schedule status:

Detector delivery	12-NOV-01, staggered delivery
Magnet delivery	29-OCT-01
Foil delivery	open
Mechanical design freeze	01-JUN-02
Electronics design freeze	01-JUN-02
Cable delivery	15-OCT-01
Pinpuller delivery	open
PDFE ASIC delivery	new redesign in 15-MAY-01
FPGA delivery	first programmed prototype is delivered to ESTEC 01-OCT-01
GSE	
Hardware Assembly	open , (3 PC's are set-up, plug-in cards are inhouse)
Programming	open
Mathematical Modelling	
Mechanical	01-MAR-02
Thermal	01-MAR-02
Engineering Model (EM)	
Sensor Assembly	01-OCT-02
Electronics Assembly	01-OCT-02
SEPT Integration & Test	15-NOV-02
SEPT Acoustics	15-JAN-03
Flight Models FM1, FM2	
Sensor Assembly	01-FEB-03
Electronics Assembly	01-FEB-03
SEPT Integration & Test	15-JUN-03
SEPT Vibration	01-AUG-03
SEPT TV/TB	10-AUG-03
SEPT delivery to Caltech	10-SEP-03
SEP Integration & Test	02-OCT-03
SEPT Calibration	16-APR-04
SEP delivery to UCB	10-SEP-04
IMPACT delivery to S/C	01-OCT-04

Note: this is a first cut on the schedule. Most dates are best estimates. Dates given are starting dates. Open dates will be specially marked if on critical path.

4.2. *Major Accomplishments*

1. The SEPT mechanical configuration has been redesigned to reflect
   - the new board size causing the outer diameter of the E-Box to shrink from 70x80 mm^2 to 69x77 mm^2
   - the rotation by 90° of the E-Box w.r.t. the sensor
   - the addition of a sensor thermistor with coax cable connection to the E-Box
   - the new location for 12 detector connections at two side walls instead of top wall of the E-Box
   - the addition of a grounding stud
   - the new mount released recently by the project office for thermal insulation
   - the cover release mechanism (was not yet included in sufficient detail in old design)
   - the new pinpuller dimensions of Model P5-403-10S which replaces P5-403-10.

2. The far field of the SEPT magnet system at the location of the MAG sensor has been modelled using an analytical calculation (point charge model). The magnet system was assumed to consist of two perfectly matched dipoles.

3. A manufacturer for the triax cable has been identified, the cable is ordered. This was a major concern because of problems with reliability to MIL Standard, lead time, and minimum buy. This has now been solved.

4. The SEPT electronics configuration
   - First Actel 54SX32S chip is programmed (according to SEPT FPGA data sheet draft_E)
   - SEPT digital board (PCB) ready for part assembly (including FPGA)
   - SEPT analog board still under test (problem with manpower deployment at ESTEC)

5. The SEPT EGSE
   - EGSE computers are available (needs further software development)
   - Plug in cards for direct board data read out are installed (needs further software development)

6. Planned activities for October are
   - the release of an updated set of mechanical interface control drawings
   - the accomodation of a series resistor in each of the two pinpuller connections
   - the recalculation of the far field with a mismatch of the dipoles
   - the incoming inspection for the magnet system.

4.3. *Design Updates*

- Mechanical layout change requested:

Old configuration (known to the project): E-box 70 mm (front) x 80 mm (side) with mounting lugs on front and rear and sensor looking towards front and rear.
New configuration: E-Box 77 mm (front) x 69 mm (side) with mounting lugs on left and right side and sensor looking towards front and rear.

I.e. the footprint dimensions are somewhat smaller, and the E-box is rotated by 90° w.r.t. the sensor. The data connector and the bias connector are now sitting on the front side, the purge nipple and the pyro connector are sitting on either one side wall of the sensor. So far, we are free to choose left or right, the two on same or on opposite sides whichever is easier accessible.

Electronics/ FPGA
   - single count rate included in current FPGA
   - current monitor for HV-bias designed (needs to be tested)
   - current limiter under design

4.4. *Outstanding Problems*

- How to gain confidence in PIPS detectors of open telescope to be insensitive to stray light. Possible solution: perform solar simulation test (see also PDR RFA # 29).

- new grounding scheme for SEPT (?)
There is a need from SEPT to have the grounds of the instrument tied together at SEPT side, which is now in contradiction with some new spacecraft EMI constraints.

4.5. *New Problems*

- Magnetic cleanliness problem. Action required: Project or MAG PI to specify dipole and higher pole field strength, SEPT to calculate field for mismatched magnets (see also PDR RFA # 13).

4.6. *Top Risks*

None to be rated as a risk to IMPACT

4.7. *Problem/Failure Quick Look*

N/A

5. Caltech (SEP) Status

5.1. *Summary of Status*

Preparations for the PDR occupied us to a great extent during the first two weeks of September. The VLSI design continues on schedule. We hope to submit the design to the foundry in late November. Draft versions of both the Flight and GSE Software Development Plans were prepared. A separate 1553 interface between SEP and the spacecraft is under consideration at the suggestion of the Project. We are anxiously awaiting the arrival of the new contract and its associated money.

5.2. *Major Accomplishments*

Contract:

- The Statement of Work was approved.

Design reviews:

- Prepared presentation materials for the PDR.
- Prepared deliverables for the PDR.
- Participated in the PDR via telecon.

Electronics:

- PHA Chip: Detailed schematics completed; layout begun; team approach with Rick and Jill, helped by new effort by SI (Dean). Chip floor plan set and tasks divided; Rick -- preamp, Dean -- backend, Jill -- digital. Progress after two weeks is good. Still possible to make November submission. Updated VLSI doc sent to GSFC.
- Hybrid: A kickoff design meeting for the hybrid that will house the VLSI chip was held at JPL.
- MISC: Worked with Bob Baker to iron out some wrinkles in his Verilog/Altera gate array implementation of the MISC. It seems to be entirely working now.
- Data Formats: Caltech meeting led to push for common integration time base across IMPACT instruments. Basic plan for data collection from SEP instruments to SEP DPU laid out. Still need to fix basic integration interval.
- Commanding: Issue of commanding method raised by GSFC, basic approach described in e-mails to Bob Baker appears to be satisfactory to GSFC. Command response packets to be ascii encoded to form a printable, human-readable, complete command log.
- Separate 1553 interface for SEP: The idea of letting SEP talk directly to the S/C via its own 1553 interface was raised by the project. After a preliminary look, we like the idea and are to provide mass and power impacts. There would likely be no significant change in cost or software effort at CIT, provided UCB continues to be the main point of contact for JHU/APL for SEP. There are potential ITAR problems in having a direct interface to the spacecraft from Caltech electronics. This issue is being worked.

GSE:

- A preliminary GSE Software Development Plan was prepared.

Software:

- Draft version of SEP Software Development Plan prepared.

Detectors:

- Mask designs for fabrication for all HET and LET detectors were produced at Micron Semiconductor and reviewed by the HET/LET team. Final corrections will be made in October and the designs will be sent out for fabrication.
- Thermal-vacuum system for detector testing at Caltech underwent minor refurbishment and testing and is now ready for testing detectors when they are delivered in early 2002. In October we will be working on getting new vacuum system for alpha particle tests of detectors at JPL assembled and tested. This activity should be completed sometime in November.

5.3. *Design Updates*

No mass and power changes since PDR.

5.4. *Outstanding Problems*

None.

5.5. *New Problems*

None.

5.6. *Top Risks*

- Development of the L1 detector. The current approach is to produce a thin detector from a thicker one by an etching technique. The detector is pre-processed by Micron in England, shipped to the U.S. to be etched at Berkeley by a JPL employee and then shipped back to Micron for final processing. Tests of the etching process indicate that this technique will produce detectors with the required uniformity and absolute thickness. However, we have not yet had a complete detector fabricated through all the processing steps. An alternate, more conventional method is to mechanically grind down a thicker piece of silicon to the desired thickness. Tests show this produces detectors with poorer uniformity. Furthermore, the yield is rather low since breakage is an issue. Since the schedule is rather tight, we think it might be prudent to start this more conventional approach on a few detectors in parallel with the etching approach. We are investigating the cost of doing this and when we would have to start.
- Development of the VLSI chip. Currently we have only one production run planned for the chip. There is currently about 4 months total slack in the VLSI schedule. Should the protoflight run produce a part that is not in specification, we may need to re-design and re-submit. A single channel version of most of the chip has been prototyped so any failure is not expected to be total. Rather, we hope that the chip could be used in keeping the board designs on schedule while another run was submitted. The cost of the run might be $100,000, plus extra resources would be required to support the labor of any re-design activity.

5.7. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT
September 2001

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - We have the prototype telescope in house and have been using it for testing. Sandy Shuman at GSFC has lists of existing-design parts that need to be fabricated for the flight units and will be ordering them soon. Parts that have changed for the SIT design (sunshade/cover, mounting system) are still waiting for design.

b. SIT TOF System - The analog portion of the prototype TOF system has been checked with the prototype telescope and works adequately. The digital portion remains to be tested. See "Accomplishments" below.

c. SIT Energy/Logic System - This is waiting for some design input from Rick Cook on connecting the CSA to the Caltech VLSI and on the GSFC ACTEL design. The ACTEL design needs a Front-End logic specification from UMd, which we are working on.

d. SIT HVPS - Design exists, in principle. This is quiescent and needs some attention, particularly wrt the mechanical interfaces. This is an action for UMd.

6.1.1. Schedule Changes

In August we rearranged the schedule to meet Tycho's new SIT delivery dates to SEP (7/30/03) and responded to the Caltech decision to not provide early engineering model VLSI chips by eliminating the Energy/Logic prototype board. No further changes were made in September. Our current schedule is dated 8/20/01

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

This month we supported the IMPACT PDR.
In addition we hosted a visit from Axel Korth and his engineer Klaus Herrlein who brought over a prototype of the analog portion of the TOF system for evaluation with the prototype telescope. We found that the UMd-supplied design as implemented by MPAe performs as expected with 1 MeV/nuc alpha particles but that the signals from the micro-channel plates are a slightly different shape than expected. This means MPAe will need to adjust the delay lines in the constant-fraction discriminators to accommodate the new shape. It is hoped this will result in even better performance. A second design for the analog electronics was also tested but had several problems that couldn't be resolved in the time available. MPAe will concentrate on implementing the first design. The expected visit from the TOF digital electronics did not occur for a variety of reasons (Sept. 11, medical leave for UMd engineer).

6.2.2. Next Month

We expect next month to receive the digital TOF prototype from TUB and to test it with our GSE.

Also on the agenda is to deliver the SIT Front-End Logic Specification document to Tycho so this logic can be designed into the SIT ACTEL.

6.3. ***DESIGN UPDATES***

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1220	1220	0
Power (mW)	1290	1340	50
Telemetry (bps)	240	240	0

* Includes 200g bookkept by GSFC for SIT structure

Discussion: The power increase is from the analog TOF system. The power numbers for that circuit are now based on a measurement of the prototype electronics whereas they were previously based on estimates from the STEP design.

6.4. ***OUTSTANDING PROBLEMS***

We are still not under contract and have not yet entered Phase B

6.5. ***NEW PROBLEMS***

None

6.6. ***NEW RISKS***

None

6.6.1. Mitigation Plan

6.6.2. Schedule

6.7. ***PROBLEM/FAILURE QUICK LOOK***

Starts at first turn-on of flight hardware. We ain't there yet.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 1
(October 15, 2001)

September 2001

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001 On the way
Mechanical analyser fabrication end 22/04/2002
Electronics fabrication end 28/01/2002 will start soon
ETU Assembly start 06/05/2002 end 05/07/2002
Delivery to UCB 12/07/2002

7.2. *Major accomplishments*

Electrostatic analyzer design under finalization. Last verification of the design (starting from the schematics) on going using simulation software. Schematics and informations have been given to the subcontractor to start the detailed preparation of the fabrication. First report by the end of October (to be used for the thermal study). Final report by the end of November for verification. Fabrication will start at the beginning of next year.
Deflectors grids fabrication will start soon.

Electronics boards are designed. We are waiting for the finalization of the mechanical design to start the fabrication of the 3 electronics boards. Mounting into the box has to be clarified.

7.3. *Design Updates*

Mass : 1210 g
Power : 446 mW min ; 662 mW max
No change from PDR

7.4. *Outstanding Problems*

Pin puller : P5-403-10

More information are needed to be able to implement it on the top of the analyzer. The best should be to get a sample to determine precisely the interface.

Thermal design :

Preliminary study is showing that the temperature will be to low for the power on. Full study should be necessary to freeze the design. The results will have impact on the interface attachment point between the different items. We will send as soon as possible (probably end of this month) the preliminary detailed design to Bob Eby.

Interface with UCB section

Has to be defined clearly: mechanical, electrical connection (routing cables) and purging system location.

AMPTEKS amplifiers quality

It will difficult for us to have the best quality for them as done for Goddard

7.5. *New problems*

Not yet !

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

Not yet

8. GSFC (MAG) Status

Nothing to report