SWEA/STE Interface FPGA (SSF) Description/Operation

Revision 0.4
11 August 2003

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References.

1. SWEA/STE Interface FPGA (SIF) Specification, Version D, 2002-Apr-11
2. SWEA UCB to CESR ICD, Version E, 2002-Mar-29
3. STEREO IMPACT Intra-Instrument Serial Interface, Version F, 2002-Jun-19
4. SWEA/STE Interface FPGA (SIF) Description/Operation, Version 1.0, 25 March 2002

Revision History

Revision Number	Date	Change Summary
0.1	27 March 2003	Initial Draft - design based on Reference 4, but with alternate DACs. Also modified: Heater Control (changed from PWM to commanded 1-bit output) & Event Input Filter (any Pulse Reset inhibits all channels). Corresponds to SSF-FPGA Rev. 0
0.2	23 July 2003	Modifications to STE Test Pulser, Event Acceptance & Monitor Rate LLD,ULD Gating; misc. modifications as per change bars
0.3	1 August 2003	Added STE Bias DAC Load via command I/F - corresponds to SSF-Rev. 1
0.4	11 August 2003	Modified Gating of Monitor Rate Counters - corresponds to SSF-Rev 2

Table of Contents

1.0 Introduction

The SSF (SWEA/STE Interface FPGA), logic contained in an Actel 54SX32S, handles the overall control and communication requirements for two types of instruments: the SWEA/STE-D and the STE-U. It incorporates components required by both instruments; however certain of the modules can be disabled via command, enabling the same design to be used for both systems.

An external reset signal (active low) is controlled by an RC with a time constant of approximately 0.68 seconds.

The SSF is based on an earlier FPGA (SIF) which used parallel DACs for the MCP, STE-Pulser and Sweep DACs, and discrete DACs for the Threshold DACs. The SSF instead uses three quad-serial 16-bit DACs: one for the four Threshold DACs; one for the four Sweep DACs, and one shared by the MCP, the STE Bias and the STE Test Pulser DACs.

Figure 1 on page 4 (the FPGA schematic) shows an overview of the main subsystems comprising the SSF.

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Figure 1: Overall Block Diagram

2.0 Subsystem Descriptions

2.1 Timing Control

The timing (TIMCNTL) module receives the 1MHz Spacecraft clock (CLK1M), the 1 Second Tick (TK1S) and the seconds count bit 0. It creates the following signals/strobes and fowards them to the various SSF subsystems:

CYCLECLK: Occurs every 2 seconds, as parsed from the "F0" command data (every "even" instance of TK1S). Only SECS[0] is used by the TIMCNTL module.

STEPCLK: STEPCLK divides the 2 second cycle clock into 1345 intervals as follows: at the beginning of a CYCLECLK period 1344 1.45 ms intervals are generated (totally 1948.8ms). The last interval is 51.2 ms.

SAMPLECLK and SAMPLECNT[8:0]: SAMPLECLK occurs every 4th STEPCLK during the 1344 1.45ms interval period, restarting at the next CYCLECLK. SAMPLECNT, a 9-bit down-counter, is loaded with the maximum count (337 decimal, 151 hex) at the occurrence of each CYCLECLK. The counter decrements every SAMPLECLK, reaching and holding the final count of 1 during the 51.2ms interval.

TESTCYCLECLK: Occurs every ten seconds. The TESTCYCLECLK hardware does not use the F0 data directly to determine timing, but counts CYCLECLKs, "ticking" every 5th CYCLECLK (different than as described in Reference 1).

HSKPMD: Toggles between 0 and 1 every CYCLECLK when ENBSWEA is set. Jammed to zero when ENBSWEA is cleared.

TK8HZ: This tick, which occurs 8 times per second (or 16 times per CYCLECLK), is used to time housekeeping data acquisition/telemetry and the STE cover actuator "ON" durations. Since the TK8HZ is derived from the SAMPLECLK, its duration alternates between 127.6ms and 121.8ms, with one 126.6 period following each CYCLECLK.

SYN100K and SYN100KN: 100KHz Reference Supply (and an inverse version) which is forwarded to the SWEA-HVPS. The outputs are disabled (held in high impedance) when AFEPWR is deasserted or the SYNCH Disable bit (Control/Enables Register, Bit 0) is set.

2.2 Command Interface

The command interface module performs serial to parallel conversion, receiving commands in the 24-bit format described in Reference 3. If a parity error is detected, the command is ignored and an error indicator set (CMDPE). CMDPE is sent down as part of the digital housekeeping word (see Section 2.14, "Housekeeping Control," on page 17) and is reset following transmission.

The command interface module directly drives the simple control signals, either to internal SSF subsystems or off-chip to the various SWEA/STE-D or STE-U subsystems. For these outputs, any required staging is performed in the command interface module itself Other commands are forwarded to the SSF subsystems using the latched command data bus and subsystem select strobes.

The Command ID start at E0 hex.

The commands are:

COMMAND NAME	ID (Hex)	DESCRIPTION	Staged - When Effective
SRAM Buffer Select	E0	Sets Buffer Use D[1]: SWEEP Table Buffer Select - the value of this bit determines which buffer is the read buffer. D[0]: Energy Table Buffer Select - the value of this bit determines which buffer is the read buffer.	SWEEP LUT Updates at the beginning of the Next "GAP" Energy LUT updates at the Next CYCLECLK
MCP DAC Load	E1	Loads MCP DAC (8 bit value) D[7:0]: DACValue[15:8] (DACValue[7:0] remain cleared)	Immediately queued, effective within 40-200µs
SWEA/STE Controls/Enables	E2	Sets/Clears Various Controls D[15:12]: Telemetry Subsystem Enbs D15: Enable ACOUNTER Messages D14: Enable HSKPG Messages D13: Enable STE-PHA Messages D12: Enable RATES Messages D[11]: AFEPWR Force On D[10]: AFEPWR Force Off D[9]: STE Test Pulser Enable D[8]: SWEA Test Pulser Enable D[7:4]: Shaper Chain Enable[3:0] D[3]: ADCs Reset D[2]: Enable SWEA (enables the following SWEA/STE Subsystems: DAC SWEEP and SWEA Counter Readout) D[1]: STE Test Pulser Low Resolution Mode D[0]: Disable the 100KHz Synchs All bits default to disabled at reset: This results in all bits except the ADCs Reset defaulting to zero. The ADCs Reset line, which is active high, defaults to one; clearing it enables ADC operation.	Test Pulser, Telemetry Subsystem and Shaper Chain Enables take effect at the next CYCLECLK. All others are effective immediately.

COMMAND NAME	ID (Hex)	DESCRIPTION	Staged - When Effective
Protected Command Execute	E3	Sets/Clears Protected Signals D[15]: NR HV Off D[14]: MCP HV Off D[10]: SWEA Cover Actuator Off D[8]: FORCE STE Cover Actuator Off D[7]: NR HV On D[6]: MCP HV On D[2]: SWEA Cover Actuator ON D[1:0]: FORCE STE Cover Actuator ON D1: Set Force Cover In (Close) D0: Set Force Cover Out (Open) NOTE: Only one of the "On" Command bits should be set. This restriction does not apply to "Off" bits. All signals default to 0 (disabled) at reset	Setting: Synchronized to Half-Second Tick Clearing: Immediate (Setting occurs only if armed, except for STE; clearing does not require arming. When STE Cover Actuator In or Out commanded without an arm, the command executes in "non-forced" mode.)
Operational Heater Control	E4	Sets the OpHeater Value D[0]: OpHeater Value Defaults to 0 at reset	Takes effect at the next "GAPSTART", 51.2 ms before CYCLECLK
Threshold DAC Load	E5	Sets One of Four Threshold DACs D[7:6]: DAC Select D[5:0]: DAC Data NOTE: Allow at least 15μs "dead-time" between Threshold DAC load commands.	Immediately shifted, effective at next CYCLECLK
ARM Protected Command	E6	ARMs the following commands D7: 1-> ARM NR HV ON D6: 1-> ARM MCP HV ON D2: 1-> ARM SWEA Cover Actuator D1: 1-> ARM Force STE Cover In (Close) D0: 1-> ARM Force STE Cover Out (Open) NOTE: Only one of bits D7,D6,D2,D1 & D0 should be set; if more than one are set, the arm does not occur.	Immediate (Enables future commands): expires in 14-16 seconds
SWEEP Housekeeping Channel Select	E7	Selects Active Housekeeping Channel for Sweep Housekeeping Mode D[3:0]: SWEEP Housekeeping Select	Next CYCLECLK

COMMAND NAME	ID (Hex)	DESCRIPTION	Staged - When Effective
LUT Address Pointer Write	E8	D[14] - LUT Sector Select 1 sets pointer to SWEEP LUT 0 sets pointer to ENERGY LUT D[13:1] - Word Address[13:1] Address pointer for IDPU writes to the Sweep Look-up Table, loaded into a word counter, whose output drives MemAddr[13:1]. The address is incremented by one following each LUT Data Write.	Immediate
LUT Data Word Write	E9	D[15:0] - Data to be written to current LUT location, determined by both the corresponding Buffer Select and the LUT Address Pointer	Immediate
Memory Quadrant Select	EA	D[1:0] - Set MemAddr[18:17] - Drive the upper 2 bits of SRAM; these bits default to zero at reset.	Immediate
Memory Test Mode	EB	D8=1 => TestMode Selected D[7:0] sets MemAddr[16:9] for accumulator telemetry readouts if TestMode is asserted	Bit[8] - Next CycleClk Bits[7:0] - Immediate
STE Cover Time-out Delay	EC	Sets STE Door Timeout D[3:0] - 16 settings, in $^{1}/_{8}$ second increments from $^{1}/_{8}$ second at the minimum setting of zero to $^{15}/_{8}$ second at 14 (E-hex). The setting of 15 (F-hex) selects an infinite timeout.	Immediate
STE Bias Supply DAC Load	ED	Loads STE Bias Supply DAC (8 bit value) D[7:0]: DACValue[15:8] (DACValue[7:0] remain cleared)	Immediately queued, effective within 40-200µs

2.2.1 Protected Commands

The following commands are protected:

- Enabling the High Voltage Power Supplies (NR HV ON and MCP HV ON)
- Activating the SWEA Cover Actuator (SWEA Cover Actuator ON)
- Activating the FORCE STE Cover Actuators (Force STE Cover Actuator In ON & Force STE Cover Actuator Out ON)

A protected command is executed as follows:

1. Write the appropriate ARM to the "ARM Protected Commands (ID E6). The ARM command should only have one signal set; if more than one signal are set, it is ignored. The ARM expires in 15-16 seconds. During the period when a command is ARMed, all other ARM command are ignored.
2. Issue the corresponding execute command "Protected Command Execute (ID E3)" less than 15 seconds after the ARM command dispatch. The execute bit, must match the ARM bit, or the command is ignored, and the ARM is deactivated. Additionally, if more than one "ON" bit is set in the execute command, the command is ignored and the ARM is deactivated.

Note: Like "Radio Buttons", the "Protected Command Execute" only sets or clears when the applicable bits in the command are set. Clearing signals does not require arming, and can be issued with multiple clears in one execute. Clearing always overrides setting, if they occur simultaneously in the same execute command.

A Protected Command Subsystem error is registered in the following cases:

- Timeout Error: the arming occurs and expires with no execute command received.
- Invalid Execute: the arming occurs and is followed by an invalid execute (more than one ON bit set, or the incorrect ON bit set).
- Illegal Arm: more than one signal armed, or an all zero arm received when the Protected Command Subsystem is in the IDLE state.
- Unarmed Execute: Execute occurs (Bits D7 or D6 or D2 set) when the Protected Command Subsystem is unarmed. (NOTE: If bits D0 or D1 are set in an execute command, the command executes, but in "nonForced" mode.)

The error, which is available as digital housekeeping, is cleared once it has been read-out.

A "disarm" capability is available. The user can undo an arm by sending another arm command with a data value of all zeros. (NOTE: if a "disarm" is received when the system is not currently armed, an error will be flagged.)

2.3 Latchup Protect

The Latchup Protect (LATCHUPPROT) module manages AFEPWR based on the states of an external overcurrent detect: AFESHDN and two commanded controls. The two commanded parameters, which both default to zero, are AFEPWR Force Off (AFEPWROFF) and AFEPWR Force On (AFEPWRON).

The following truth-table describes the AFEPWR control:

AFESHDN	AFEPWROFF	AFEPWRON	AFEPWR
0	0	0	Previous State
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

AFEPWR is active high: a logic 1 indicates that the supplies are turned on, and the system is active. AFEPWR is cleared at reset.

The "Force" signals, AFEPWRON and AFEPWROFF, cleared by reset, are set/cleared via the command interface. Note that AFEPWRON must be set following a reset in order to turn on AFEPWR.

An assertion of AFESHDN (when AFEPWRON is deasserted) clears AFEPWR. This clear is latched; AFEPWR remains off even when AFESHDN deasserts. Following a clear, AFEPWR can only be switched on via the command I/F (AFEPWRON).

The clearing of AFEPWR in the event of an AFESHDN assertion occurs asynchronously. The resetting of AFEPWR due to a force (AFEPWRON) occurs synchronously. As a result, if the clocks are absent for any reason, the power can be turned off by the hardware if AFESHDN asserts. Power will not be restored, however, until either clocks are restored and the appropriate command issued.

NOTE: to exit "Force" mode, the AFEPWRON and AFEPWROFF signals should be explicitly commanded to zero directly following the force.

The following SSF modules are held in reset when AFEPWR is deasserted: ACOUNTERS, DACSWEEP, MPDACWR, EVPROC, MRCOUNTERS, TDACWR, STETESTPULSE, ATESTPULSE, and MCPDAC. Most of the HSKPR module is reset. The Housekeeping ADC controller is held inactive, but the request for housekeeping telemetry is kept active, asserting every $^1/_8$ second. This allows for transmission of digital housekeeping during AFESHDN periods.

The following SSF modules are "kept alive" during AFEPWR deassertion: TIMCNTL, COMMANDIF, MEMCNTL, TLMMNGR, COVERCNTL, a portion of HSKPR, and the LATCHUPPROT module itself.

Both AFEPWR and AFESHDN are available as status via the digital housekeeping register.

AFEPWR, which controls the external power switches for the analog supplies, is also fed to SSF subsystems so that the analog circuitry inputs can be suppressed when the power is off. The HV Enables, ADCRESET, Shaper Chain Enables, and ENBSWEA signals are cleared when AFEPWR goes off, and remain cleared until commanded on.

The following outputs are forced into a high-impedance state when AFEPWR is deasserted:

Signal/Bus Name	Description
ADCSOC[3:0]	Shaper Chain ADC Start of Conversion
ADCREAD[3:0]	Shaper Chain ADC Read
AMUXSEL[2:0]	Housekeeping Analog Mux Selects
AMUXENB[1:0]	Housekeeping Analog Mux Enables
HADCSOC	Housekeeping ADC Start of Conversion
HADREAD	Housekeeping ADC Read
DACDATA[7:0]	Dac Data Bus
DAC Control Lines	Dac Clears, Dac Latches, DAC Writes, DAC Byte Selects
TDAC Data	Threshold DAC Data Lines
100KHz Synchs	100KHz Synch Signals
STETESTPULSE	STE Test Pulser
ATESTPULSE	Anode Test Pulser

Cover Actuator Controls, the Operational Heater Pulse, and the Memory Control signals (MEMOE, MEMWR and MEMCS) remain driven during AFEPWR shutdowns.

2.4 SWEA/STE DAC Sweep Control

The Sweep Control subsystem (DACSWEEP) is responsible for loading four DACs at the STEPCLK frequency, and cycling through a preloaded pattern every CYCLECLK. The IDPU loads the SWEEP LUT portion of memory and initiates LUT buffer swapping via the command interface.

Every STEPCLK, the DAC Sweep Control logic reads four 16-bit words from Memory. The controller tracks the current address and requests SRAM cycles via the memory arbiter. Upon assembling a 16-bit word, DACSWEEP transfers the word to the DAC serial input via a 16-bit shift register (operating at 500KHz). The DAC (an AD5544) stores the data in an internal holding register. For every STEPCLK, DACSWEEP repeats the memory read/DAC-Data shift four times. The DAC data becomes effective at the next STEPCLK, when it is transferred from the 16-bit holding register to the output register.

NOTE: The uppermost memory address bits [13:12] are driven by DACID during the memory reads, so that each DAC is assigned its own quadrant in the Sweep memory segment. The same DACID is used when shifting data to the AD5544.

The Sweep DAC assignment is defined as:

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0-> Analyzer; 1-> Deflector 1; 2-> Deflector 2; 3-> V0
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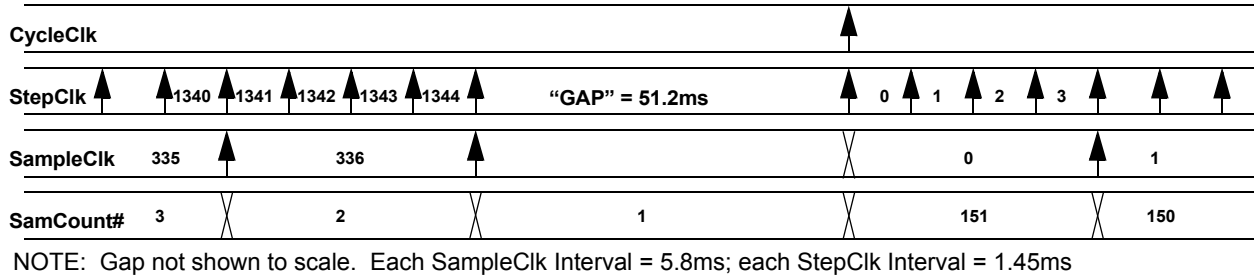
2.4.1 Sweep DAC Sequence

Figure 2 (below) shows the StepClock and SampleClock relationships just prior to and just following the occurrence of CYCLECLK. The system is designed such that the first SWEEP_LUT value (at address 0) will be clocked into the DAC exactly at CYCLECLK. (These values are written to the DACs at the start of the 51.2ms final interval (the "GAP") and then latched in coincident with CYCLECLK.)

The final DAC Values (addresses A80-A81 of the SweepDACCount sections of the Sweep LUT memory) are latched into the DACs at the start of the GAP. These values are held for 51.2ms, until the occurrence of CYCLECLK.

Note that the first SAMPLECLK following the GAP occurs 5.8ms after CYCLECLK. Thus, even though SampleCount changes at CYCLECLK, the Anode Counter telemetry isn't transmitted coincident with CYCLECLK. The first Anode Counter Telemetry Message following a CYCLECLK occurs 5.8ms after CYCLECLK with SAMCNT=150. This represents the accumulation during the GAP and the first 5.8ms interval. Anode counter messages then occur every 5.8ms with the SAMPLECNT decrementing each time. The last message, with SAMPLECNT=1 is sent at the start of the GAP, and represents the accumulation at the 5.8ms interval right before the GAP.



NOTE: Gap not shown to scale. Each SampleClk Interval = 5.8ms; each StepClk Interval = 1.45ms

FIGURE 2. SWEA Interval Sequence

SampleCount, also used by the SWEA/STE Test Pulser Subsystem (see Section 2.8, below), sets the frequency of the Anode Test Pulse.

2.5 MCP & STE Bias Supply DAC Control

The MCP & STE Bias Supply DAC Control (MCPDAC) module receives a signal from the Command I/F following the reception of either an MCP or STE Bias Supply DAC Load Command. It immediately requests the a shift/load cycle from the MCP/STE-TestPulser DAC (MPDACWR) controller. If a DAC request is initiated when the STE Pulser is active, there may be latency of up to 160µs between the command reception and the MCP or STE Bias Supply DAC load completion. When the STE Pulser is disabled, the latency is approximately 40µs.

The commanded data is transferred to the upper 8 bits; the lower 8 bits are always set to zero. If two back-to-back MCP or STE Bias Supply DAC load commands are received, the second one is ignored.

The DACs are cleared by the assertion of RESET or the deassertion of AFEPWR. Since the DAC package is shared by the STE Test Pulser and Bias Supply DACs, the MCP DAC cannot

automatically be cleared when ENBSWEA is deasserted. If it is required that the MCP DAC be cleared, it should explicitly be set to zero via the MCP DAC load command.

2.6 STE Test Pulser

The STE Test Pulser (STETESTPULSE) module both programs an external DAC and generates a test pulse. It is enabled via command: (Controls/Enables Command ID E2), STE Test Pulser Enable.

When enabled, the DAC ramps up from zero to its maximum count (65536) incrementing by one approximately every 500µs. (The actual sequence of pulses is somewhat irregular because the decode is based on the 1.45ms STEPCLK. The spacings of the pulses are as follows: two 512µs followed by one 426µs. The last spacing, at CYCLECLK, is 452µs.)

The Ramp begins upon detection of a TESTCYCLECLK. The pulse, generated before each DAC increment, is active low and lasts 16µs. The DAC data is updated at the rising edge of the test pulse by the MPDACLD output. When the DAC count/value reaches its maximum, the DACs are cleared and the pulses are stopped. The DACs remain at zero until the next TESTCYCLECLK, at which time the DAC ramping and test pulses are restarted. If the STE Test Pulser is commanded off following a period of activity, it will write all zeros to the DAC and then deactivate. This insures that the STE Test Pulser DAC is cleared when inactive.

TESTCYCLECLK has a period of 10 seconds. Since the ramp period is 32 seconds, there may be some uncertainty in the telemetry. Three TESTCYCLECLK marks will appear for each ramp. If the test pulser is left on, the ramps will occur every 40 seconds: 32 seconds on and 8 seconds off.

A low resolution mode (selected by setting Control/Enables register bit 1) is available. Selecting this mode forces the lower13 bits of the STE Test Pulser DAC values to zero. The ramp thus contains only 8 values, evenly spaced over the 32 second period.

All DAC writes must be arbitrated through the MCP/STE-TestPulser DAC (MPDACWR) controller, which manages the shared quad-DAC package.

2.7 MCP/STE Bias Supply/STE Test Pulser DAC Controller

The MCP/STE Bias Supply/STEP DAC Controller (MPDACWR) receives DAC requests from both the STE Test Pulser Subsystem (every ~500µs when active) and the MCP & STE-Bias Supply DAC subsystem (initiated by the command interface).

The STETESTPULSE module outputs timing information which allows MPDACWR to schedule the MCP or STE Bias Supply DAC writes. When the STE Test Pulser is disabled, the command interface initiated DAC Writes are always enabled. When the STE Test Pulser is enabled, the command interface DAC Writes are disabled approximately 128µs per 500µs cycle of the Test Pulser. This allows sufficient time for loading the STE Test Pulse in order to update its DAC when required. The command interface DAC write request wait period ranges from 1-128µs (measured from the time the DAC Load Command is shifted in). The DAC output registers are loaded immediately following an MCP or STE Bias Supply DAC data-shift.

DAC-IDs are assigned as follows: STE Test Pulser = 0; STE Bias Supply = 2; MCP = 3. (DAC 1 is unallocated.)

Because of the accrued delays, the latency between when an MCP or STE Bias Supply DAC load command is issued until the DAC value is registered can be almost 200µs (27µs for the command shift, 128µs worst-case wait when the STE Test Pulser is active, and another 36µs to perform the DAC shift/load). MCP DAC loads and STE Bias Supply DAC loads should therefore be separated by at least 200µs when the STE Test Pulser is enabled; they should be separated by at least 40µs when the STE Test Pulser is disabled.

An output load pulse is also generated by the STE Test Pulser subsystem (when active) approximately every 500µs. The logic enforces the minimum delays between the shift and load operations for both subsystems.

2.8 SWEA/STE (Anode) Test Pulser

The Anode Test Pulser (ATESTPULSE) module generates a variable frequency test pulse, used to stimulate the SWEA anodes during testing. It is held in a reset state (at which time the output is a logic low) when the SWEA is disabled or when the SWEA Test Pulser is disabled. The test pulse is activated via the Controls/Enable command.

When enabled, the ATESTPULSE frequency is stepped up each SAMPLECLK and returns to the start frequency (approximately 3KHz) at each CYCLECLK.

The Anode Test pulser generates a pulse train based on CLK1M divided by SAMPLECNT[8:0] (see Figure 2, above). SAMPLECNT[8:0] is decremented each SAMPLECLK and set to the starting number of 151hex (337dec) each CYCLECLK. The pulse, which is active high, is one microsecond in duration for all intervals. During the 51.2ms “gap”, the test pulse reaches its maximum frequency of 500KHz.

2.9 Threshold DAC Controller

The Threshold DAC (TDACWR) write controller manages the shifting/loading of four DACs housed in an AD5544, Serial Input 16-bit Quad-DAC. Although the AD5544 DACs are 16-bits, only the most significant 6 bits are used; the lower 10 bits are set to zeros.

They are programmable via the threshold DAC Load Command, with bits[7:6] selecting the DAC to be loaded, and bits[5:0] containing the DAC data to be loaded. The 16-bit shift is initiated immediately upon the arrival of a Threshold DAC load command. The data, however, is not forwarded to the DAC output until the occurrence of the next CYCLECLK.

NOTE: Since DAC loads require approximately 40µs, a dead-time of at least 15µs must be guaranteed between Threshold DAC commands. If two TDAC commands are received back-to-back, the second one will be ignored. (It is permissible to issue a “non-TDAC command” immediately following a TDAC command.)

2.10 Cover Actuator Control

The control logic in this module (COVERCNTL) provides switch control for the cover actuators. Both cover actuator outputs are active high.

All cover commands should be separated by the timeout period of the cover subsystem (maximum = 2 seconds). If a cover actuator command is received when the cover subsystem is already active, it is ignored.

2.10.1 SWEA Cover

There is one 1-time opening cover on the SWEA. This switch shall be activated via the IDPU command I/F (Actuator Enables - Command E3).

The SWEA cover control is a “protected command”, requiring a sequence of two commands in order to take effect. (See Section 2.2.1, “Protected Commands,” on page 9.)

The actuator control bit automatically clears two seconds after it is set via the arm/execute sequence. It can also be cleared explicitly via the command interface. There is no arm required for clearing the actuator control.

2.10.2 STE Cover

STE has a reclosable cover. There are two switch controls to the STE and two status signals from the STE. The controls are activated via the command I/F (Actuator Enables): one commands the cover open and the other commands the cover shut. When one of these commands is received, power is supplied to the appropriate actuator, until the status signal feedback indicates that the cover has reached its desired position. If the corresponding status signal is low, the actuator power is inhibited. If at any time, the OPEN or CLOSE commands are received with the data bit set to zero, the actuator control will be deasserted immediately, regardless of the state of the status feedback. If both a set OPEN and CLOSE command are asserted simultaneously, neither command shall register.

(The SSF STE Cover control and status signals corresponding to OPEN are STECOVSW0 and STECOVSTAT0; those corresponding to CLOSE are STECOVSW1 and STECOVSTAT1.)

There is also a “force” command available for each STE actuator. This allows power to be supplied to the appropriate actuator regardless of the state of the feedback status signal. The force commands are protected via an “arm-execute” command sequence (one arm per actuator). (See Section 2.2.1, “Protected Commands,” on page 9.)

The activator enables, whether in “force” mode or not, automatically clear within a programmable delay period after assertion. The Programmable Delay is set via Command STE Cover Timeout Delay (ID EC) to a value ranging from $^{1}/_{8}$ to $^{15}/_{8}$ seconds. (NOTE: the $^{1}/_{8}$ increments are not exact; see the description of TK8HZ in Section 2.1, “Timing Control,” on page 5 for more detail.) An “infinite” timeout setting is also available. When using the infinite timeout setting, the status signals will still serve as a shutoff if the system is operating in non-forced mode. However, when in forced mode, the actuator remains energized until the FORCE STE Cover Actuator OFF is received via the command I/F. The FORCE STE Cover Actuator OFF command must also be issued if in non-forced mode with an infinite timeout set and the corresponding status feedback is stuck high.

2.11 Anode Counters

The Anode Counter (ACOUNTERS) module contains 16 counters, each 14-bits, which register pulses generated by the SWEA anodes.

Anode Pulses are 250-300ns, positive-going pulses; rising edges are counted. As the fastest clock used by the SSF is 1MHz, each anode pulses must be fed directly to the clock of its counter. (So if the input is noisy, the counter will increment. Also, runt pulses may be registered as counts.)

Each SAMPLECLK, the count values are transferred to holding registers, and the counters are cleared. The Telemetry Manager subsystem (see Section 2.16 on page 22) is responsible for reading out the holding registers (and the sweep housekeeping value) following each SAMPLECLK. There may be a few microseconds of downtime during the count latching/ clearing every SAMPLECLK.

This module is held in a reset state when ENBSWEA is deasserted.

2.12 Event Processing

The event processing (EVPROC) subsystem handles the outputs from the STE shaper circuits. The EVPROC module is held in a reset state if either of the following occurs: ADCRST is asserted or AFEPWR is off. At initialization, first AFEPWR should be forced on and ADCRST should be deasserted; next the analog chains can be enabled/disabled (via the Controls/Enables command).

The four analog chains each drive a separate set of control/pulse signals, but share a common 12-bit ADC data bus. (This ADC data bus is also shared with the 12-bit analog housekeeping ADC data bus. Arbitration, between the four analog chains as well as the HSKPR module, is performed by the Event Processing subsystem.)

A combination of control signals (as described in Reference 1) determine whether an event should be processed. The SSF-FPGAs differ from Reference 1 in the following ways:

- the Pileup Filter accepts events with no minimum spacing required between the rising edge of LLD and the falling edge of Peak. As long as LLD is asserted when the Peak falling edge is detected, and if LLD has not been asserted for more than 4-5 μs, the event will be accepted.
- if any of the chain PULSERST signals (active high) are asserted when that chain is enabled, no chain shall accept events. (If a chain is disabled, the state of its PULSERST has no effect on the other chains' events.)

Upon acceptance, the SSF issues an ADCSOC pulse to the active chain. ADCSOC is initiated via combinational logic only, in order to insure a small time delay. The SSF then waits for the busy line to transition high (25ns MAX) and deasserts ADCSOC. When the busy line returns to low, it is queued up for readout and processing.

After conversion, a request is made to the Event Arbiter/Processor subsystem. Each chain is allowed to convert when another event from a different chain is being processed. However, any further events in the same chain that arrive while an event is still pending are dropped.

Following readout, the EVPROC module uses the ADC Data along with the Detector ID as an index to a lookup table, located in external RAM. The 8-bit value returned is used as an index to a 16-bit counter, also located in external RAM. EVPROC reads the counter value, increments it, and writes it back into memory. Only the modified counter byte needs to be read/written back into memory. This eliminates two memory cycles for most cases.

Processing takes a minimum of 3µs, and there is a required IDLE state between event processing for each chain. Processing time could be longer depending the value of the accumulator count (6µs required if the lower byte of the accumulator count= FFhex) and increases if other memory clients (Telemetry, Sweep DAC and LUT Write subsystems) are accessing SRAM.

The arbiter is non-preferential. If all four detector chains are continuously receiving events, each will receive one-fourth of the event processing subsystem bandwidth. However, if only one detector is active, this chain will receive the total available bandwidth. An enable is provided for each analog chain, so that a noisy channel can be disabled.

2.13 Rate Counters

The Rate Counter (MRCOUNTERS) Module contains 12 counter/accumulators. Three signals from each PHA chain are used to clock the counters, which are latched into holding registers and cleared every occurrence of a "free-running" version of SAMPLECLK (SAMPLECLKINT: does not stop during the "GAP"), approximately once every 5.8ms. Each accumulation interval, the Telemetry Manager reads the latched values and assembles them into a message. If the counters reach their maximum during any time during the accumulation, they lock this value in until cleared.

For PHA chain, the following signal assertions are counted:

Counter Clock	Number of Counter Bits
LLD	9
ULD	4
PULSERESET	3

The LLD and ULD count-enables are inhibited by the assertion of PULSERESET from any of the active chains. The PULSERESET count-enables are inhibited by the assertion of PULSERESET from any of the other active chains.

The counting not synchronized to the 1MHz clock. Each signal rising edge clocks a counter, which freezes at the final count. The counters are latched and reset every interval (during which time the subsystem will incur a few microseconds of dead-time). All accumulation intervals except the interval immediately preceding CYCLECLK are 5.8ms. The last interval of a 2 second cycle, which is 4.8ms, is marked in the telemetry stream with a MessageID tag.

2.14 Housekeeping Control

At initialization, the Housekeeping ADC must be activated (via the Controls/Enables command). (The Housekeeping ADC shares a command bus and reset line with the Detector ADCs.) The Housekeeping module powers up and remains in "Shutdown Mode" (described below) if ADCRST is asserted or if AFEPWR is off.

The Housekeeper (HSKPR) module receive a status signal (HSKPMD) and a timing signal from the TIMCNTL subsystem. HSKPMD, which toggles every CYCLECLOCK, selects either CYCLING or SWEEP Mode. The timing signal occurs 8 times/second, or 16 times every CYCLECLK. (NOTE: The 8Hz Housekeeping frequency is slightly uneven: some intervals may be 122ms, while others might be 128ms.)

When in CYCLING mode: at CYCLECLK the AMUX channel is set to zero. At the first DOHSKP, HSKPR performs an ADC conversion and latches the result. (NOTE: All ADC Reads must be negotiated through the Event Processing subsystem ADC bus arbiter.) When the readout has completed, HSKPR informs TLMMNGR, which constructs a message containing the 12-bit ADC result in bits 11:0 and the 4-bit Analog Mux channel in bits 15:12, followed by the 16-bit digital housekeeping register. After latching the current result, HSKPR increments the AMUX channel in preparation for the next conversion, which occurs at the next DOHSKP tick. This process continues until the 16-values have been scanned through in one CYCLECLK period.

When in SWEEP mode: The Housekeeper maintains a 4-bit register, loaded via command, which sets the analog channel for ADC conversions. At the next CYCLECLK when HSKPMD=SWEEP, the AMUX channel is set to the commanded value. Conversions are then performed every SAMPLECLK. TLMMNGR still reads the result and constructs messages (the last ADC conversion followed by the digital housekeeping register) eight times per second; however the AMUX channel is not incremented. TLMMNGR also appends the ADC result onto the SWEEP messages.

Housekeeping is kept in CYCLING mode when ENBSWEA is deasserted.

Housekeeping “Shutdown Mode” provides transmission of digital telemetry even when the analog subsystem is inactive. During periods of AFESHDN (when AFEPWR is deasserted or ADCRST is asserted), if Housekeeping Telemetry is enabled, the Housekeeping subsystem will enter a special “Shutdown Mode”. In this mode it sends telemetry every 1/8 second, but does not interact with the ADC (since the ADCs are powered down). While in Shutdown mode, the AMUX Channel count is held at zero.

The digital housekeeping register provides status from the various digital and external subsystems. The register is defined as follows:

Bit Position(s)	Signal Name	Definition
15	PCE	Protected Command Subsystem Error Detect (occurred in previous 1/8 second interval)
14	ENBSWEA	SWEA Subsystem Enable
13	ENBSWEATP	SWEA Test Pulser Enable
12	ENBSTETP	STE Test Pulser Enable
11	HSKPMD	Current Housekeeping Mode
10	NRHVENB	NR High Voltage Enable
9	MCPHVENB	MCP High Voltage Enable
8	ANORM	OR of any unusual setting or conditions
7:6	STECOVSW[1:0]	STE Cover Switch Control Outputs
5:4	STECOVSTAT[1:0]	STE Cover Status
3	SWEACOVSTAT	SWEA Cover Status
2	AFESHDN	AFE Shutdown
1	AFEPWR	AFE Power
0	CPE	Command Parity Error in previous 1/8 second interval

The ANORM signal indicates a divergence from normal operational mode. It ORs the assertion of the following conditions or signals: AFEPWRON, AFEPWROFF, the Telemetry Subsystem

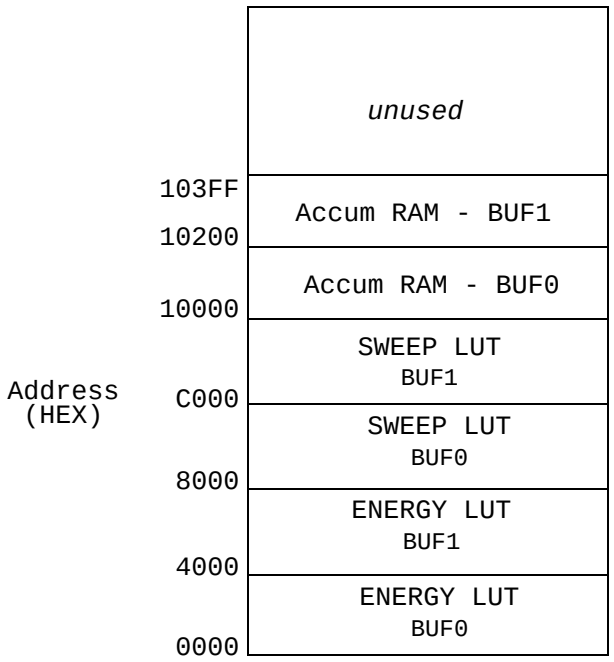
Disables*, Protected Command Subsystem Currently Armed, and all of the Shaper Chain Disables.

* (NOTE: ANORM is asserted if ACOUNTER Messages are disabled when SWEA is enabled OR if ACOUNTER Messages are enabled when SWEA is disabled.)

2.15 Memory Cycle Control

An external 512Kx8 SRAM holds the various data buffers used by the SSF: the Energy LUT, the Accumulator RAM, and the Sweep LUT. All of these SRAM Areas are double buffered. The LUT buffer select is determined by IDPU command; the Accumulator RAM buffer select is swapped regularly as messages are read-out.

Memory allocation is shown below:



The address bits are driven by the various memory clients as follows:

Cycle Type	18:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW-LUT-WR	Mem-Quad Sel	0	1	$\overline{SB}$	LUTAddrPtr[13:1]													CMD-Byte-Sel
EN-LUT-WR		0	0	$\overline{EB}$	LUTAddrPtr[13:1]													CMD-Byte-Sel
TLM-Acc-Readout		1	0	0	0	0	0	0	AB	TLMSubSysWordAddr[8:1]								TSS-Byte-Sel
EVPROC-LUT-RD		0	0	EB	DetID[1:0]		EventEnergy[11:0]											
EVPROC-ACC-R/W		1	0	0	0	0	0	0	$\overline{AB}$	AccumAddr[8:1]								EVP-Byte-Sel
SW-DAC-RD		0	1	SB	DacID[1:0]		SWEEPDACCNT[13:1]											SWP-Byte-Sel

where SB = Sweep LUT Buffer Select; EB = Energy LUT Buffer Select; and AB = Accumulator Buffer Select.

Bits[18:17] of the SRAM, programmable via the Memory Quadrant Select register, select between the four segments of RAM. This function might be useful if a memory cell develops a problem during the life of the mission.

The Memory Controller (MEMCNTL) manages the cycles to the 8-bit SRAM, selecting between the following memory clients: DACSWEEP, EVPROC, TLMMNGR, and COMMANDIF.

The DACSWEEP module must read out of SRAM in order to update the Sweep DACs. It requires eight byte reads every STEPCLK.

EVPROC requires one byte read (counter address), followed by one byte read and one byte write (counter LSB increment), the possibly a second byte read/byte write (counter MSB increment).

TLMMNGR requires 512 byte reads followed by 512 byte writes (clears) every CYCLECLK, for the accumulator messages.

COMMANDIF requires one word write each time a LUT DATA WRITE command is received. Both LUT address registers and write control subsystems are included in the MEMCNTL module. When an LUT address write command is received, a counter is loaded. This word counter increments following each LUT data write. A registered LUT Sector Select, which determines whether a LUT write goes to the SWEEP LUT or to the ENERGY LUT, drives bit 15 of memory. Bit 14 of memory is driven by the inverse of the corresponding buffer select. When an LUT data write command is received, the data is written into memory low byte first.

MEMCNTL coordinates all the SRAM buffer controls, based on input from the Command I/F and the various timing signals. It selects the client for the current cycle (delineated by CLK1M), drives the selected address, data and control strobes onto the memory bus, and informs the client

that the cycle has been completed. The memory bus arbitration scheme is fixed with the following priority assigned: 1: TLM, 2: CMD, 3: SWP, 4: EVPROC. This assures that each client is able to obtain the bus with a small enough latency to assure continuous operation. For example, when TLMMNGR is reading out the accumulator RAM, two byte reads must occur at least every 16µs in order to keep up with the message generation. Bursts are spaced out at the subsystem level so that none of the higher priority subsystems will ever monopolize the bus.

2.15.1 Memory Test Mode

A dedicated Memory TestMode can be selected via the command Interface (Command ID EB). (Note: the TestMode bit is staged and takes effect at the next CYCLECLK.) In Memory TestMode the upper bits of SRAM can be jammed into a set state for telemetry readout. This allows for a readout of the LUT sections of SRAM. Testmode also permits data to be jammed into the accumulator section of SRAM, allowing for a complete end-to-end test of all SRAM locations.

LUT Writes behave almost the same when TestMode is set. There is one exception: if TestMode MemAddr[16] is set (choosing the accumulator for Telemetry Readout), all LUT Writes are directed to the Accumulator section of SRAM (memory bit 16 set).

During TestMode, the accumulator is not cleared following a telemetry readout.

2.16 Telemetry Manager

The telemetry manager (TLMMNGR) module constructs, formats and serializes messages in accordance with the requirements outlined in Reference 3. The following message types are constructed by TLMMNGR:

Message Type	ID (HEX)	Length (DEC)	Frequency	Description
Anode Counters without HSKPG	30	18	336 msg/ CYCCLK - every other CYCCLK	The 16 latched counter values accumulated by the SWEA Anodes every SAMPLECLK, followed by the SAMPLECNT value (bits 8:0) for the accumulating interval.
Anode Counters with HSKPG	31	19	336 msg/ CYCCLK - every other CYCCLK	The 16 latched counter values accumulated by the SWEA Anodes every SAMPLECLK, followed by the SAMPLECNT value (bits 8:0) for the accumulating interval, followed by the SWEEP Housekeeping Value (bits 11:0) and analog mux channel (bits 15:12).
Energy Bin Counters TESTCYCLKCLK =0 MTESTMODE = 0	32	257	one msg/ CYCCLK	The 256 event counters used for STE PHA.
Energy Bin Counters TESTCYCLKCLK =1 MTESTMODE = 0	33			
Energy Bin Counters TESTCYCLKCLK =0 MTESTMODE = 1	3A	257	one msg/ CYCCLK	Contents of the 256 memory locations selected by the TestMode Register
Energy Bin Counters TESTCYCLKCLK =1 MTESTMODE = 1	3B			
Rates	34	13	344 msg/ CYCCLK (1 msg/ ~5.8msec)	The 12 monitor rate counter values accumulated over the CYCLECLK interval There are three data words per each of the four chains, arranged as follows (where word 0 is the message header): WORD 1: LLDLatchedCount[8:0] - Chain 0 WORD 2: LLDLatchedCount[8:0] - Chain 1 WORD 3: LLDLatchedCount[8:0] - Chain 2 WORD 4: LLDLatchedCount[8:0] - Chain 3 WORD 5: ULDLatchedCount[3:0] - Chain 0 WORD 6: ULDLatchedCount[3:0] - Chain 1 WORD 7: ULDLatchedCount[3:0] - Chain 2 WORD 8: ULDLatchedCount[3:0] - Chain 3 WORD 9: PulseResetLatched Count[2:0] - Chain 0 WORD 10: PulseResetLatched Count[2:0] - Chain 1 WORD 11: PulseResetLatched Count[2:0] - Chain 2 WORD 12: PulseResetLatched Count[2:0] - Chain 3

Message Type	ID (HEX)	Length (DEC)	Frequency	Description
Rates - 1st Message	35	13	1 msg/ CYCCLK	Monitor Rates, in format described above. Message ID 35 is reserved for the first message following a CYCLECLK.
Housekeeping	36	3	8 msg/sec	The most recently converted HSKPG-ADC value, followed by one Digital Housekeeping value

The length is the number of telemetry message words, including the first (header) word. (The header word contains the message ID in the upper 6 bits and LENGTH-2 in the lower 10 bits, as specified in Reference 3.) TLMMNGR handles the timing for Anode Counter readout, starting the message construction following every SAMPLECLK, and extracting the necessary data from the ACOUNTER (and HSKPR if in SWEEP Housekeeping mode) modules.

TLMMNGR constructs and transmits the housekeeping message upon receipt of the signal HKPGDN from HSKPR, generated following each ADC conversion, 8 times/second.

The Energy Bin Counters: While TLMMNGR is constructing Energy Bin Counter messages, it requests RAM via MEMCNTL for two byte reads per counter readout. The Accumulator Buffer is cleared as a block action after the message is constructed, but preceding the Accumulator Buffer Swap. During the accumulator clear phase, each memory request is spaced by an interval of one step clock. This prevents TLMMNGR from accessing memory too frequently, which could cause the other subsystems to slow down.

The accumulator RAM is not cleared until one message buffer has been read out. This invalidates the first accumulation following system start-up.

Each telemetry message type has its own enable, which is set via the command I/F. Additionally, each subsystem's telemetry is inhibited if the corresponding subsystem is disabled. Only Housekeeping Packets are transmitted when AFEPWR is off. Anode Counter Messages are enabled only when ENBSWEA is asserted.