STEREO
IMPACT

SWEA/STE Interface FPGA (SIF) Specification

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Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2002-Jan-17	Preliminary Draft	-
B	2002-Mar-15	• Operational PWM frequency to 100KHz to limit EMC • Add PHA & DAC interface details • Add STE cover control	
C	2002-Mar-29	• Add HV Sync signal	
D	2002-Apr-12	• Add STE monitor rate counters • Minor fixes	

Distribution List

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1. Introduction

The SWEA/STE Interface board interfaces between the SWEA and STE instruments and the IDPU. There are two versions of this circuit; one for SWEA and STE-D, which shall be mounted in the base of SWEA, and one for STE-U, mounted in the IDPU. Both versions use a common FPGA design for the digital logic part of the circuit (together with an external RAM used for look-up tables and accumulators). Since the STE-U interface does not require the SWEA functionality, a signal shall be provided to enable or disable this functionality, so that the same FPGA design can be used for both. This specification describes that FPGA, called the SWEA/STE Interface FPGA, or SIF.

1.1. *Document Conventions*

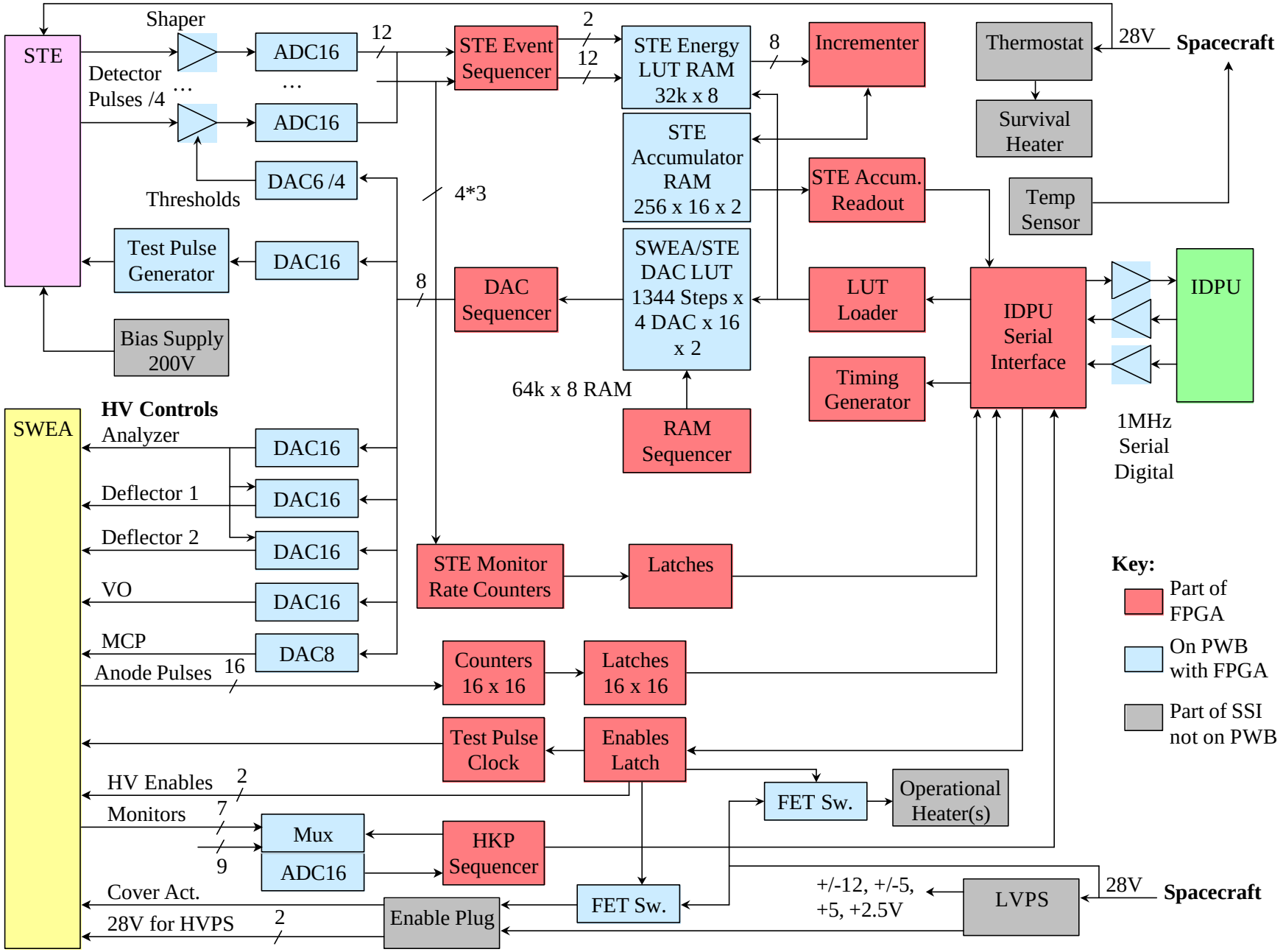
In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by UCB and /or Elf indicating who is responsible for providing the data, and a unique reference number.

1.2. *Applicable Documents*

The following documents include drawings and STEREO Project policies, and are part of this specification. In the event of a conflict between this Specification and the following documents, this Specification takes precedence. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

1. ICD/SWEAICD
2. ICD/Impact Serial Interface
3. ICD/IMPACT Harness
4. Project/FPGA-Guidelines


STE
Shaper
Detector Pulses /4
ADC16
ADC16
12
STE Event Sequencer
2
12
STE Energy LUT RAM 32k x 8
8
Incrementer
Thermostat
28V
Spacecraft
Survival Heater
STE Accumulator RAM 256 x 16 x 2
STE Accum. Readout
Temp Sensor
DAC6 /4
Thresholds
4*3
Test Pulse Generator
DAC16
8
DAC Sequencer
SWEA/STE DAC LUT 1344 Steps x 4 DAC x 16 x 2
LUT Loader
IDPU Serial Interface
IDPU
Bias Supply 200V
64k x 8 RAM
RAM Sequencer
Timing Generator
1MHz Serial Digital
SWEA
HV Controls
Analyzer
Deflector 1
Deflector 2
VO
MCP
DAC16
DAC16
DAC16
DAC16
DAC8
STE Monitor Rate Counters
Latches
Anode Pulses
16
Counters 16 x 16
Latches 16 x 16
Test Pulse Clock
Enables Latch
HV Enables
2
Monitors
7
9
Mux
ADC16
HKP Sequencer
FET Sw.
Operational Heater(s)
Cover Act.
28V for HVPS
2
Enable Plug
FET Sw.
+/-12, +/-5, +5, +2.5V
LVPS
28V
Spacecraft
Key:
Part of FPGA
On PWB with FPGA
Part of SSI not on PWB

2. SWEA Requirements

Reference 1 describes the interface between the SWEA/STE Interface and SWEA.

2.1. *Timing*

The DIF shall use the 1MHz clock provided on the IPDU interface (see reference 2) to generate the timing signals required for SWEA control.

The basic timing interval shall be 2 seconds, locked to the sample clock provided by the IDPU such that the 2-second interval starts on the 1-second tic decoded from the sample clock command, when the sample clock value is even. This signal shall be called CYCLECLK.

The 2-second interval shall be divided into 1344 1.45ms intervals, followed by a 51.2ms interval to make up the full 2 seconds. This signal shall be called STEPCLK.

A second clock shall be used to delineate SWEA counter accumulations. It shall tic every fourth STEPCLK, and shall be called SAMPLECLK. A counter incrementing each SAMPLECLK and reset by CYCLECLK shall be called the SAMPLECNT (0-335).

2.2. *Sweep Voltage Control*

The four SWEA sweeping voltages, ANAL, DEFL1, DEFL2, and V0, are controlled by the SIF via 16-bit DACs on the SWEA/STE Interface card. The SIF must automatically program these DACs every STEPCLK to generate the desired waveforms, repeating every 2 seconds, as described in reference 1.

The DACs are on a common 8-bit bus, and are programmed by putting the desired value onto the bus and then pulsing the write strobe for the DAC (two write cycles are required to write the 16-bit value). The DACs are double-buffered, and the DAC outputs are not changed until a common latch signal is pulsed, which should be a signal corresponding to the start of the next STEPCLK interval.

Not every DAC needs to be updated every step; typically only one DAC need to be updated per step, and the 8 LSB of some DAC registers may be set only once per CYCLECLK.

The DACs shall be programmed from a look-up table in the external RAM, which shall be programmable by the IDPU. This table shall be double-buffered to allow the IDPU to be loading one table while the other is being used to generate the sweep waveform. The SIF shall continue to use the same sweep table until the IDPU requests that the tables are swapped. This request shall be implemented at the next CYCLECLK.

The look-up table may either contain new values for all four DAC for each STEPCLK (4*2*1344 values = 10752 bytes), or may just contain a list of values to be changed, whichever is easier to implement.

2.3. *MCP DAC*

One more 8-bit DAC (actually implemented as a 16-bit DAC) is used to control the MCP voltage to SWEA. This requires a fixed value programmed by the IDPU via the serial interface. The DAC is on the same bus as the sweep voltage DACs, which implies an arbitration scheme between the automatic look-up table loading of the sweep DACs and the IDPU loading of the MCP DAC. The STE Test Pulser DAC is also on this bus, so its access must also be arbitrated (see 3.2 below).

2.4. *DAC Interface*

The 16-bit DACs (including the STE Pulser DAC) use the following interface signals:

MLBYTE	selects High/Low byte of the LTC1599 DAC
/DACCLR	active low (? power on) clear for DACs
/XXXXWR	active low write signal to input buffer of DAC
/XXXXLD	active low signal to transfer input buffer to output
DACDn	8-bit DAC data bus, n=0-7

where XXXX is one of six DACs

ANAL	Analyzer (main sweep)
DEFL1	Deflector 1 (ANAL is the reference input)
DEFL2	Deflector 2 (ANAL is the reference input)
VO	Bias Voltage
MCP	MCP Voltage
PULSE	STE Detector test pulse level

ANAL, DEFL1, DEFL2, and VO are swept synchronously according to the lookup table in the external ram. The MCP DAC is set according to an external command. PULSE sets the level of the STE test pulser and is ramped.

The DACs are all cleared to 0 with an active low /DACCLR signal. The input registers of the DACs are loaded according to MLBYTE signal with the /XXXXWR signals. For the 8-bit DACs (DEFL1, DEFL2, VO, and MCP), the LSB need only be loaded to 0s once. Activating the /XXXXLD signal transfers all 16 bits of the input latches to the output latch. The 16 bit DACs are loaded by activating /XXXXWR with MLBYTE low to load the least significant byte, and then with MLBYTE high to load the most significant byte. /XXXXLD then transfers the data to the output.

2.5. *High Voltage Enables*

The SIF shall provide signals that enable the MCP and NR supplies (MCPHVEBL and NRHVEBL). These signals shall be logic zero to turn the supply off, logic 1 to turn them on (power-on default = 0). They shall be programmed directly by the IDPU via the serial interface.

2.6. *Cover Actuator*

The Cover actuator FET switch shall be controlled by a logic level from the SIF, which shall be set by the IDPU via the serial interface. The cover status signal shall be included in the digital housekeeping.

2.7. *Operational Heater*

The operational heater FET switch shall be controlled by a logic level from the SIF. The heater shall be pulse-width modulated to provide one of 11 values of heater from always off (value=0) to always on (value=10). The PWM shall operate at 100KHz, with pulse width changing in 1us intervals (based on the 1MHz IDPU Interface clock). The PWM control (0-10) shall be provided by the IDPU over the serial interface.

2.8. *Test Pulser*

SIF shall generate a test pulser output used to stimulate the anodes directly for test purposes. The IDPU shall control if the test pulser is on of off. When off, the test pulser output shall be zero. When on, it shall generate a variable frequency pulse train, stepping in frequency each SAMPLECLK, and retuning to the start frequency each CYCLECLK. The test pulser frequency can be generated by the carry-out of a programmable down-counter loaded with the value of SAMPLECNT.

2.9. *Counters*

SWEA has 16 anodes connected to preamps that generate a logic pulse when an electron is detected. These 16 lines are directed to the SIF, where they clock 16 14-bit counters. These counters shall be latched and reset each SAMPLECLK. The latches shall then be read out to the IDPU, together with the SAMPLECNT value. An sweep waveform analog housekeeping measurement shall be appended to these messages as described in section 4.2 (on cycles when fixed housekeeping is being collected, the sweep housekeeping will not be appended, as indicated by a different message ID).

2.10. *SWEA Disable Mode*

An enable bit programmed by the IDPU via the serial interface shall control the SWEA logic in the SIF. For the STE-U, SWEA will always be disabled, while for SWEA/STE-D, it will typically be enabled, but may be disabled when SWEA is not used. The disable should stop the sweep waveforms, and stop reading out the SWEA counters. The remaining controls should remain active under IDPU control.

2.11. *SWEA HV Synchronization Signals*

SWEA requires high voltage synchronization signals. Two 100KHz square-wave signals with opposite polarity shall be generated by dividing the 1MHz clock by 10. These signals shall be routed to pins on the FPGA.

3. STE Requirements

The SWEA/STE interface includes Shapers and Pulse Height Analyzers for 4 STE detector channels. The SIF, together with the external memory, provides the digital part of that system.

3.1. *Timing*

The STE basic accumulation shall use the same 2-second CYCLECLK described in section 2.1.

A 10-second cycle shall be generated for use by the test pulser, which shall tic when the sample clock seconds provided over the serial interface, modulo 10, equals zero. This shall be called the TESTCYCLECLK.

3.2. *Threshold DACs*

Each of the 4 channels has a 6-bit threshold DAC. Each DAC is implemented as a R-2R ladder on the SWEA/STE Interface card, controlled directly by outputs from the SIF. The DAC values shall be programmed by the IDPU via the serial interface.

3.3. *Test Pulser*

The SWEA/STE Interface provides a programmable amplitude test pulser to STE. The amplitude is set by a 16-bit DAC controlled by the SIF, while the actual test pulse occurs when a logic pulse comes from the SIF. The logic pulse shall be negative going, lasting 10 microseconds, at a frequency of 10KHz (when enabled). The DAC value shall be incremented by one after each pulse, starting at zero at the TESTCYCLECLK tic. The ramp will continue for 65536 pulses until the DAC reaches the maximum value (after about 6.5 seconds). At that point the test pulses will be stopped and the DAC will be set back to zero until the next TESTCYCLECLK tic. The IDPU shall enable or disable the test pulser. When disabled, the logic pulse shall be set high.

3.4. *PHA*

The STE events are passed to an ADC that digitizes their amplitude into a 12-bit value (the 4 LSB of the 16-bit ADC are ignored). The front end circuit provides a number of logic signals to the SIF to allow it to determine when a valid event has occurred (see 3.4.1 for a discussion of the interface logic and timing requirements). The SIF then causes the ADC conversion to take place and reads out the converted value. All 4 ADCs are on a common bus, so the SIF must arbitrate events from each ADC into the accumulator sequencer in an unbiased way.

The events are then routed to a look-up table using the external RAM. The address shall be the 12-bit event energy from the ADC plus 2 bits identifying which detector generated the event. The 8-bit output of the LUT indicates which counter to increment (normally the LUT corresponds to 64 log-spaced energy bins for each of the 4 detectors, but other organizations are possible).

The SIF cycles the RAM to read the LUT and latches the result. This is used to increment one of 256 16-bit event counters in the external RAM. A read-modify-write cycle is used. 4 RAM cycles are required to increment the 16-bit value.

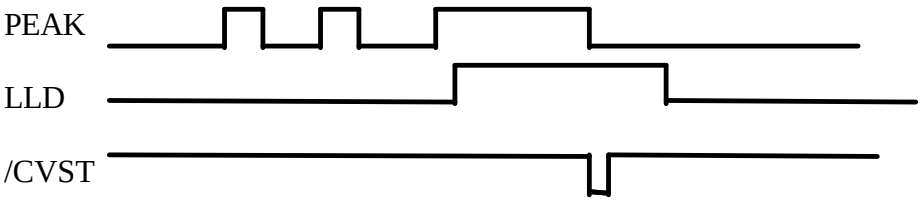
The array of 256 16-bit counters is double-buffered. While one set of accumulators is accumulating, the other shall be being read out via the serial interface to the IDPU and then reset.

3.4.1. PHA INTERFACE

Signals (one set per PHA):

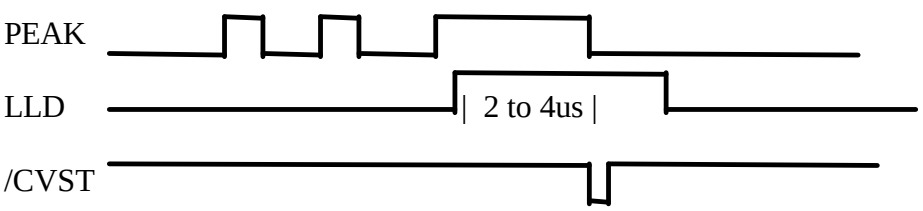
Signal	Description
/CVST	Start Conversion signal (active low) to A/D converter for Shaper
/PHARD	Read signal (active low) to put the PHA data from Shaper on PHA0-12
LLD	Low Level Discriminator - high when there is an active event on Shaper
ULD	Upper Level Discriminator - high when the signal on Shaper is too large
PEAK	Peak signal (active falling edge) for Shaper
PULSERESET	Pulse Reset - high when Preamp is resetting
BUSY	high when A/D converter is doing conversion

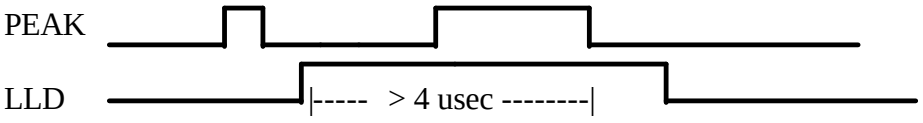
Start the A/D converter with /CVST when LLD is high, ULD is low, and PULSERESET is low, on the falling edge of PEAK signal.



The /CVST signal is active low and should be produced with a small time delay (< 100 ns) after the falling edge of the PEAK signal. It should be a narrow signal (> 5 ns and < 1000 ns). After /CVST goes low, BUSY goes high (delay < 15 ns), and remains high for approximately 2 us. At the end of this time the A/D converter should be read with an active low /PHARD signal. The A/D converter will put its data on the bus < 40 ns after activating /PHRD.

Additionally a digital pileup rejecter should be implemented as follows: only generate /CVST to start the A/D converter in the time window between 2 usec and 4 usec after the leading edge of the LLD signal. Sampling the LLD signal with the 1 MHz clock would be acceptable to implement this function.





/CVST remains high

One additional common signal resets all ADC (including the housekeeping ADC): A/DRESET. This signal is active high, and shall be set by IDPU command.

3.5. *Rate Counters*

Each of the 4 STE detector produces 3 event signals; LLD, ULD, and PULSERESET (the same signals used in the PHA interface described above). These events shall be routed to counters in the SIF (a total of 12 of them). The LLD counter max rate is 20,000 counts/second. The ULD max rate is 2,000 counts/second, while the reset max rate is 1,000 counts/second. These are nominally accumulated for CYCLECLK interval, latched at the end of the interval, and read out in a message to the IDPU. The number of bits per counter shall be 16, 12, and 11 respectively (packed into 3 16-bit words in the message to the IDPU). If a counter reaches its maximum value, it should stop there.

If necessary to save FPGA modules, these counters can be read out more often, and so need fewer bits of counter. For example, if they are read out 8 times a second, the counters need only be 12, 8, and 7 bits long respectively (saving 48 bits of counter and latch). To avoid overloading the message queue, a reasonable maximum readout rate would be 128Hz.

3.6. *STE Cover Actuators*

The STE has a reclosable cover. Two signals control the power to the cover actuators. In addition two status signals indicate the current position of the cover. A command from the IDPU over the serial interface shall request that the cover be opened or closed. Power to the appropriate actuator shall be supplied until the sense switch indicates that the cover is in the desired location; the power shall then be automatically turned off. If the IDPU sets the in or out request inactive, the actuator shall be immediately deactivated (this allows the IDPU to impose a timeout).

In addition to these controls, the IDPU shall have a “force on” control for each actuator independent of the switch state (in case the switch fails). This command shall be protected to avoid accidental setting since it will destroy the cover actuator if left on for more than a few seconds. Protection might consist of a 2-command sequence with a timeout on the interval between the commands of a second for example.

The STE cover state (both the position state and the actuator power) shall be included in the digital housekeeping.

4. Housekeeping

The SWEA/STE interface includes a 16-channel analog multiplexer followed by a 16-bit ADC. The SIF controls the select lines to the mutiplexer and the ADC conversion strobe and readout. The SIF system shall run in one of two modes, toggling between them every CYCLECLK interval.

4.1. *Cycling Housekeeping*

The SIF shall cycle through the 16 inputs and convert the data, cycling over all 16 values in one CYCLECLK interval. Each sample, together with its multiplexer address and some digital status information, shall be sent to the IDPU in a short message. The multiplexer should be switched to the next sample just after the previous conversion to allow the maximum settling time.

4.2. *Sweep Housekeeping*

The ADC shall be used to sample the sweep waveforms at SAMPLECLK rate. A fixed multiplexer address, set by the IDPU, shall be used for this measurement. The ADC shall be cycled every SAMPLECLK, and the resulting value shall be appended to the SWEA counter readout message for that SAMPLECLK interval. When in Sweep housekeeping mode, the housekeeping message shall continue to be sent to the IDPU 16 times per CYCLECLK, but the housekeeping MUX shall not cycle.

4.3. *Analog Housekeeping Interface*

Interface Signals:

HKPA0	LSB Housekeeping address - selects input to analog multiplexers
HKPA1	1st Housekeeping address - selects input to analog multiplexers
HKPA2	2nd Housekeeping address - selects input to analog multiplexers
HKPA3	MSB Housekeeping address - selects input to analog multiplexers
/HKPRD	Reads the data from the A/D converter (> 2 usec after /HKPCVST)
/HKPCVST	starts the housekeeping A/D conversion (5 ns < t < 1 us)

HKPA0-HKPAD3 should be set and then allow the analog signals to settle (> 10 - 20 usec) before activating the /HKPCVST signal. After 2 usec the data can be read on the PHAD0-PHAD11 lines.

4.4. *Digital Housekeeping*

Various digital status bits, including at a minimum those explicitly called out in this document, shall be accumulated and sent to the IDPU together with the analog housekeeping message.

5. Latchup Protection

The power interface provides protection for SEU events by monitoring the current of the +5V, -5V, and 5VD supplies. If excess current is drawn, AFESHDN becomes active high. The supplies are turned on by the AFEPWR signal being high (normal operating state).

AFEPWR shall be controlled by two signals provided by the IDPU over the serial interface; Force ON and Force Off. When neither of these signals is active, the AFEPWR signal shall stay in the same state unless AFESHDN becomes active, at which time AFEPWR should be set off.

While AFEPWR is OFF, all PHA and Analog Housekeeping interface signals should be set to zero.

The state of AFEPWR and AFESHDN shall be available to the IDPU as part of a digital housekeeping.

6. IDPU Serial Interface

The IDPU to SWEA/STE interface uses the Serial Instrument Interface described in reference 2. This interface provides timing, IDPU to Instrument commands, and Instrument to IDPU data.

6.1. *Timing*

The 1MHz clock provided on the serial interface shall be the primary clock for sequencers and clocks in the SIF. The interface also provides a 1-second tic and a sample clock time code to allow sampling to be synchronous to the rest of the IMPACT instruments. The SIF shall synchronize the accumulation clocks described in sections 2.1 and 3.1 to the sample clock provided.

6.2. *IDPU Commands*

The IDPU controls the SWEA/STE instruments via the command interface. The command interface consists of an 8-bit destination ID and a 16-bit data field. Static registers such as the MCP setting shall be allocated IDs. The look-up tables (LUT) shall be accessed via address pointer IDs and data write IDs (the SWEA sweep LUT and STE energy LUT shall have separate access systems so that the IDPU can treat them independently). Once the address has been loaded, it is automatically incremented each time data is written into the LUT. LUT Data is written 16 bits at a time (using two memory write cycles) to make best use of the command bandwidth. The LUTs are double-buffered so that one is being used by the instrument while the other is available to be loaded by the IDPU. The tables shall be switched by command from the IDPU, synchronized to the data collection cycle (CYCLECLK).

6.3. *Telemetry*

The SIF generates a number of kinds of telemetry that shall be passed to the IDPU over the serial interface, including SWEA data, STE data, and Housekeeping data. These data streams are generated automatically (once enabled) without handshaking. The SIF must arbitrate use of the telemetry channel amongst the data sources. Data shall be formatted into messages with unique identifiers for each data type as indicated in reference 1.

7. External Memory Sequencing

The external memory shall be a 512K by 8 UTMC SRAM. By utilizing both phases of the 1MHz clock, and perhaps some external RC timing components, the memory access

system in the SIF shall make one transfer in or out of the memory each cycle of the 1MHz clock. A sequencer in the SIF shall cycle through 8 fixed allocations each 8 microseconds. 5 cycles shall be allocated to the STE PHA to perform one LUT cycle and 2 read-modify-write cycles required to respond to an event. One cycle shall be allocated to the SWEA sweep LUT read-out, one to the STE accumulator read-out (and reset), and one to loading the LUT. Any cycle may be skipped if no transfer is required.