STEREO
IMPACT

IDPU Data Controller Board Specification

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Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2001-Apr-27	Preliminary Draft	-
B	2001-May-1	Add details on DMA transfer	-
C	2001-May-7	Add block diagrams & sequencer charts	-
D	2001-Jan-8	• Fix uP clock • Change Command system to a single channel using DMA • Fix memory map to use 64Kbyte Instruction Fetch page	

Distribution List

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1. Introduction

The IMPACT IDPU provides the interface between the STEREO Spacecraft C&DH system and the IMPACT and PLASTIC Instruments. It consists of a small box installed in the spacecraft that contains a low voltage power supply (LVPS), a MAG heater power supply, the MAG analog electronics board, a STE-D Interface board, and the Data Controller Board (DCB). This specification describes the DCB. See figure 1-1.

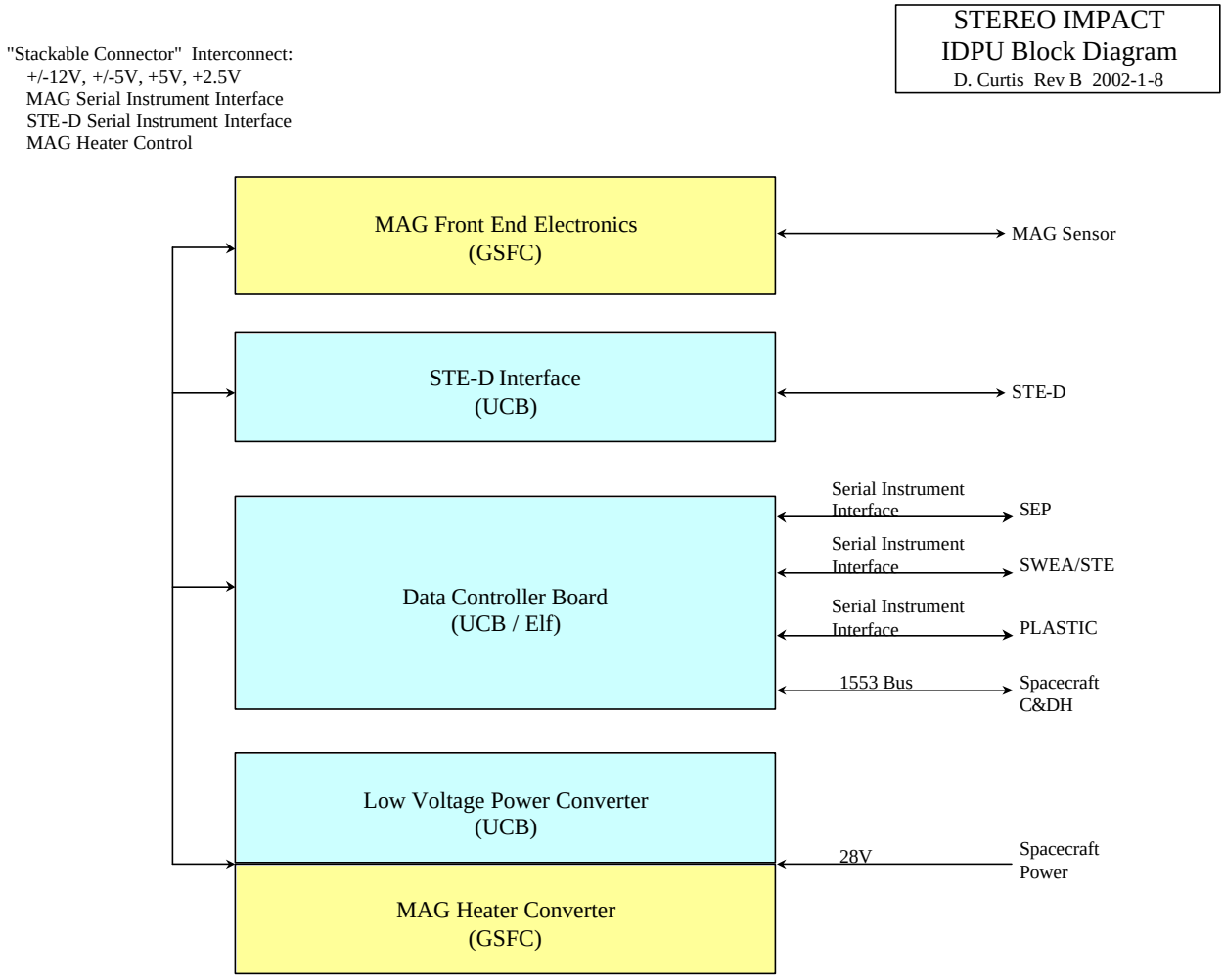

Figure 1-1 - IDPU Block Diagram

1.1. *DCB Description*

The DCB consists of a circuit board containing a microprocessor, memory, 1553 interface, and five serial instrument interfaces. The 1553 interface connects to the Spacecraft bus for commands and telemetry. The serial instrument interfaces connect the IDPU to the instrument suite (MAG, SEP, SWEA/STE-U, STE-D, and PLASTIC). The interface to MAG and STE-D are internal to the IDPU box; the rest of the instruments are remote. The DCB has connectors to each of the three remote instrument packages plus a

connector for the 1553 interface. Internal connectors route signals to the MAG board, STE-D board, and LVPS.

1.2. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by UCB and /or Elf indicating who is responsible for providing the data, and a unique reference number.

1.3. *Applicable Documents*

The following documents include drawings and STEREO Project policies, and are part of the Interface Requirements. In the event of a conflict between this ICD and the following documents, this ICD takes precedence. All ICD documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

1. IMPACT_revc_31_oct01 (IMPACT/Spacecraft ICD, on the APL web page)
2. ICD/Impact Serial Interface
3. ICD/IMPACT Harness
4. ICD/IDPUICD - IDPU ICD drawing
5. Phase A Report/C4-IDPU
6. Plans/PAIP (Performance Assurance Implementation Plan)
7. Project/FPGA-Guidelines

2. Mechanical

The mechanical configuration of IDPU is shown in the IMPACT/Spacecraft ICD (Reference 4). The IDPU consists of four trays. The DCB tray is a middle tray (MAG and STE-D Interface on top, LVPS on the bottom). The tray is 160mm x 200mm x 15mm. The dimensions of the DCB PWB including mounting locations and internal and external connector locations are shown in figure TBD-UCB-001. Note that the external connectors are mounted from the outside of the tray.

The internal connections shall be made via a stackable connector (see 5.5).

Parts dissipating more than 100mW should be mounted near the edge of the board so they can be thermally coupled to the tray.

3. Electrical Interfaces

3.1. *Low Voltage Power*

The UCB-provided Low Voltage Power Supply (LVPS) shall provide power to the DCB and MAG cards. The voltages to be provided and nominal currents are shown in table 3.1-1.

Table 3.1-1 DCB LVPS Requirements (TBR-Elf-003)

Voltage	Nominal Current	Max Current
+12.8	0	0
-12.8	0	0
+5V	0	0
-5V	0	0
+5D	220mA	
+2.5	80mA	

Max Current is the maximum expected current required over the operating conditions, including such things as high count rates and high voltage sweeping peaks. It does not include in-rush due to charging by-pass capacitors.

These supplies shall be regulated to +/-5% (including some variation in voltage with load). High frequency (supply-generated) ripple on the secondaries shall be less than 20mV peak to peak at Max Current.

The +/-12V supply is only used by the MAG board. The +/-5V is used by the STE-D board. The +5VD and +2.5V supplies provide power to the DCB as well as the MAG and STE-D boards. The 2.5V supply is used only by the FPGAs.

The power consumption estimates are:

- 1553 interface – 300mW on +5V (at nominal data rate)
- uP 220mW on +5V
- RAM 500mW on +5V
- FPGA 200mW, mostly on +2.5V
- Misc 80mW on +5V

3.2. *1553 Interface*

The spacecraft connects to the IDPU over a Mil Std 1553 interface. This interface shall be used to transfer commands, telemetry, status, and timing information between the spacecraft and IMPACT/PLASTIC. We also use this interface to exchange data with the SWAVES instrument periodically (using RT to RT transfers). The details of the exchange protocols for IMPACT are described in Reference 1.

3.3. *Instrument Serial Interfaces*

Each of the 5 instrument systems shall be connected to the IDPU over identical serial interfaces. This interface is described in Reference 2. It is used to control the

instruments and receive back telemetry and status information. It also provides a timing interface for data sampling.

4. Requirements

4.1. *Processor*

The DCB requires a data processing element to service the instrument and spacecraft interfaces, control the instruments, and collect, compress, and format instrument telemetry. The processing element needs sufficient capability to service the IMPACT and PLASTIC processing requirements. Note that the SEP instrument suite has its own processing system, so little extra is required of the IDPU for SEP. It has been estimated that a modest 16-bit processor with a fast multiplier can meet these needs.

4.2. *Memory*

The DCB processor requires a boot PROM (8 kbytes) plus EEPROM (256kbytes) for code and tables. This provides flexibility for reprogramming the processor while maintaining the reliability of the boot PROM in case of EEPROM corruption. The DCB also requires 3Mbytes of RAM, mostly for Burst telemetry storage, but also for data buffering, averaging, and formatting.

4.3. *1553 Interface*

There are a number of 1553 interface parts on the market that perform most of the protocol functions. This circuit shall transfer data directly in and out of a selected (programmable) part of the DCB RAM. Transformers are required to couple the data on and off the redundant 1553 bus.

4.4. *Instrument Serial Interfaces*

The serial interfaces shall be implemented in an FPGA. This circuit shall include a DMA system for directly transferring the data received into the DCB RAM. The system shall be capable of maintaining a continuous 1Mbps telemetry stream from each instrument without handshake or otherwise limiting the transfer. This will involve circular DMA buffers. The size of the buffers should be programmable, with options for 1kbytes, 2kbytes, 4kbytes, 8kbytes, 16kbytes, 32kbytes, 64kbytes, and 128kbytes. The locations of the buffers also need to be programmable, but can start on even boundaries (i.e. an Nkbyte buffer will start at an even multiple of Nkbytes to simplify addressing).

The system will keep track of the location of the start of the most recent complete block of telemetry for each interface. This pointer will jump forward each time a new block is received. A second pointer shall be programmable by the processor, and shall represent the start of the oldest block it has not yet processed. If the input pointer ever catches up with this output pointer, the system will flag a buffer over-run error.

Figure 4.4-1 shows a block diagram of the IDPU end of the Telemetry interface. Figures 4.4-2 and 4.4-3 show possible sequencer state machine charts.

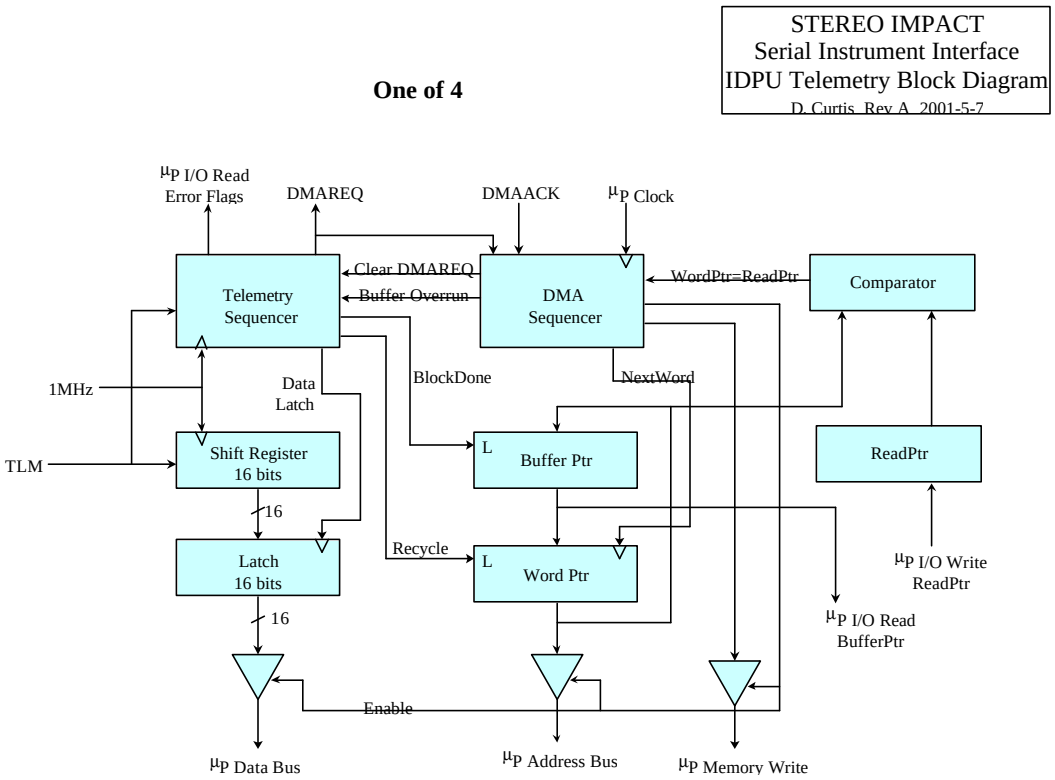

Figure 4.4-1 Serial Instrument Interface Telemetry System Block Diagram

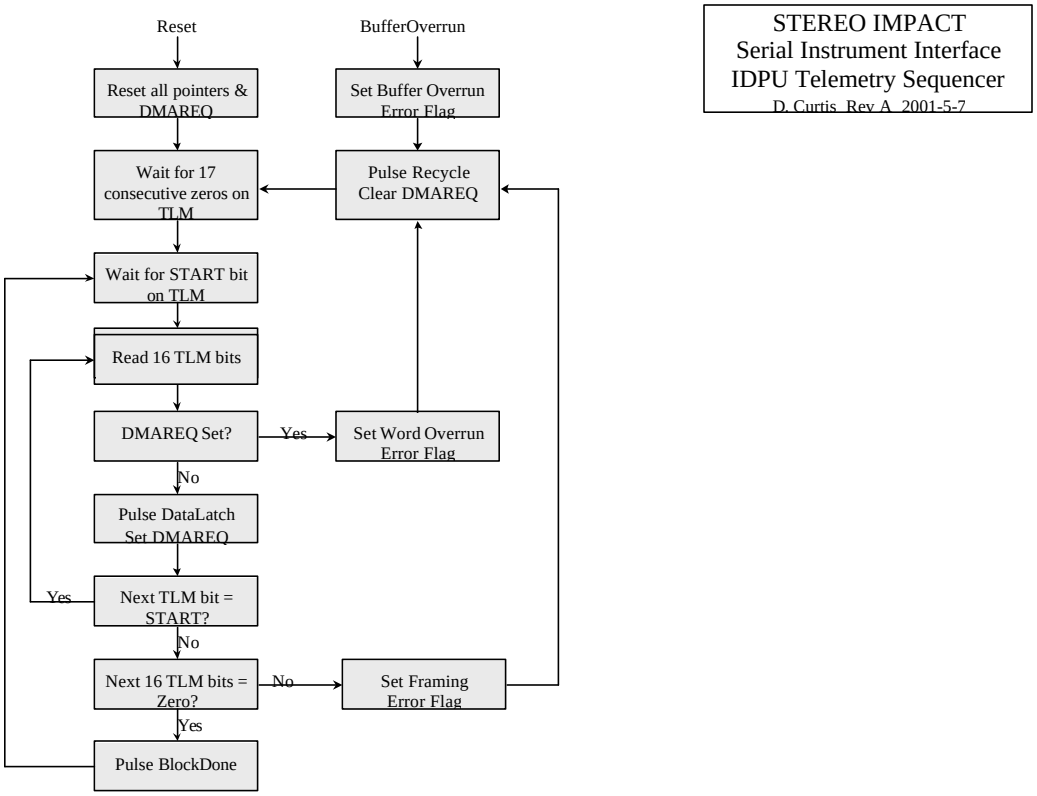

Figure 4.4-2 Serial Instrument Interface Telemetry Sequencer State Chart

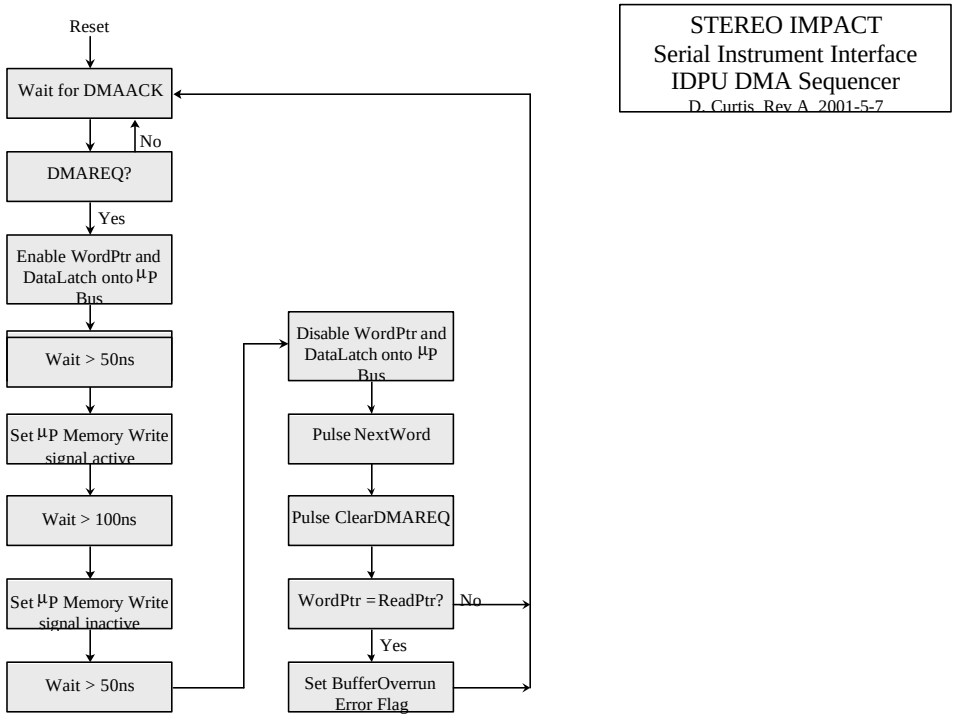

Figure 4.4-3 Serial Instrument Interface DMA Sequencer State Chart

A common command system with a steerable output system shall be used to send commands to the instruments. Note that the system needs to automatically send the time stamp command to all instruments, and to keep that time slot clear of other commanding by anticipating when that command will go out and not starting to send a command when a timing command is coming up soon. The command system shall be fed data words from a DMA buffer. Each entry shall be 32-bits, including an 8-bit prefix code indicating which subsystem is to get the command, followed by the 24-bit command word. The processor shall set up the buffer, set the buffer address, and start the DMA system working transferring commands. Commands shall continue to be sent until the prefix code indicates the end of the command list.

Figure 4.4-4 shows a block diagram of the IDPU end of the Command system. Figure 4.4-5 shows a state chart for the Command sequencer.

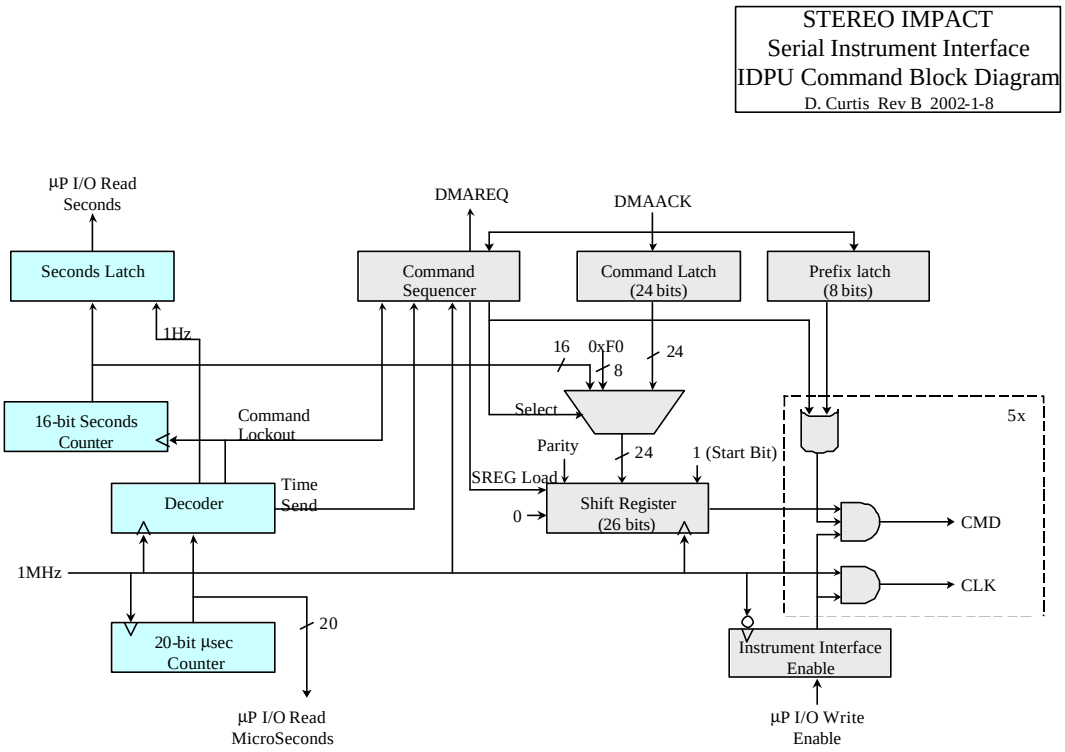

Figure 4.4-4 Serial Instrument Interface Command System Block Diagram

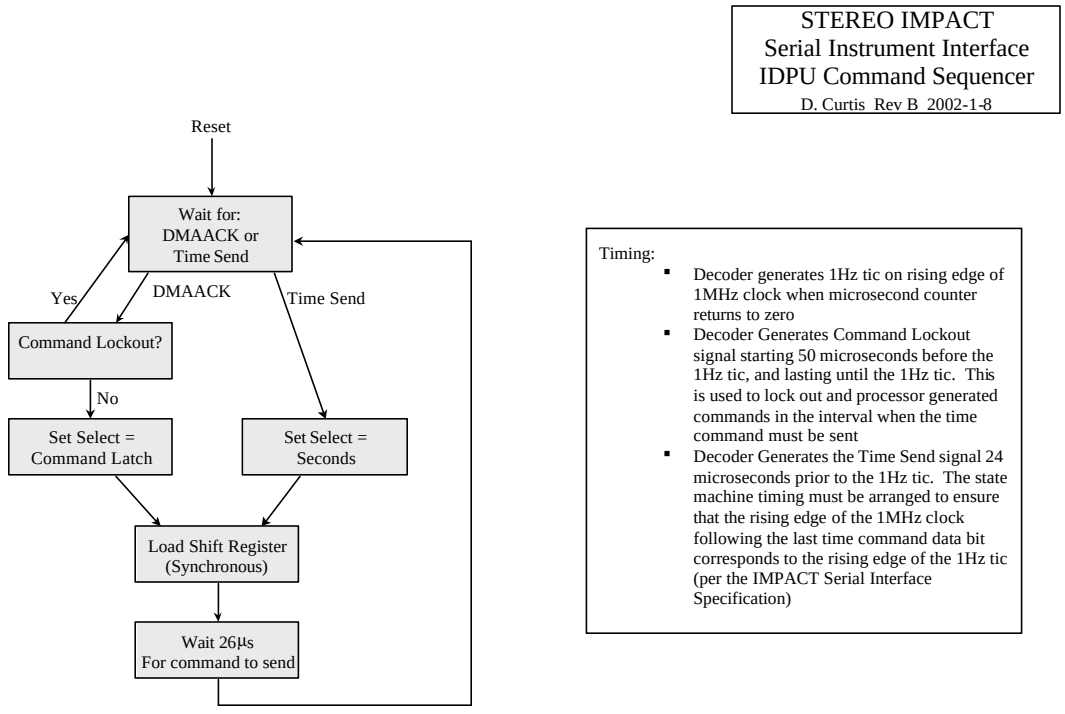

Figure 4.4-5 Serial Instrument Interface Command Sequencer State Chart

Each interface shall use a separate 54AC14 chip to buffer data in and out to minimize the risk of failure propagating from one system to another.

Pinouts for the connectors are given in reference 3.

4.5. *Glue Logic*

The FPGA shall also include memory decoding and paging logic, clock dividers, a programmable rate timer interrupt generator.

4.5.1. Memory Paging

The memory paging logic maps physical memory pages into the processor addressing space. The processor data memory shall be divided into 4 16kbyte segments. Each segment can be mapped into a different 16kbyte physical memory block. Instruction fetches anywhere in the 64Kbyte memory space shall be fetched from the memory pointed to by the first page register (the processor generates a signal indicating if a memory cycle is an instruction or data cycle).

The Boot PROM shall be either enabled or not (to save power). On reset the boot PROM shall be powered on and the first memory page pointer shall point to the boot PROM.

Any 16kbyte block of the EEPROM, RAM, or PROM shall be selected for any of the four processor memory segments.

4.5.2. Clock

A crystal oscillator shall provide the primary timing for the IDPU. This clock shall be divided down for various uses, including the 1553 chip, the processor clock, various state machines in the FPGA, the 1MHz serial clock (this is 1,000,000Hz), the 1Hz sampling pulse, etc. The FPGA shall maintain a 20-bit counter the processor can read of the 1MHz clock. This counter then generates the 1Hz synchronization tic that is broadcast to the serial instrument interfaces. The FPGA will also maintain a 16-bit seconds counter that shall be used for the time tic command over the instrument serial interface, and shall also be readable by the processor.

The FPGA will latch the contents of the 1MHz and 1Hz time counters at the time of the 1Hz timing command from the 1553 interface into a register readable by the processor. (Note that the 1553 time command will not be synchronized to the internal IMPACT clocks).

4.5.3. Interrupts

The FPGA shall pass on the 1553 interrupts to the processor. It will OR together any 1553 interrupts into a single processor interrupt input.

The FPGA will also generate a timing interrupt. This interrupt shall be synchronized to the 1Hz tic from the sampling clock. The interrupt interval shall be selectable as 256Hz, 128Hz, 64Hz, or 32Hz.

4.5.4. DMA

The FPGA shall implement a Direct Memory Access (DMA) system for transferring data in and out of the RAM from the 1553 and Serial Instrument Interfaces. This system will use the processor HOLD system to temporarily take control of the processor memory access bus (address, control, and data lines). The DMA system will then perform one or more transfers as required and then release the bus back to the processor. The UTMC 1553 chip contains logic to perform much of this task for the 1553 transfers. The FPGA must include this function for the Serial Instrument Interfaces, and arbitrate between the 1553 and 5 Serial Instrument Interfaces.

The Serial Instrument Interfaces each have a single DMA channel for data in; a single DMA channel is used for serial data out. Each DMA channel shall have a separate address pointer, as well as the block in and out pointers described in section 4.4. The DMA buffers shall be circular, continuously accepting data without re-initialization. In the event of a buffer over-run, the system will not over-write the data, but will stop transferring in new data. The data block currently being transferred in will be lost, and the input pointer will be sent back to then end of the previous block where it will stay until the start of the next block transfer in.

4.6. *Reliability*

Parts for the DCB need to meet Grade 2 requirements as called out in reference 6. In addition the must tolerate at least 8krads total dose and be Single Event Latchup (SEL) immune to an LET of 80 (or have suitable protection circuitry). Single Event Upset (SEU) sensitivity shall be low for control elements (< 1 upset per year), with a somewhat higher SEU rate permissible for data.

5. Implementation

The following sections describe the current thinking on the implementation of the DCB card. Figure 5-1 shows a block diagram of the DCB.

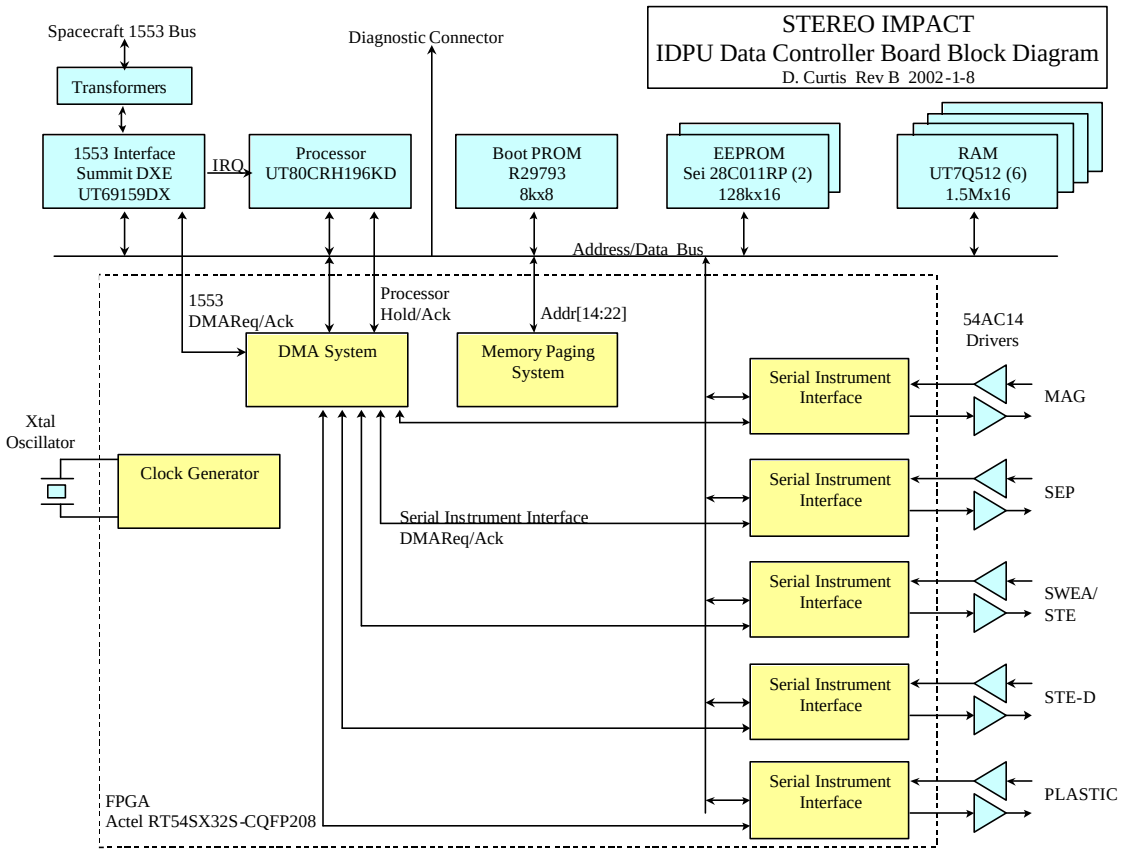

Figure 5-1 DCB Block Diagram

5.1. *Processor*

The UTMC UT80CRH196KD is the current candidate. It is a 16-bit microcontroller that shall be run at 8MHz. The processor has 1K on-chip RAM that can be used for variables and stack, so that the 3M external RAM can be used for tables and buffers. I have no plans to use the internal peripherals, though the RS232 serial interface might be good for diagnostics. I have purchased the development tools for this processor from Python. I also have an inverse assembler for my HP logic analyzer, but the pod is no longer made, so I will need to build my own. We will want to lay out a high density test connector on the DCB that brings out a bunch of processor and other signals for the logic analyzer. This need not be accessible when the IDPU is integrated, and may not even be loaded on the flight boards.

The reset vector goes to 2080H, so the PROM will need to be there at reset. I/O will also have to be memory mapped, probably somewhere just above the 1K RAM or just below 2000H. Whatever memory is enabled in the low memory segment will need to be masked to not respond when I/O is addressed.

5.2. *Memory*

5.2.1. ROM

We have enough of the Raytheon PROM we used on HESSI, but they are obsolete. Still they are my current choice. The processor can be designed to have a single 8-bit wide PROM while the rest of memory is 16-bits wide (processing is slowed down some, but that does not matter during boot). The PROM needs a power switch to turn it off when not in use, which would default to ON on reset.

5.2.2. EEPROM

My current candidate is the SEi 28C011RP 128Kx8 EEPROM. I would like to use two of these so we can choose to execute flight code out of EEPROM if we want.

5.2.3. RAM

My candidate for this is UTMC 7Q512 512Kx8 SRAM. We will need 6 of these to make 3Mbytes. I have some prototypes of these on order to test their power dissipation (the datasheet is not too clear on this point).

5.3. *1553 Interface*

We have selected the UTMC Summit UT69151DXE-WPC. This part includes the transceivers as well as a complete 1553 implementation and DMA memory access system, so it will transfer messages in and out of the DCB RAM. This is a complicated part and will take some work to understand how to use it. APL is providing a spacecraft emulator we can connect up to this for test. Transformers are available from Pulse Specialty Components. The 1553 part requires a 24MHz clock with something like 45-55% duty cycle. We can order a crystal oscillator meeting this requirement, or use a 48MHz oscillator and divide it by 2 (the former will save power, and is currently my baseline).

5.4. *FPGA*

A common FPGA has been selected for IMPACT. This is an Actel RT54SX32S-CQ208B. Prototyping can be done with the Actel A54SX32A-PQ208. This is an almost identical part in a plastic package with the same footprint as the flight part. It is somewhat faster. There is a socket that fits the prototyping part that solders to the PWB footprint, but it does not fit the flight parts. This part takes 2.5V, but has 5V I/O.

Project has some guidelines for FPGA design (reference 7). These recommend a fully synchronous design. The problem with that is power consumption. In order to keep power down, we will want a few different clocks for different purposes, and ripple counters are usually adequate. So take the guidelines as guidelines, not requirements. Keep track of which ones you violate and why.

5.5. *Stacking Connectors*

The plan is for the MAG analog, DCB, and LVPS to be connected via stacking connectors. This is a female connector with extra long pins running through the PWB to

mate with the next connector down. The current candidate part is a Hypertronics WTAX. This connector shall bring in low voltage power from the tray below and make the connections to the MAG board above. The MAG heater power supply controls shall also be routed through this connector. The pins for this connector only come in a limited selection of lengths which imposes some restrictions on the space between the MAG PWB and the DCB PWB.

5.6. *Layout*

Figure 5.6-1 is a preliminary layout of the DCB showing that the components fit pretty easily.

Figure 5.6-1 DCB Layout