STEREO
IMPACT

IDPU Simulator GSE
Hardware Specification

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Distribution List

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1. Introduction

This specification describes the hardware portion of the STEREO IMPACT IDPU Simulator GSE (ISG). The item is designed to simulate the communication interface between the IDPU and the instruments (MAG, SEP, PLASTIC, and SWEA/STE). It connects to a PC computer that is used to generate the commands and display the telemetry received over the interface. It may be configured to either simulate the IDPU or the Instrument side of the interface.

The Hardware part of the ISG shall be developed by Elf. The front-end software shall be developed by UCB. The science displays shall be developed by the instrument teams (since UCB will develop the science displays for SWEA/STE and MAG, this can be used as a starting point for the PLASTIC and SEP display software).

1.1. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by a code such as UCB indicating who is responsible for providing the data, and a unique reference number.

1.2. *Applicable Documents*

The following documents include drawings and STEREO Project policies. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

1. ICD/Impact Serial Boom Interface
2. ICD/Impact Harness Spec
3. IEEE-1284 Parallel Port Standard (not on the web site)
4. Project/FPGA Guidelines

2. Requirements

2.1. *Instrument/IDPU Interface*

The ISG must simulate the serial interface protocol described in reference 1. It should interface via a connector style and pin-out as called out in Reference 2 for IDPU-J3 and for IDPU-P3.

The system should operate in two modes: IDPU Simulation and Instrument Simulation (but only one mode at a time). It shall have two connectors corresponding to these different modes as mentioned above, marked "IDPU" (IDPU-J3) and "Instrument" (IDPU-P3). It should also have LEDs indicating activity on each of the three signals in each direction.

The mode of the ISG shall be set by the PC, and indicated by an LED on the ISG.

2.1.1. IDPU Simulation

In this mode the ISG simulates the IDPU for testing an instrument. The instrument will be connected to the connector marked "IDPU". In this mode, the ISG must have a mode bit that disables the outputs (sets the signal level on the harness to zero) on command by the PC.

2.1.1.1 Commands

The system should formulate information provided by the ISG PC into commands, and also automatically generate the timing commands. The system must anticipate when timing commands are about to be sent and delay sending PC generated commands if they will conflict with the time when the timing command must be sent.

Commands are 3 bytes long. The system must be designed to avoid loss of synchronization between the data from the PC and serial commands that would cause the bytes intended for one command to get out split between commands.

The ISG shall maintain a queue of commands to be sent, at least 200 commands deep. The PC shall be able to determine the status of the queue.

The ISG shall maintain a local counter to generate timing commands. This counter shall be settable via the PC interface. An LED shall flash once a second when the timing command is sent.

2.1.1.2 Telemetry

Telemetry blocks from the instrument must be collected and passed to the ISG PC. The ISG shall maintain a counter of the number of bytes of full telemetry blocks it has collected (excluding any bytes from partial blocks it might be currently collecting). As the PC reads out bytes from the ISG, this counter is decremented. When a full new block has been collected, its size is added to this count. The PC shall have a way of reading this counter so it can determine how many bytes to read.

The ISG shall keep track of errors on the telemetry interface, including Framing Errors (missing start bit not followed by 16 zeros, and so not the end of packet), and Packet Size Errors (packet length as determined by the header does not match the length as determined by the end of packet, 17 zeros). An LED shall indicate such errors, and this information shall be readable and resetable via the PC interface. When such an error occurs, the telemetry block shall be dropped and the system will ignore further data until a new block is found (as indicated by at least 17 bits of zero).

2.1.2. Instrument Simulation

In this mode, the ISG simulates an instrument for testing the IDPU. The IDPU will be connected to the connector market "Instrument".

2.1.2.1 Commands

Commands from the IDPU shall be collected by the ISG and passed on to the ISG PC. The counter system and a similar error tracking as outlined in 2.1.1.2 shall be used in this

mode for commands. Timing commands shall be passed through like other commands, but an LED shall flash when it is received.

2.1.2.2 Telemetry

The PC shall provide blocks of telemetry to the ISG. When a full telemetry packet has been provided, the ISG shall start to transfer it out the interface to the IDPU. The PC shall tell the ISG when it has a full block, and shall be able to poll a status bit to determine when the transfer is complete. The ISG shall only have to deal with one block at a time; the PC will not start to transfer in a new block until the previous block transfer is complete.

2.2. *Computer Interface*

The ISG shall interface to the ISG PC via the standard printer port. A standard 25-pin male D connector with the standard printer port pinout shall be used on the ISG so that a simple 1-1 cable can be used to connect the ISG to the ISG PC.

The ISG PC shall use the IEEE-1284 EPP port mode of the printer port so that data can be transferred (preferably using DMA) into and out of the ISG PC. This implies certain connections and timing conventions be used for this interface as called out in reference 3. LEDs indicating activity on this interface shall be included.

The system shall be designed to allow daisy chaining of multiple ISGs on a single printer port, as allowed by the IEEE-1284 standard. This requires a 25-pin Female D connector, and possibly some address switches (TBD-UCB-001).

To mitigate computer latency issues, FIFOs shall be implemented between the IDPU interface and the computer interface (one in each direction). These FIFOs shall be sufficiently large to accommodate at least 200ms latency. The FIFOs may either be chip FIFOs or else SRAM configured as a FIFO in the interface logic (FPGA). LEDs shall indicate the status of the FIFOs (one each for Empty and Full).

2.3. *Packaging*

The ISG shall be housed in a small aluminum box. It shall include its own power converter so that it can be plugged into a standard 110VAC wall plug. It shall have the IDPU and Instrument connectors, as well as the indicator LEDs, mounted on the front face, and the PC connectors (in and out) mounted on the opposite face together with the power cord. The top surface shall remain blank. Inside this box shall be mounted the power converter plus a small PWB on which the FPGA and drivers are installed.

2.4. *FPGA Recommendations*

Reference 4 includes guidelines for the development of FPGAs. Places where the detailed design recommendations in the Methodology/Design Approach section of the guidelines will not be met should be documented and provided to UCB (Dave Curtis).