STEREO IMPACT 1553 Software
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1. Implementation

Per IMPACT ICD

1. 1553B Standard (not A)
2. IMPACT RT Address = 17
3. No broadcast commands
4. TBD Mode Codes (at least “Synch with Data”)
5. Loopback

Design Decisions:

1. No Buffer Mode (improve worst case DMA timing margins)
2. Ping-Pong buffer mode
   2.1. Some or all of the sub-addresses may use a single buffer, based on >10ms between accesses.
3. No Interrupt Log (use A/B buffer bit in the Descriptor Block to determine what subaddress was accessed)
4. Interrupt on message transfer (last sub-address for multi-block messages like Telemetry)
5. Interrupt on error

2. Hardware

UTMC Summit DXE chip
RTA = 17 per IMPACT ICD
RTPTY = 1 (odd parity)
MSEL = 01 (RT)
A/-B = 0 (1553B)
-LOCK = 0, fixed address & mode.
-AUTOEN = 1, no auto init. (?)
80C196KD Processor
Custom FPGA DMA system

3. Initialization

1. Wait for not busy (TERACT: reg.1&1 = 0), with 10us timeout
2. Stop Execution (STEX: set reg.0 = 0)
3. Reset hardware (SRST: set reg.0 = 0x2000)
4. Wait 5us
5. Do BIT (SBIT: set reg.0 = 0x4000)
6. Wait for BIT Complete (READY: reg.1 & 2), timeout 1ms
7. If timeout of BIT Fail (BITF: reg.6 & 0x1000), flag error; continue
8. Set 1553 address page into memory paging system in FPGA
9. Initialize Descriptor Block

9.1. Setup for ping-pong mode
9.2. Most can use the same buffer for both halves (single buffer mode) because the interrupt routine will transfer the data before another 1553 transfer can occur
9.3. Set unused buffer pointers to the bit bucket.
9.4. Loopback Read buffer should be the same as the Loopback Write buffer
9.5. Interrupt When Accessed (Receive Control Word in Descriptor Block, IWA) on:
9.5.1. Time / Spacecraft Status (Rx.1)
9.5.2. Command Block (Rx.3)
9.5.3. SWAVES RT-RT (Rx.29)
9.5.4. Instrument Status (Tx.1)
9.5.5. Last Telemetry Buffer (Tx.7)
9.5.6. SWAVES RT-RT (Tx.29)
9.5.7. Synch with Data Mode Code (MC Rx.17)

10. Initialize registers:
10.1. Interrupt Mask: Enable interrupts DMAF, WRAPF, TAPF, BITF, MERR, SUBAD, ILLCMD. (set Reg.3 = 0xFC80)
10.2. Interrupt Log : Log is disabled: (set Reg.5 = bit bucket)
10.3. BIT Word Register: Clear user bits (Reg.6 = 0)
10.4. Descriptor Pointer Register: (reg.8 = Pointer to Descriptor Table)
10.5. Status Word Bits: Clear bits (Reg.9 = 0x80000)
10.6. Illegalization Registers: Enable sub-addresses per ICD: Rx: 1,3,29,30,31: Tx: 1,2,3,4,5,6,7,29,30,31, Brd Rx: None, Brd Tx: None, Mode Rx: TBD, Mode Tx: TBD, Mode Brd Rx: None, Mode Brd Tx: None (Reg.16 = 0x000A, Reg.17 = 0xE000, Reg.18 = 0x00FE, Reg.19 = 0xE000, Reg.20 = 0, Reg.21= 0, Reg.22 = 0, Reg.23 = 0, Reg.24 = TBD, Reg.25 = TBD, Reg.26 = TBD, Reg.27 = TBD, Reg.28 = 0, Reg.29 = 0, Reg.30 = 0, Reg.31 = 0)
10.7. Control Register: STEX=1, SBIT=0, SRST=0, CHAEN=1, CHBEN=1, ETCE=0, BUFR=0, BCEN=0, DYNBC=0, PPEN=1, INTEN=0, XMTSW=0 (reg.0 = 0x9804) - Starts up system

4. 1553 Interrupts (Errors or Messages)

First read Pending Interrupt Register to determine what is happening (Reg.4). Read another register (Reg.3) to clear the Interrupt Pending Register.

4.1. *Error Conditions*

For error interrupts (DMAF, WRAPF, TAPF, BITF, MERR, ILLCMD), there is not too much that can be done. Report the error in the housekeeping. If the problem is fatal, the timeout function will attempt a reset.

If no 1553 interrupts occur in a set time interval (several seconds), attempt to reset the 1553 interface. If that fails, try resetting the processor (via the watchdog).

4.2. ***Messages***

For SUBAD interrupts, find which sub-addresses or modes have been accessed. This is done by polling the Ping-pong A/B bit in each Message Descriptor Blocks Control Word.

Verify the Information Word (first word in buffer) contents: Correct message length in WC and RT-RT type for this sub-address, no error (ME, ILL, TO, OVR, PRTY, MAN)

- If bad, log error, ignore receive data, act on transmit

4.2.1. Time / Spacecraft Status (Rx Sub-address 1)

Send the status data to the decoder task
Save the time code for the "synch with data" mode code

4.2.2. Command Receive (Rx Sub-address 3)

Send data to the command receiver task

4.2.3. SWAVES Data (Rx Sub-address 29)

Send the data to the Burst Trigger task

4.2.4. Synch With Data (Rx Mode 17)

Update time received from Time / Spacecraft Status with offset. Poke into UTC time register. (Error if Time not received since last Synch with Data)

4.2.5. Instrument Status (Tx Sub-address 1)

Update Instrument Status field.

4.2.6. Last Telemetry Block (Tx Sub-address 3)

If there is another telemetry packet available, copy into the buffer and increment the Data Available Counter. Otherwise wait for next time.

4.2.7. SWAVES RT-RT (Tx Sub-address 29)

Get data for SWAVES from Burst Trigger Task & copy into buffer.