IMPACT Subsystem Milestones SEP Cen - SEP Central Data Processing Unit

Page 1 of 3 Status as of:8/31/03

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									2003								2004								
ITEM	EVENT	N	D	Į,	J F	·	/ A	М	J	J	J	A S	6 (O N	1 [) J	F	М	Α	M	J	J	Α	s	0
1	EM Logic Board Fabricated				3/19	9																			
2	EM Analog/Post-reg Board Fabricated				3/2	28	V																		
3	EM Solid State Detector Bias Supply Board Fabricated				4	1/2 	V																		
4	B1 Flight Software Available					4/8 		7																	
5	EM Analog/Post-reg Board Assembled				4	1/11 	1	4/	/14																
6	EM Logic Board Assembled					4/14	1		5.	/13															
7	ETU LVPS Received						5/5	V	7					9/1 L	Jp	dat	ed	fo	r S	ер	ten	nbe	r		
8	EM Logic Board Tested						5/5		5/	8															
9	ETU LVPS Tested						5/14		7			-	\Diamond	9/26	6										
10	FM 1 SEP Central Common Enclosure Fabricated						5/2	2	7				$\overline{+}$		10/2	23									
11	FM 2 SEP Central Common Enclosure Fabricated						5/2	2	7				+		10/2	23									
12	EM Analog/Post-reg Board Tested						5/2	28			6/2	4													
13	EM Solid State Detector Bias Supply Board Tested						5/2	28	7		1	8/	/11												
14	EM Boards Available for EM I & T						5/2	29		6/	9														
15	FM 1 SEP Central Common Electronics Enclosure				T		5/3	30	V	7			+		10/	30									
	∇ On Time ∇ Co	om	ple	te	d C)n	Tim	ie		·				1				Mis	ssic	on	Crit	ica	ΙM	s	
	Possibly Early C	om	ple	te	ed Early												IMPACT Critical MS								
	Possibly Late Completed Late										Suite MS														

IMPACT Subsystem Milestones SEP Cen - SEP Central Data Processing Unit

Page 2 of 3 Status as of:8/31/03

Page 2 of 3						Status as 01:8/31/03														_					
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ITEM	EVENT	N D	J	F	M	1 A	\ N	1 J	J	Α	١ (s	0	N	D	J	F	М	Α	М	J	J	Α	s	0
16	FM 2 SEP Central Common Electronics Encloure Assembled					5/3	30	$\sqrt{}$					\leq	> 1	0/30	ı									
17	B2 Flight Software Available							7/3 (7/7	7														
18	Flight Logic Boards Fabricated							7/2 	\ 8 	Ż	+	$\langle \langle $	> 9/2	25											
19	Flight Logic Boards Assembled									9/17 	7	\) 10 	/23										
20	Flight Analog/Post-reg Boards Fabricated									9/17	7 \	V	9/2	23											
21	Flight Solid State Detector Bias Supply Boards Fabricated									9/2	29	$\overline{\ \ }$	7	\dashv	\Diamond	12/1	12								
22	Flight Analog/Post-reg Board Assembled									10	0/2	\bigwedge	\angle	> 1	0/30										
23	FM 1 LVPS Received									10	0/13	3 \	A		\prec	>	1/9								
24	Flight Logic Boards Tested										10/	'28 	\bigvee		11/	18									
25	Flight Analog/Post-reg Boards Tested											11 	/25		7 11	1/26									
26	Flight Solid State Detector Bias Supply Boards Tested												12/9	9 \	/) 1/2 	21							
27	FM 1 LVPS Tested												12/1	1	$\sqrt{}$		>1	/30							
28	FM 1 Ready for I & T												12/1	2	7		>2	2/2							
29	FM 2 LVPS Received												12/	17	$\sqrt{}$		\prec	\supset	3/9						
30	B3 Flight Software Available W/User Manual											11.	/24			12/	18								
	\bigvee On Time	omple	tec	d C)n 7	Γim	ne										Ν	⁄lis:	sio	n C	riti	cal	MS	3	
	Possibly Early	omple	tec	ΗE	arl	у											II	ИP.	AC	CT (Cri	tica	l M	S	
	○ Possibly Late ○ Column ○ Colum	omple	tec	l L	ate)											S	uit	e N	ИS					

IMPACT Subsystem Milestones SEP Cen - SEP Central Data Processing Unit

Page 3 of 3 Status as of:8/31/03

				2003 2004																				
ITEM	EVENT	N	D	J	F	М	Α	М	J	J	Α	s	0	N	D	J	F	М			J	Α	s	0
31	FM 2 Ready for I & T													1.	/2				3/2	26				
32	FM 2 LVPS Tested													1.	/2	\mathbb{Z}		\leq	3/2	26				
33	Final Flight Software Available												1	12/3	ģδ	$\sqrt{}$	1/7							
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	√ On Time	Comp	olet	ed	On	Ti	me)									Ν	/lis	sior	Cri	Critical MS	S		
	Possibly Early	Comp	Completed Early										IMPACT Critical MS											
	Possibly Late	Comp	olet	eted Late								Suite MS												