



Pin	Signal
1	TOF Bit 9 (MSB)
2	TOF Bit 8
3	TOF Bit 7
4	TOF Bit 6
5	TOF Bit 5
6	TOF Bit 4
7	TOF Bit 3
8	TOF Bit 2
9	TOF Bit 1
10	TOF Bit 0 (LSB)
11	TREND?
12	USR
13	STARTR
14	STOPR
15	+12V
16	+5V
17	+3.3V
18	ROUND
19	-5V
20	-5V
21	CALGATE
22	CHLCLK
23	CHLDATA
24	spare
25	spare

TOF0-9 Parallel TOF output data

TRENDV A 5v logic signal going high when TOF0-9 are valid. May not be necessary. If can get timing from USR.

USR A 5v logic pulse indicating a STOP signal has occurred within 60ms after a START signal. Might also indicate TOF data valid. Width 0.5-1us

STARTR A 5v logic pulse indicating that the START discriminator has fired. Width 0.5-1us.

STOPR A 5v logic pulse indicating that the STOP discriminator has fired. Width 0.5-1us.

CALGATE CALCLK CHLDATA ] A 5V 3-wire serial interface for calibrating the TOF. Details TBD

**SIT TOF BOARD**

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## INPUT SIGNALS

START, STOP      Capacitively coupled to MCP collection anode at HV  
START rate      Signal rate during 10mV-1V with peaking time of 1.5-2ns and <10% ringing  
STOP rate      0-100kHz  
TOF rate      0-50kHz  
TOF - 1-2 to 60 ns

TEST CONNECTOR      Signals from pulse generator. Negative going, 0.1V Rate 1kHz

## POWER

Voltage	Current	Regulation	Power
+12	3.5mA	5%	40mW
+5	40mA	5%	200mW
+3.3	30mA	5%	100mW
-5	2mA	5%	10mW
			350mW TOTAL

## SIZE

Single board, < 13cm x < 13cm      Mounting TBD (5 mounting holes?)

## MASS

100g      total including conformal coat and connectors  
excluding mounting hardware

## OPERATION

System is free-running. A START signal begins measurement of time-of-flight. In all, a voltage within 60 ns of a STOP, a TRIG stop pulse is generated and the digitized TOF is output in 100ns bins. If there is a TRIG stop pulse, the system clears itself in 100ns and is ready for the next START. If there is no valid stop, the system clears itself in TBD ns ready for the next START. I assume that the data is buffered internally and remains valid until the next valid stop.  
Calibration cycles: ?

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