IMPACT TEAM MEETING

5/ 10-11 /00

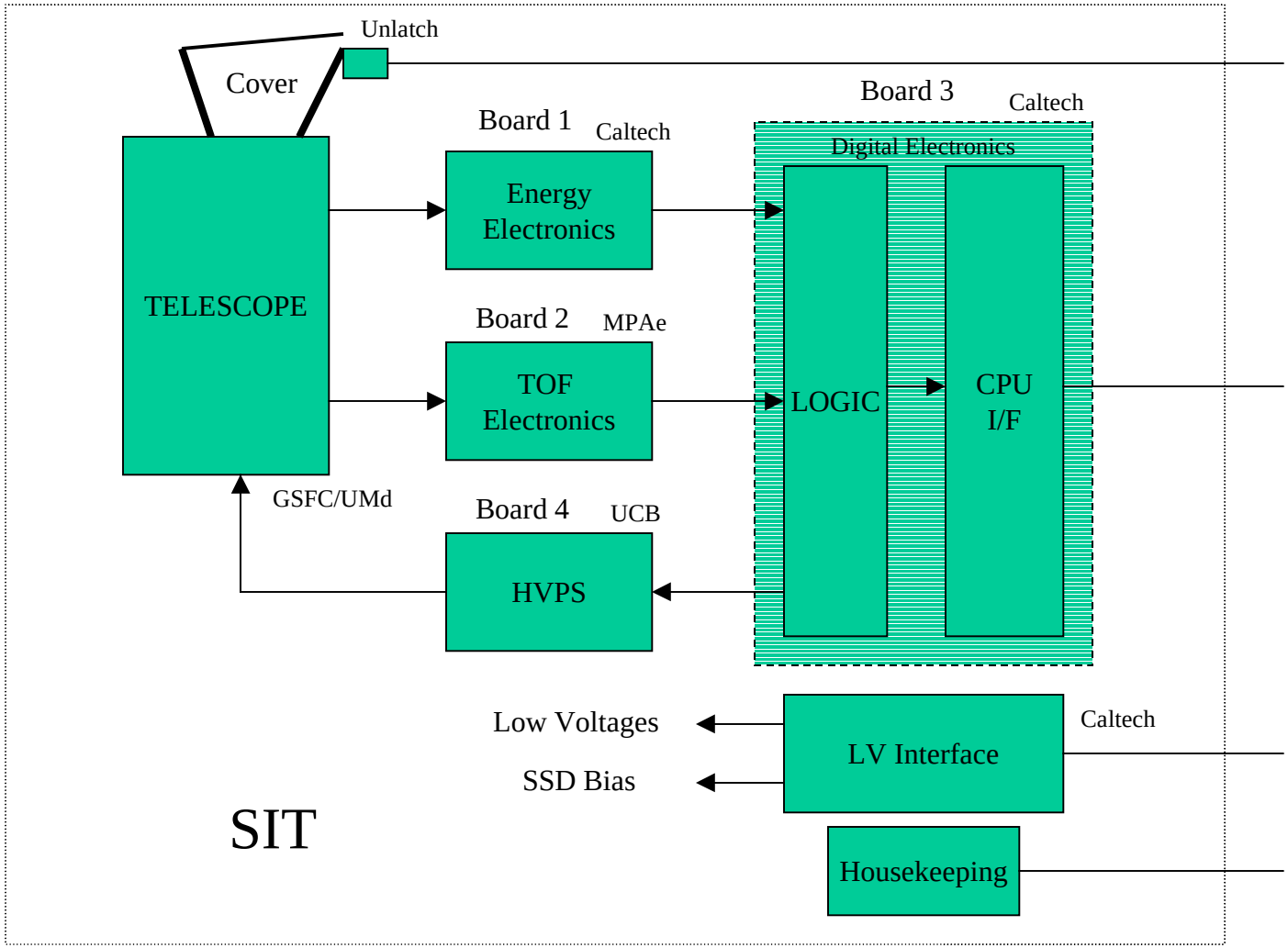
SUPRATHERMAL ION TELESCOPE

SIT STATUS

SIT Development

- SIT consists of:
  - a telescope with sunshade and acoustic cover, a foil, SSD and MCPs
  - Energy, Time-of-Flight, Logic electronics, and a HVPS
  - an interconnecting harness
  - Structures to shield and support the above
- The SIT development concept is that:
  - GSFC will design, build and assemble the telescope based in part on existing UMd designs and parts
  - Caltech will design and build the energy and logic electronics based on UMd inputs
  - Caltech will provide the harness as part of the SEP harness, with inputs from UMd
  - MPAe will supply the time-of-flight electronics board
  - UCB will supply the HVPS
  - SIT will be housed in a common box as part of SEP which is being built by GSFC and Caltech
  - UMd will assemble SIT and provide SIT-level testing and calibration including SIT-level GSE
  - UMd will provide limited support of the integration of SIT into SEP and STEREO
  - It is assumed that most environmental testing will be done at the SEP level

SIT BLOCK DIAGRAM



SIT Status - Telescope

- Box and Internal Parts
  - Unit #1 - use WIND/STEP spares from UMd
  - Unit #2 - use spares as available plus build additional parts using existing designs
- Sunshade/Acoustic Cover
  - Design may be based on WIND/STEP
- Sensor Elements
  - Foils - use WIND/STEP spares as available
  - SSD - new flight SSDs to be procured by UMd
  - MCPs - new flight MCPs to be procured by UMd

SIT Status - Electronics

- Energy Electronics (Board 1)
  - CSA - Design available and submitted to Caltech
  - 2-ramp amplifier/HTC - concept design with Caltech chip
  - Control Logic - TBD
- TOF (Board 2)
  - Requirements submitted to MPAe
  - Digital Design - MPAe will modify existing MPAe design
  - Fast amplifier - is existing design available?
  - Discriminators - is a CFD required?

SIT Status - Electronics (cont.)

- Digital Electronics (Board 3)
  - Instrument Logic - Conceptual design begun at UMd
  - CPU I/F - interface definition needed
    - Event data - 24 bits/event (?), serial interface, asynchronous, 1000 events/sec (?)
    - Discriminator rates (6) - accumulated in ACTELs, 24 bits(?), serial I/F, read out periodically
    - Commands - infrequent commands to set HV level and operating state of SIT. Calibration service of TOF board (once/second).
    - Analog Housekeeping - 2 thermistors and a 0-5v HV monitor
- HVPS (Board 4)
  - Preliminary requirements submitted to UCB
  - Power and mass?, Use voltage divider or tap multiplier? Switch power or rely on inhibits for safety?

SIT Status (cont.)

- Miscellaneous
  - Need to define SSD bias requirement with Caltech
  - Need to define LV interface - filters, regulators
  - Assume Caltech will build what is required for SIT
  - Housekeeping - currently 2 thermistors and an HV monitor signal from the HVPS
- Harness
  - assume part of SEP harness provided by Caltech
- Structure
  - SIT will be integrated part of the SEP box

SIT Status - Open Items

- Telescope
  - Thermal design, acoustic cover, UMd inventory, procure detectors
- Energy Electronics: Caltech hybrid/VLSI circuit definition
- TOF : Design of fast amps, and are discriminators necessary?
- HVPS: Power/mass/size?, voltage divider or taps from multiplier?, switch power or rely on inhibit and level commands for safety?
- Digital Electronics: Define CPU interface
- Other: LVPS filtering? Detector bias filtering?
- Testing: Simple DPU simulator needed from Caltech

SIT Description - Integration/Test

- **General**
  - Our preference is that SIT electronic boards and telescope be separate enough from the rest of SEP that SIT can be assembled onto a test fixture and tested as a unit prior to integration with the rest of SEP.
- **Test Flow** - Proposed test flow:
    - Build and test individual SIT subsystems (various locations)
    - Assemble SIT on test fixture (UMd)
    - Functional test of SIT (UMd)
      - Bench tests with pulsers and test equipment
      - Vacuum tests with alpha particles
      - Characterization of performance with temperature?
      - Bench Calibration
    - Accelerator calibration
    - Deliver SIT to SEP, Integration & Instrument-level Test(SEP)

SIT - Changes Since Proposal

- Telescope: none
- Energy Electronics: mass increase of 87g due to oversight, power increase of 33mW from reassigning voltage lines and local regulator
- TOF : 6x8 cm board size from early MPAe e-mail seems small to UMd, small increase in power from reassigning voltage lines (18mW)
- HVPS:
  - Proposed power was 100mW. Per conversation with Peter Berg in Mar 00 estimated power has risen to 160 mW
  - we have added a DAC to digital electronics to provide HV control (proposal assumed digital control)

SUMMARY:

- Power - increase of 111mW (= 33+60+18)
- Mass - increase of 87 grams (energy electronics)
- Bit Rate - no change (60bits/sec)

SIT - Resources

	MASS (g)		POWER (mW)	
Subsystem	**Proposal**	**Current**	**Proposal**	**Current**
Telescope	483	483	0	0
Energy Electronics	0	87	50	83
Time-of-Flight	100	100	350	365
Digital Electronics	60	60	50	53
HVPS	100	100	100	160
Housekeeping	0	0	0	0
Test Connector	10	10	0	0
Wiring	30	30	0	0
TOTAL	**783**	**870**	**550**	**661**
Delta		**87**		**111**

SIT - Electronics Board Area

Board	Proposal	Current
Energy Electronics	Included per Sandy Schuman with Caltech estimate	17 x 6 cm
TOF electronics	6 x 8 cm per MPAe e-mail	6 x 8 cm (1)
Digital Electronics	10 x 7 cm	10 x 7 cm
HVPS	11 x 7 cm	11 x 7 cm
Miscellaneous	0	tbd (filters?)

Notes 1. Not sure if includes amplifiers, discriminators

SIT - Upcoming Tasks

- Inventory WIND/STEP Telescope parts
- Support SEP preliminary mechanical design
  - inputs for telescope pointing
  - inputs for location of telescope and electronics in box
  - thermal requirements
- Preliminary CPU I/F definition
- Firm up TOF and HVPS designs
- Preliminary Digital Electronics Specification
- Discussions with Caltech on CPU requirements

SIT - Schedule/Concerns

- Schedule
  - 13 months design (phase B through CDR)
  - 18 months instrument build/test (CDR through delivery)
  - 12 months S/C integration/test (delivery through launch)
- SIT Technical Staffing is very tight
  - Phase B: total technical effort is 2/3 of 1 FTE
  - Phase C/D: starts at 1/3 FTE for 1 year and drops to 1/10 FTE for remainder
- UMd has no technician so cannot build or modify flight hardware
  - how will we trim the electronics?
- There is no non-flight hardware to check designs

CPU Data Processing Requirements

- Collect and Process Event Data
  - Events arrive asynchronously over serial interface from SIT
  - Assign a box number and a 1-bit priority to each event using a sequence of lookup tables. For each event increment the appropriate box rate(s). Select events to be read to ground in full, based on priority bit.
  - Event rate < 1000/sec
  - Expected lookup table size: 28 kBytes
- Collect and Process Discriminator rates
  - Periodically (e.g. once/sec) collect discriminator rates. Accumulate them, compress them.
- Collect and Convert Analog HK data
  - Periodically collect 3 analog HK values, convert to digital
- Format data into Science Data Record and output to IDPU
- Commanding

Proposed Science Data Record

- 512 seconds of data
- Header, including time - 6 bytes
- 728 PHA events (36 bits each)
  - 728 * 4.5 bytes = 3726 bytes
- 128 low-time resolution (512 sec) box rates (compressed to 12 bits)
  - 128 rates * 1.5 bytes = 192 bytes
- 9 high time resolution (32 sec) box rates (compressed to 12 bits)
  - 9 rates * 16 intervals * 1.5 bytes = 216 bytes
- 6 discriminator rates (32 sec) (compressed to 12 bits)
  - 6 rates * 16 intervals * 1.5 bytes = 144 bytes
- Trailer including HK data and checksum - 6 bytes

- TOTAL: 3840 bytes / 512 sec = 60.0 bits/sec