Tycho and Branislav,

below please find the SEPT power breakdown. This is based on info's from Peter Falkner/ESTEC who is the ESTEC project engineer for the SEPT electronics. This closes the action item on me from the telecon dated 6-JUL-00.

Best regards
Reinhold

********** START **********

Case A (quiet rate)

Description	Number	Power/unit [mW]	Power total [mW]
PDFE ASIC, both channels on, digital output	8	67	536
FPGA, 20 mA @ 5 V	2	100	200
SRAM, standby 5 mW	2	5	10
Remaining electronics	2	150	300
Total			1,046

Case B (high rate)

Description	Power total [mW]
PDFE (no increase)	536
FPGA depends on design, assume modest increase of 10 %	220
SRAM 10 mW per MHz, 8 accesses per event (4 byte read and write)	170
Remaining electronics (no increase)	300
Total	1,226

Note: Remaining electronics comprises:
- voltage reference for PDFEs
- inflight test pulse generator (standby)
- latch-up monitor
- power-switch-off circuit
- interface to SEP DPU circuits which is still tbd
  (parallel, serial, symmetrical, opto couplers ?)

********** STOP **********