STEREO

SIT CPU24

Flight Software Requirements
March 5, 2002

PRELIMINARY

Glenn Mason, University of Maryland
Mihir Desai, University of Maryland
Peter Walpole, University of Maryland

1. Overview

The SIT flight software shall run on a CPU24 processor. The SIT sensor shall interface with its front-end electronics and the SEP Central MISC through a series of Universal Asynchronous Receiver/Transmitters (UARTs).

1.1. *Document Conventions*

1.1.1.1 In this document, TBD (To Be Determined) means that no information currently exists.

1.2. *Applicable Documents*

Some of these documents and drawings can be found on the Berkeley STEREO/IMPACT website: http://sprg.ssl.berkeley.edu/impact/dwc/

- STEREO SEP SIT and SIT CPU24 Processors, Flight Development Plan
- PHA User's Manual, Rich Cook, Clatech internal memo
- CPU24 Processor Manual, Bob Baker
- PHASOFT.DOC, Don Reames
- PHAINT.TXT, Don Reames

1.3. *Acronyms*

CPU24 24-Bit Embedded Microprocessor
DPU Data Processing Unit
SIT High Energy Telescope
ICD Interface Control Document
IMPACT In situ Measurements of Particles and CME Transients
LET Low Energy Telescope
MISC Minimal Instruction Set Computer
SEP Solar Energetic Particles
SIT Suprathermal Ion Telescope
SEPT Solar Electron Proton Telescopes
SRL Space Radiation Laboratory
UMD University of Maryland
GSFC Goddard Space Flight Center

2. Host System and Interfaces

2.1. *System Overview*

The LET, SIT and SIT sensors each require a dedicated microprocessor for onboard data processing. The microprocessor used for LET shall be the P24 MISC (Minimal

Instruction Set Computer), described in Reference 5. The microprocessor used for SIT and SIT shall be the CPU24 (24-Bit Embedded Microprocessor), which is described below and in Reference 4. Processed data from all of the microprocessors associated with these three sensors shall be gathered by the SEP Central MISC (P24 processor), and formatted for transmission to the IMPACT DPU (per Reference 7 ICD). The SEPT sensor does not have a dedicated microprocessor, and data from SEPT shall flow directly to the SEP Central MISC. Some processing of SEPT data shall occur in the SEP Central MISC before the data are formatted and transmitted to the IMPACT DPU. Figure 1 shows a block diagram of the SEP Instrument Suite.

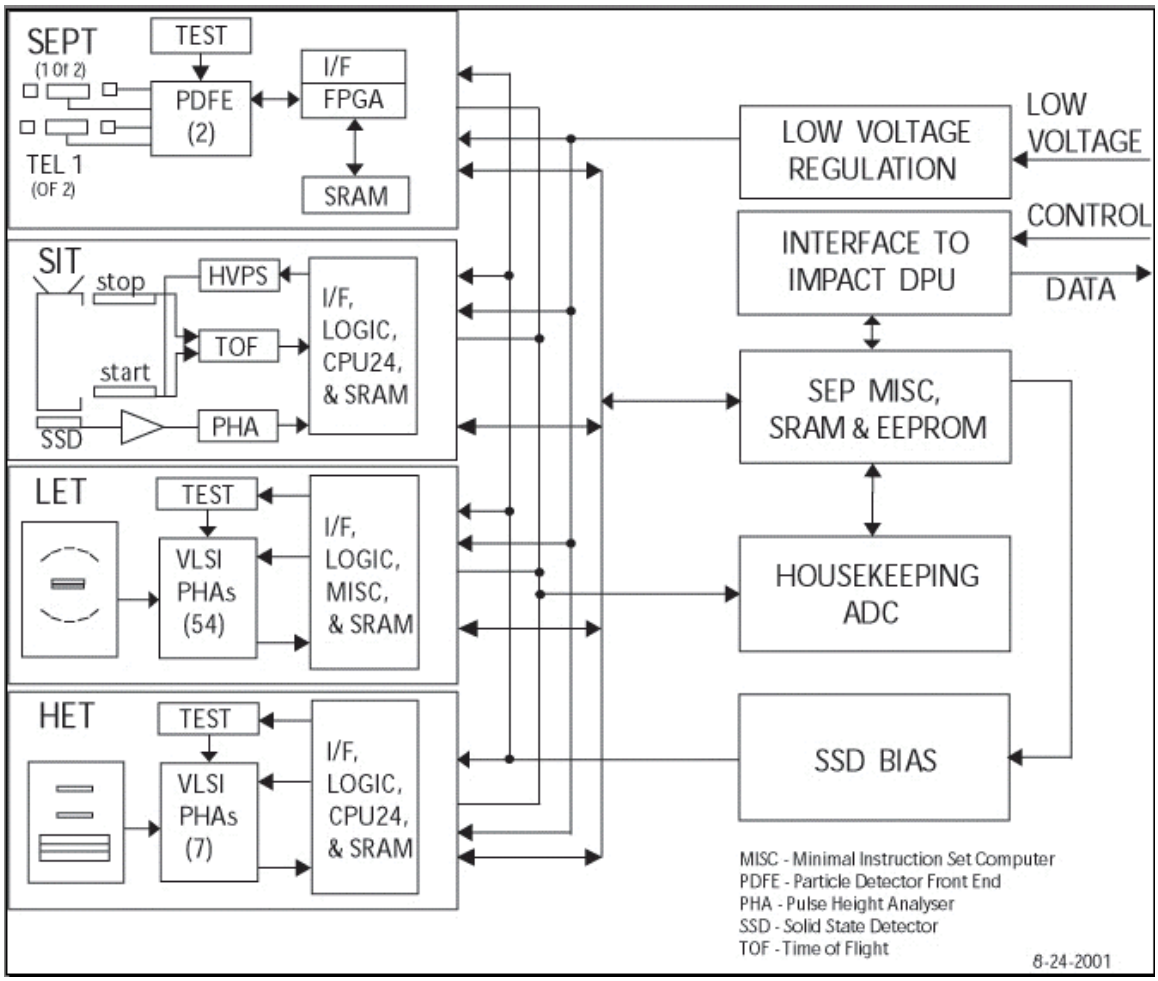


Figure 2.1: SEP Instrument Suite Block Diagram

2.2. *CPU24 Microprocessor*

The CPU24 has a 24-bit core with dual stack architecture. The processor design is simple to allow implementation within field programmable gate arrays. For STEREO SEP applications, the CPU24 is implemented in the ACTEL 54SX72A FPGA. The current implementation runs at 10 million instructions per second.

2.2.1. Code Memory

Current CPU24 development boards are provided with 128K×24 SRAM. The CPU24 boots over a serial link. During boot, system software is copied from the serial link to RAM and the software runs from RAM.

2.2.2. Memory Map

The CPU24 is capable of addressing a memory page of 256Kwords (each word is 24 bits). Other pages can be reached by pushing a 24-bit address on the return stack and executing the RET instruction, as described in Reference 4, but this capability is not expected to be required for STEREO (128K words of SRAM per CPU24 should be adequate).

2.2.3. I/O Bus (G-Bus) Peripherals

G-bus peripherals are described in detail in Reference 4. Currently, G-bus peripherals include:

```
g@0  read interrupt control and status register
g@1  read UART receiver data
g@2  read zero
g@3  read one

g!0  write interrupt control and status register
g!1  write UART transmit data
g!2  write second UART transmit data
g!3  write to test board LED's (lower four bits)
```

G-bus functions will be added to interface to the PHA ASICS and perform other functions as needed.

2.2.4. Boot ROM

The CPU24 contains 16 words of ROM that holds a small program to boot over the serial link. After a reset, the CPU24 starts execution at location 0 which is mapped to the internal ROM. The instruction at location 0 performs a jump to location 20001 (hex) where the remainder of the boot code is located. A fixed number of bytes are received over the serial link. Every three bytes received are packed into a 24-bit word, with the first byte going into the most significant slot and the third byte going into the least significant slot. Words are stored beginning at address 1 in SRAM. Execution begins at address 1 (in SRAM) following the serial transmission.

2.3. *External Interfaces*

Interface between the SEP and the SIT and SIT sensors

There shall exist two serial interfaces between the SEP and the SIT and SIT sensors. The first serial interface shall be bi-directional, for transferring boot-code, commands, and command responses. The second serial interface shall be uni-directional, for transferring

data from the SIT and SIT sensors to the SEP. These interfaces shall be defined in Reference 7 (TBD-Kecman/WRC).

2.4. *Hardware/Software Interfaces*

The hardware/software interfaces for the SIT and SIT processors shall be defined in the CPU24 processor manual (reference 4).

3. SIT CPU24 Software Requirements

3.1. *SIT CPU24 Software Overview*

The SIT CPU24 shall operate as a multi-tasking, interrupt-driven processor. It shall be coded using the CPU24 native assembly language. The SIT CPU24 main software logic shall accomplish the following tasks:

- Process next particle in event queue
    a. increment events-processed counter
    b. increment appropriate SW bin
    c. increment appropriate SW bin
    d. select and buffer PHA sample events
- If Cmd flag – process immediate command or queue it for EOF
- If 1-sec interrupt
    a. calibrate TOF system
    b. read hardware rates from TOF system
- If EOF:
    a. begin formatting output packets for HW & SW rates and PHAs.
    b. process any EOF commands to affect next frame.
    c. run algorithm enable/disable H1 singles processing at high rates
    d. clear all SW counters, clear event queues.
    e. clear EOF flag
- Continue formatting output packets, if any. This is done in pieces so that particle processing can continue, *i.e.* to prevent queues from filling.

The SIT CPU24 shall consists of the following software modules to perform the above logic:

- Science data acquisition
- Science data processing
- Beacon data processing
- Housekeeping and status data acquisition
- Command processing
- Science data formatting

3.2. *Interrupt Processing Overview*

The SIT CPU24 software system shall be responsive to servicing several interrupts, which are generated by the SEP Central MISC and the SIT front-end electronics. These interrupts are defined as the following:

- **Reset**

- **1-second timer**: Time synchronizing pulses from the SEP Central MISC will be 1 ms wide positive pulses with a 1 second period. Use to increment second clock (0-59).

- **1-minute timer**: Every 60^{th} 1-sec pulse will be followed, after a 1 ms delay, by an extra 1 ms wide pulse (the 1-minute timer pulse). The basic sensor data accumulation interval will be one minute, starting at the first 1-second timer pulse following the 1-minute timer pulse (i.e. reset the second clock to 0 at this time). The SIT CPU24 will send data to the SEP Central MISC during a 100 ms window following 1-second timer pulses 0, 3, 6, ….., 57. SIT may send no packets or more than 1 packet during a window, but packets should be spread out over the 60 second cycle. The 1-minute timer pulse may also be referred to as a frame synch pulse or end-of-frame (EOF) pulse since rate counters should be read out and reset at this time, packets should be queued for readout into the telemetry stream, and any status bits (e.g. the high-rate/low-rate bit) should be captured and readout.

- **Serial Command In**: There is a serial line which sends command information from the SEP Central MISC to the SIT CPU24 via the receive portion of the Command UART. An interrupt is set by the UART to indicate that the next command byte has been received.by the UART and is ready to be read by the SIT MISC to the command buffer. Boot-up of the SIT MISC also uses the Command UART.

- **Serial Command Out**: The Command UART also transmits Command Response information to the SEP Central MISC. This response information is to be printable ASCII text. An interrupt from the Command UART signals the MISC that it is ready to get the next byte to be transmitted from the command response buffer.

- **Serial Data Out**: The 'transmit' half of a UART (referred to as the Data UART) sends formatted data from the SIT CPU24 to the SEP Central MISC. The Data UART sends the Serial Data Out interrupt to the MISC when it is ready to get another byte of data to send out.

- **PHA**: The SIT front-end logic is in the same ACTEL chip as the SIT MISC. When the front-end logic detects that a pulse height event has been collected, the front-end logic sends an interrupt to the SIT CPU24 to go read

the event out of the front end logic. The pulse-height values for an event are read out using a 24-bit wide bus (the G-bus). When an event has been read it should be queued in a FIFO for further processing.

The PHA-in counter and the PHA-queued counter (if queued) should also be incremented correspondingly.

3.3. *SIT CPU24 Power-On Initialization*

In flight configuration, it is expected that the SIT CPU24 will boot via the serial link from the SEP Central MISC. Therefore, only the SEP Central MISC will need EEPROM during flight.

After the initial boot code has loaded, the SIT flight software shall be transferred over the serial link and loaded from the SEP Central MISC to the SIT CPU24.

Once the boot process has completed, the SIT CPU24 shall configure the SIT front-end electronics into a default state. The default state shall be defined in tables loaded into SRAM during the boot process.

3.3.1. **SIT CPU24 Boot-up Procedure Requirements**

3.3.1.1 The SIT CPU24 boot-up shall be able to download code and tables from the EEPROM in the SEP Central MISC.

3.4. *1-minute Timer Interrupt*

The 1-minute timer pulse shall invoke the rate counters to be read out and the PH event buffer to be formatted into science packets and be prepared for output. The End-of-Frame flag shall be set in response to the 1-minute timer interrupt.

3.4.1. **1-minute Timer Interrupt Software Requirements**

3.4.1.1 The 1-minute timer interrupt shall respond by setting the End-Of-Frame flag.

3.5. *SIT CPU24 Soft Reset*

The SIT CPU24 soft reset shall respond to command from the SEP Central MISC. The soft reset shall initialize all the hardware, and software counters and memory buffers; this includes resetting the End-Of-Frame (EOF) flag.

3.5.1. **SIT CPU24 Soft Reset Requirements**

3.5.1.1 The SIT CPU24 soft reset shall initialize all the UARTs.

3.5.1.2 The SIT CPU24 soft reset shall initialize and clock out all the hardware setup serial strings.

3.5.1.3 The SIT CPU24 soft reset shall clear all the software counters, queues and output packet buffers.

3.5.1.4 The SIT CPU24 soft reset shall be passed to the front-end logic which will initialize itself and the TOF system.

3.5.1.5 The SIT CPU24 soft reset shall wait for the End of Frame (EOF) flag, then clear it and start the main processing loop.

3.6. *Science Data Acquisition*

The SIT flight software shall be responsible for acquiring science data from the SIT front-end electronics. Event control logic on the MISC FPGA shall interrupt the MISC processor when event data is ready to be read into memory. Refer to the following SIT data flow block diagram (figure 3.6.1).

3.6.1. **Science Data Acquisition Software Requirements**

3.6.1.1 The SIT data acquisition software shall respond to the PHA event interrupt by reading a PHA event from the front end logic.

3.6.1.2 The SIT data acquisition module shall store each PH event in a queue using first-in-first-out (FIFO) ordering.

3.6.1.3 The SIT data acquisition module shall count all PH events read from the front end logic.

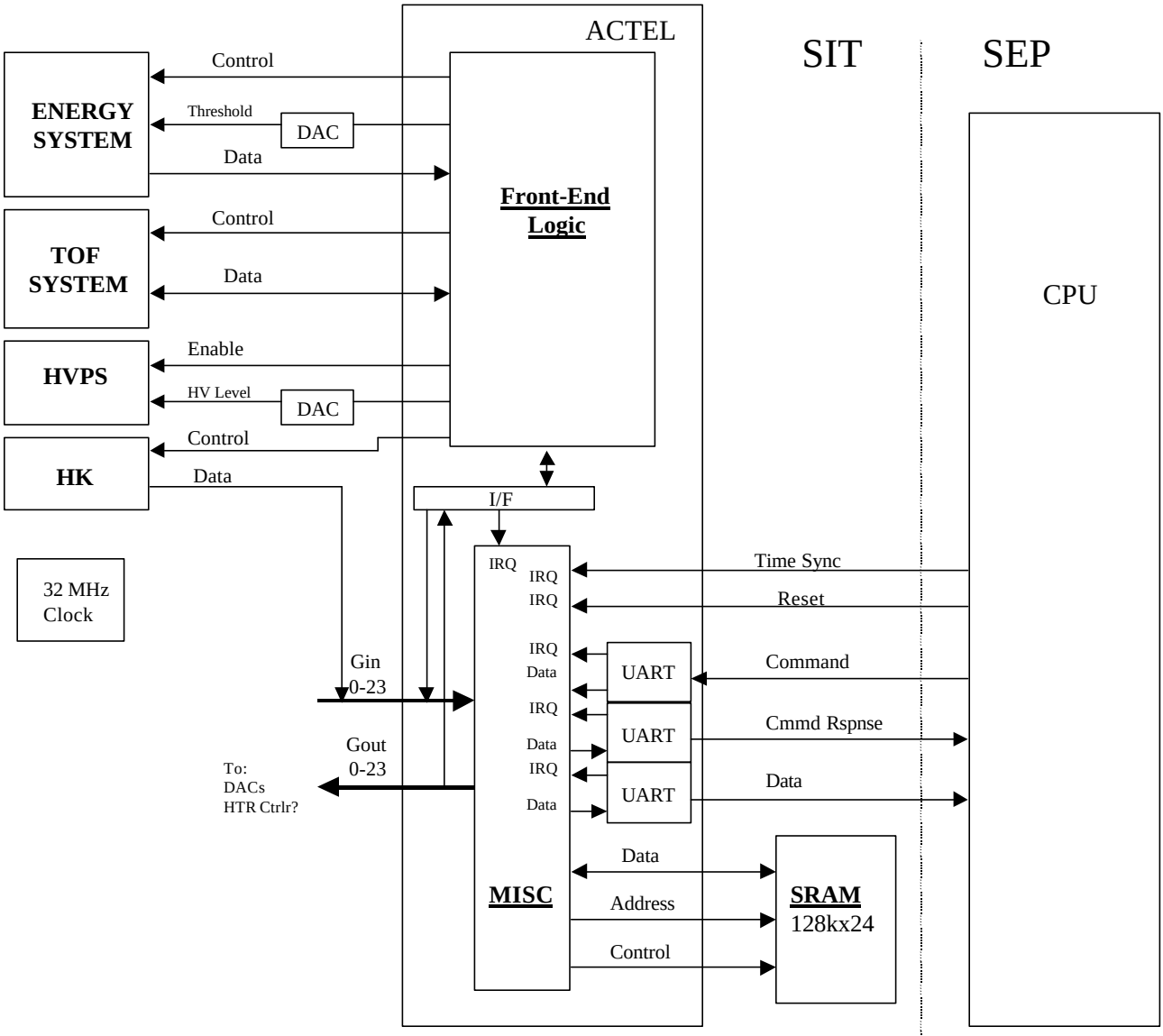


Fig. 3.6.1 SIT Logic/Data Flow Block Diagram

3.7. *Science Data Processing*

The telemetry bandwidth allocated to SIT is adequate to telemeter only a fraction of the events recorded by the instrument. Therefore the SIT software is required to process most events onboard. The objective of the onboard event processing software is to analyze the data gathered during each event and assign a species and energy to the particle that

generated the event. The species and energy determination shall be carried out using a 2-dimensional detector response matrix.

Once the software has determined the position of an event in the response matrix, the appropriate counter shall be incremented. It is expected that the size of a response matrix shall be of 128×128, with 100 software bins overlaid on the matrix. Each software bin shall have an associated counter. Note that this means that many cells of the response matrix shall lie within the same software bin and shall be associated with the same counter. The counters associated with the software bins shall be read out periodically, and this constitutes the data, which shall be telemetered.

When the SIT CPU24 receives an event interrupt, the interrupt service routine shall read the pulse-height data from the front end logic. The event is put into a queue for further processing. Refer to figure 3.7.

3.7.1. **Science Data Processing Software Requirements**

3.7.1.1 The SIT event processing module shall select the PH events from each priority type and store them in a sample event buffer. This buffer shall be used for output in the science data packet.

3.7.1.2 The SIT event processing module (Figure 3.7.1) shall determine species, energy and priority level (0 or 1) by using a 2-dimensional detector response matrix and riority table.

3.7.1.3 The SIT event processing module shall respond to the EOF reset by resetting the software counters.

3.7.1.4 The SIT event processing module shall respond to the EOF reset by resetting the hardware counters.

3.7.1.5 The SIT event processing module shall respond to the EOF reset by clearing all the event queues.

3.7.2. **SIT Event Interrupt Service and Processing DFD**

The following data flow diagram (Figure 3.8.1) shows the logic flow for the SIT event processing

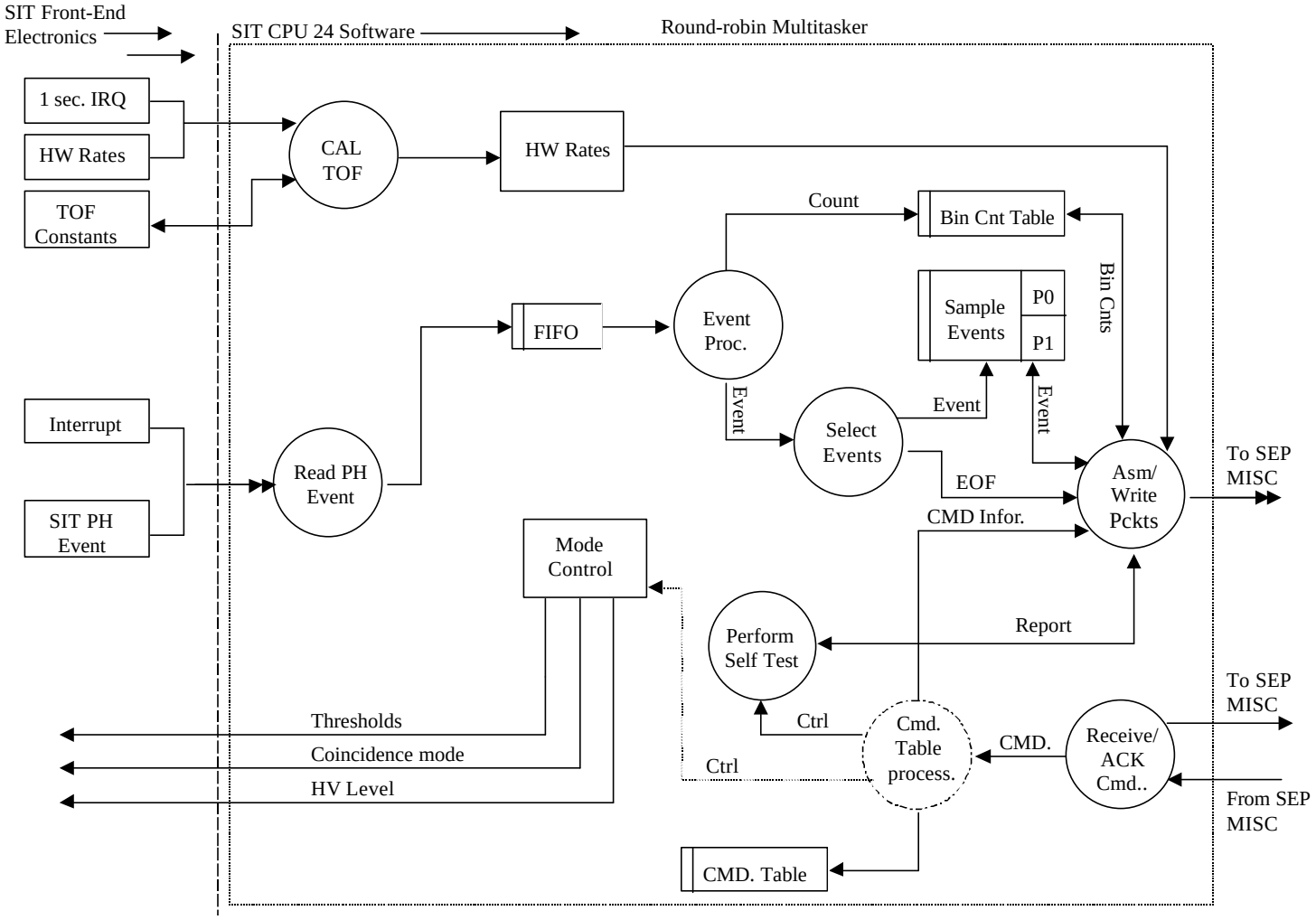
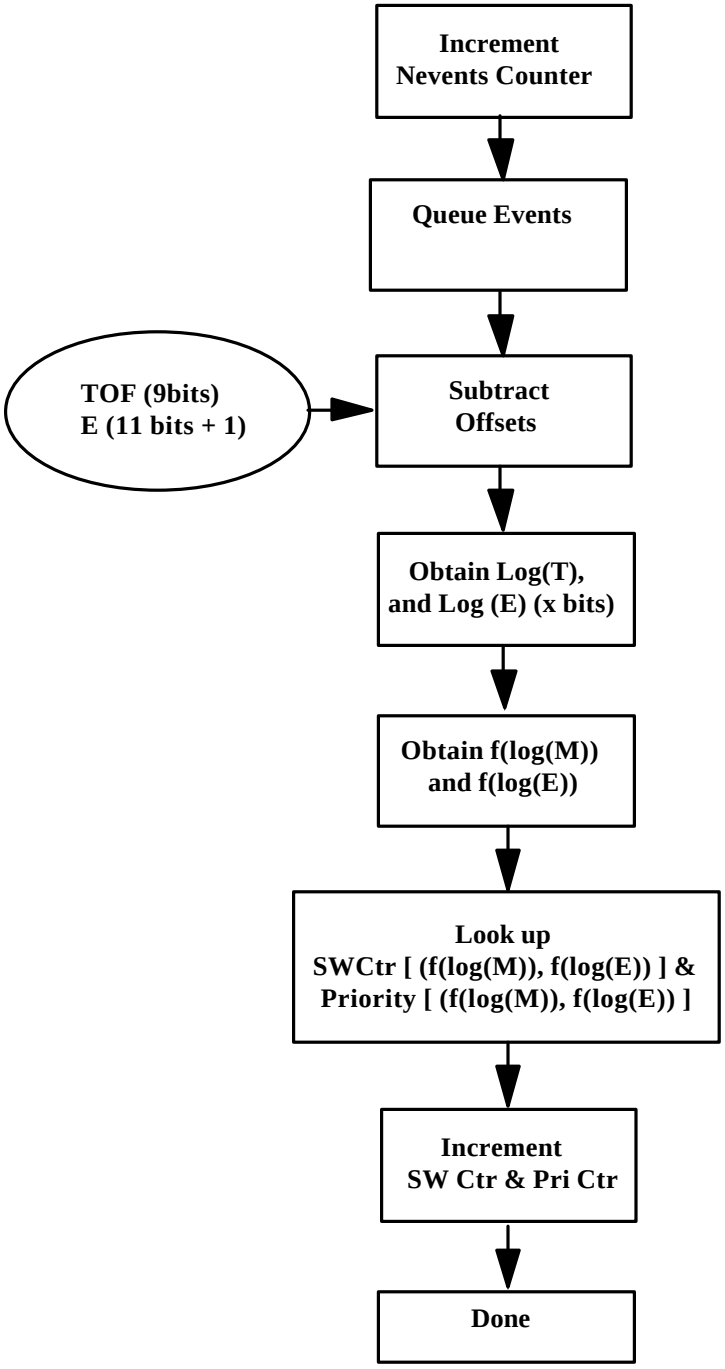

SIT Front-End Electronics
SIT CPU 24 Software
Round-robin Multitasker
1 sec. IRQ
HW Rates
TOF Constants
CAL TOF
HW Rates
Count
Bin Cnt Table
Bin Cnts
Sample Events
P0
P1
FIFO
Event Proc.
Event
Event
Event
Select Events
Interrupt
SIT PH Event
Read PH Event
EOF
Asm/ Write Pckts
To SEP MISC
CMD Infor.
Mode Control
Report
Perform Self Test
To SEP MISC
Thresholds
Coincidence mode
HV Level
Ctrl
Ctrl
Cmd. Table process.
CMD.
Receive/ ACK Cmd..
From SEP MISC
CMD. Table

Fig. 3.7

.

STEREO SIT Pulse Height Event Processing



1 March 2002

3.7.2.1 Figure 3.7.1

3.8. *Beacon Data Processing*

Beacon data shall be transmitted to the ground by the SEP Central MISC and are not to be included in the 6 packets per minute allocation. Beacon packets shall be generated once per minute by the SEP Central MISC using sub-packets sent each minute from the SIT sensor.

3.8.1. Beacon Data Processing Requirements

3.8.1.1 The SIT beacon data processing module shall calculate beacon data every 60 seconds.

3.8.1.2 The SIT beacon data processing module shall calculate beacon data for the following species and energy ranges:

Species	Energy Range (keV/nucleon)
He	20-100
He	100-1000
CNO	20-100
CNO	100-1000
Fe	20-100
Fe	100-1000

3.8.1.3 The SIT beacon data processing module shall format the beacon data into a packet of 272 bytes.

3.8.1.4 The SIT beacon data processing module shall transmit the beacon data packet every minute to the SEP Central MISC via the data-out UART.

3.9. *Housekeeping and Status Data Acquisition*

The SEP Central MISC shall be responsible for gathering housekeeping data (voltages, currents, temperature, checksums etc.). Housekeeping data are transmitted to the ground by the SEP Central MISC and are not be included in the 12 packets per minute allocation.

3.9.1. **Housekeeping and Status Data Acquisition Requirements**

3.9.1.1 The SIT housekeeping and status data acquisition module shall read SIT-specific software status information from the SEP Central MISC.

3.9.1.2 The SIT housekeeping and status data acquisition module shall read SIT-command table information from the SEP Central MISC.

3.9.1.3 The SIT housekeeping and status data acquisition module shall read SIT-specific software housekeeping information from the SEP Central MISC.

3.9.1.4 The SIT housekeeping and status data acquisition module shall format SIT-specific software status information for the science data packet.

3.9.1.5 The SIT housekeeping and status data acquisition module shall format SIT-specific software command table information for the science data packet.

3.9.1.6 The SIT housekeeping and status data acquisition module shall format SIT-specific software housekeeping information for the science data format..

3.9.1.7 The SIT housekeeping and status data acquisition module shall format the housekeeping and status data into a packet of 272 bytes.

3.10. ***Science Data Formatting***

Science data is to be transferred from the IMPACT DPU (IDPU) in packets of fixed length of 272 bytes, which includes an 11-byte header. SIT is allocated 12 packets per minute. Each packet shall include a checksum in order to be able to discriminate against data with bit errors.

Data packets collected from the instruments during a given accumulation minute (N) by the SEP Central MISC shall contain data accumulated during the previous minute (N-1) and shall be transmitted to the IDPU during minute N+1. The SEP Central MISC shall fill in the UT portion of all packet headers with the time corresponding to the beginning of the accumulation minute.

Special modes:

- **Accelerator testing mode**: In this mode the SEP Central MISC only pays attention to one sensor at a time. The sensor can use the full 57.6 kbaud bandwidth of the serial data line. The data format from the sensor can be anything in this mode, but could be in the form of multiple packets per second.

- **Variable packet rate**: The number of packets per minute generated by SIT should be commandable. This allows one sensor to make use of available bandwidth should another be disabled. Currently, in addition to SIT, SIT transmits 12 packets per minute in 100 ms windows following 1-second timer pulses 1, 4, …, 58; LET transmits 16 packets per minute following 1-second timer pulses 2, 5, …, 59; and SEPT has 2 packets per second handled separately by the SEP Central MISC.

The science data formatting software shall be responsible for formatting the SIT science data into minor frames, in response to the End of Frame Flag (EOF) being set. The SEP Central MISC shall perform formatting of SIT science frames into CCSDS packets. Checksum values shall be calculated for each packet in order to be able to discriminate against data with bit errors.

3.10.1. **Science Data Formatting Requirements**

3.10.1.1 The SIT data formatting module shall execute in response to the End of Frame (EOF) flag being set.

3.10.1.2 The SIT data formatting module shall retrieve the rate counters and the live time from memory.

3.10.1.3 The SIT data formatting module shall retrieve the sample PH event data from a buffer.

3.10.1.4 The SIT data formatting module shall format the SIT science data (rates and PH events) into science data packets.

3.10.1.5 The SIT data formatting module shall format 12 science packets accumulated over one minute.

3.10.1.6 The SIT data formatting module shall format each science packet to be 272 bytes in length, which includes an 11-byte header.

3.10.1.7 The SIT data formatting module shall calculate a checksum value for each science data packet.

3.10.1.8 The SIT data formatting module shall write the checksum value in the science data packet.

3.10.1.9 The SIT data formatting module shall transmit the science data packet to the SEP Central MISC via the data-out UART at the rate of 12 packets per minute.

3.10.1.10 The SIT data formatting module shall reset the End-Of-Frame (EOF) flag.

3.10.1.11

3.11. ***Command Processing***

Commands to the SIT CPU24 shall be used to set configuration control bits for front-end logic and to set the HV and discriminator levels. The command state of this instrument register be trickled to the ground every TBD minutes as part of the SIT housekeeping data.

Commands for SIT shall be received via the command data-in UART connection to the SEP Central MISC. Command responses from the SIT CPU24 shall be sent via the command data-out UART connection to the SEP Central MISC, where they will be formatted for telemetry. Flags shall be used in the SIT science data packets to indicate error conditions. Refer to the SIT Event Data Flow diagram.

Command responses are transmitted to the ground by the SEP Central MISC are are not included in the 12 packets per minute allocation.

3.11.1. **Command Processing Software Requirements**

3.11.1.1 The SIT command processing module shall respond to the serial command in interrupt by reading the command byte from the UART connection to the SEP Central MISC and storing it in a buffer.

3.11.1.2 The SIT command processing module shall use the command buffer and lookup and retrieve the associated commands in a table or shall decode the command directly - at the discretion of the programmer.

3.11.1.3 The SIT command processing module shall respond to commands to set data table values.

3.11.1.4 The SIT command processing module shall execute the commands producing a status flag to indicate error conditions.

3.11.1.5 The SIT command processing module shall write the command status flag to the science data packet.

3.11.1.6 The SIT command processing module shall respond to the serial command out interrupt by transmitting the command byte to the UART connection to the SEP Central MISC.

3.12. ***Reliability***

Abnormal conditions shall be detected by the SIT software and reported in the science data packet. It is not expected that automatic onboard correction of error conditions shall be implemented, but whenever possible (consistent with instrument safety) the system should remain in an operational state following an error. Error conditions shall be flagged in the science telemetry and corrective action shall be initiated from the ground.

3.12.1. **Reliability Requirements**

3.12.1.1 The SIT software shall be able to detect error conditions.

3.12.1.2 The SIT software shall set flags to indicate error conditions.

3.12.1.3 The SIT software shall write the error flags to the science data packet.

3.12.1.4 The SIT software shall remain in an operational state following an error condition.

3.12.1.5 The SIT software shall set flags to indicate error conditions.

3.12.1.6 If the command table method of command decoding is used:

3.12.1.6.1 The SIT software shall maintain a command table containing all variable settings (thresholds, gains, modes, etc).

3.12.1.6.2 The flight software shall calculate checksums on the variable setting command table.

3.12.1.6.3 The SIT software shall write the command table checksums to the science data packet.

3.12.1.6.4 The SIT software shall monitor the command tables for changes in status, if a change occurs, a flag shall be set.

3.12.1.6.5 The SIT software shall write the command table status flag to the science data packet.

4. Ground Support Equipment Software

The SIT CPU24 is being built by GSFC and needs to be tested and monitored using the ground support software. This software shall support the SIT CPU24 by itself and when it is connected to the SEP Central MISC, which is being built by Caltech. This support shall include the following tasks:

- Boot code loading via the UART.
- Display of data received via the UART.
- Plotting of the data received via the UART.
- Command processing via the UART.

4.1. *Ground Support Software Requirements*

4.1.1. **Boot Code Loading**

4.1.1.1 The SIT GSE software shall be able to load download boot-up code and tables.

4.1.2. **Display of SIT CPU24 Data Bytes**

4.1.2.1 The SIT GSE software shall be able to retrieve data packets via the UART.

4.1.2.2 The SIT GSE software shall be able to retrieve data packets via the TCP/IP protocol and use of Windows sockets.

4.1.2.3 The SIT GSE software shall be able to format the data packets into the LECR format.

4.1.2.4 The SIT GSE software shall be able to display the data packets in a readable a format.

4.1.2.5 The SIT GSE software shall allow selection of quantities for plotting.

4.1.2.6 The SIT GSE software shall be The SIT GSE software shall be able to write the LECR format data to an output file. This shall promote archiving of the test data and allow the user to review the data at a later time.

4.1.2.7 The SIT GSE software shall allow command file setup and processing.

4.1.3. **Plotting of the SIT CPU24 Data Bytes**

4.1.3.1 The SIT GSE software shall be able create 2 dimensional plots of the formatted data bytes.

4.1.3.2 The SIT GSE software shall allow selection of quantities for plotting.

4.1.3.3 The SIT GSE software shall allow command file setup and processing.

4.1.4. **Command Processing To and From the SIT CPU24**

4.1.4.1 The SIT GSE software shall be able to retrieve command bytes from the CPU24. This shall allow for simulation of commands being sent from the SIT CPU24 to the SEP Central MISC.

4.1.4.2 The SIT GSE software shall be able to send command bytes to the SIT CPU24. This shall allow for simulation of commands being sent from the SEP Central MISC to the SIT CPU24.