Specification of Functional Test Modules and In-flight Calibration Routines for LET
10/11/02

This document describes Functional Test Modules for pre-launch testing of LET as well as in-flight calibration routines. These routines are designed to make use of the built-in test-capacitors in each ADC, a programmable 8-bit DAC, and the MISC processor in LET. In this document we outline the design of the routines, including the pulse levels and patterns, describe the nature of the output of the tests, estimate the accuracy of the results, and estimate the time required to carry out the tests. The design of these routines builds on earlier experience with pre-launch and in-flight calibration of instruments on ISEE-3, SAMPEX, and ACE.

1. Functional Test Modules:

The following three functional test modules should test essentially all routine operating modes of LET and provide valuable calibration data that should be reproducible from one run to the next. One can envision long and short versions of each of these if required.

1) ADC Calibration – Calibrates all 54 ADCs at 32 specified DAC levels
2) Logic Test – Pulses detector combinations in a specified pattern with combinations of four DAC levels to test whether events are properly identified, sorted, and prioritized for telemetry
3) ADC Threshold Calibration - Tests stability of discriminator and noise levels by pulsing selected levels and monitoring “singles” rate data

Descriptions of these tests follow:

1.1 ADC Calibration

This module is designed to calibrate all of the 54 ADCs in LET. It will provide calibration data that can be fit off-line to measure the gain, offset, and linearity of each ADC, based on a total of 32 input pulse levels. There are two versions of this routine: (A) In the Functional Test mode both gain stages of all 54 ADCs are sequentially pulsed at a rate of ~5/sec, providing event data that is used to calibrate the ADC response. (B) In the continuous “STIM” mode, run continuously in background, the pulse pattern is the same, but the pulse rate is only ~0.1 second and it takes 2.8 hours to cycle through all ADCs. This latter routine is designed to be run continuously in flight and on the ground. Here we consider the Full ADC Calibration (Functional Test Mode).

Assumptions:

- ADC Cal events will be tagged and probably given high priority
- Assume an 8-bit DAC, 4-bit test capacitor selection (3.3 to 49.5 pF), and a “divide by 20” attenuation function
- Span full dynamic range of ~10,000 with 32 pulse levels

- Pulse at rate (~5/sec) that allows all events to be telemetered
- Pulse detector combinations that minimize/isolate any cross-talk
- Make use of appropriate test-pulser, DAC, and attenuation-factor combinations to span dynamic range of all L1, L2, L3 channels
- Telemeter both high and low gain values when both available
- The same DAC levels are used for all channels – could upload new list of values if needed.
- Pulse only one detector within a given PHASIC chip at a time
- Pulse A and B sides simultaneously
- Assume 32 DAC levels with pseudo-logarithmic spacing that spans the full dynamic range and adequately covers the extremes of all ADCs

Results:

Figures 1 and 2 show the pulse pattern and DAC levels that were assumed, along with the resulting energy levels in each ADC.

- With pulse rate of 5 per second it takes 14 minutes to cycle through all ADCs, giving eight pulses per ADC at each of 32 DAC levels.
- The 32 trial DAC levels result in 19 hi-gain and 25 lo-gain levels
- For expected noise levels (e.g., 30 keV for L1), uncertainty in the mean is nominally ~12 keV, much less than the channel width of 22 keV

1.2 Logic Test

The logic test is designed to trigger a full range of detector combinations with pulses that vary in amplitude in order to simulate particles with a range of nuclear masses and energy. In this case the LET telemetry data is monitored to see if the correct particle species are properly identified, prioritized, and selected for readout. The test is designed to be run at a rate that allows all events to be analyzed, but not all events will be read out because of telemetry limitations. The rate data should always produce reproducible results, hopefully it will also be the case that the same events are always telemetered.

Assumptions:
- Include events that trigger the A and B sides alone, as well as those that trigger both sides.
- Send separate pulses to L1A, L2A, L3A, L1B, L2B, and L3B, but do not send pulses to multiple detectors within the same PHASIC chip
- Attempt to design a test that can be executed in less than an hour – at 100/sec this means less than 2^{19} combinations

Results:

- Four pulse height levels were selected for each detector, corresponding roughly to H, He, O, and Fe. There are 4^3 possible combinations and when on-board angle corrections are made, a whole range of valid and invalid species are produced.

- The entire test is done with the same test capacitor selection
- By using the same (but scrambled) control bits for both side A and B it was possible to limit the test to 18 control bits
- The complete test (A-side, B-side, And B together) takes 33 minutes – a shorter version (A and B together) takes ~11 minutes
- Of the ~200,000 events pulsed, ~2/3 will give valid events, including all nominal detector combinations

The 18 control bits are listed below. For further detail, see Table 3.

A, B, or AB sides	2
L1 id	4
L2 id	4
L3id	2
L1 DAC level	2
L2 DAC level	2
L3 DAC level	2
Total	18

1.3 The ADC Threshold Test

There are 108 ADC thresholds in LET – two for each dual-gain ADC. They range in value from ~0.25 MeV to ~20 MeV. Taking into account the high-rate provisions, there are three nominal values for L2 and L3, and 4 for L1. This test is designed to monitor these levels and the associated detector noise levels. It does this by sequentially pulsing 256 DAC levels in a "ramp" fashion, and then counting how many pulses trigger each of the ADC thresholds by monitoring the rate data.

Assumptions:

- Best to do only one detector per chip at a time, but perhaps this does not matter since all pulse levels could be similar if ramped simultaneously
- Assume that all single detector rates due to noise and background are <1/minute (The test will last ~10 minutes or less)
- The test should be synchronized to start at the beginning of a 1-minute rate cycle

Results:

Table 4 lists the DAC levels, text capacitors, and resulting channel numbers that would be pulsed. The lowest energy to trigger the listed nominal thresholds are shown in bold. Note the following:

- It is possible to cover all low-gain and high-gain ADC thresholds with a dynamic range of 256.

• If pulse only one detector/chip at a time, and pulse each 16 times at each of 256 DAC levels, the test takes ~10 minutes to run
• The running time could be reduced substantially be pulsing more than one detector/chip at a time
• The precision achieved for the high-gain L1 and L2 thresholds is limited by the resolution of the DAC (.07 MeV).
• The high-gain precision could also be limited if there are also other noise or background triggers of several/minute or more
• The run time and L3 precision could be improved by changing test capacitors midway through the test – a minor complication

2.0 In-flight Live-time and ADC Calibration

The following routines are designed to be run continuously in-flight and on the ground to monitor ADC stability and instrument live-time performance.

2.1 ADC STIM Mode

This is an automated, continuous version of the ADC Calibration described above in Section 1.1. It completes a full test of all 54 ADCs (32 DAC levels) in 8 hours if the pulse rate is 0.1/sec.

The design is based on the following assumptions:

• STIM events will be tagged and possibly given high priority
• Assume an 8-bit DAC, 4-bit test capacitor selection (3.3 to 49.5 pF), and a "divide by 20" attenuation function
• Span full dynamic range of ~10,000 with 32 pulse levels
• Pulse at rate (=0.1/sec) that doesn't interfere with telemetry of real events
• Pulse detector combinations that minimize/isolate any cross-talk
• Evaluate precision as a function of pulse and background events rates
• Make use of appropriate test-pulser, DAC, and attenuation-factor combinations to span dynamic range of all L1, L2, L3 channels
• Telemeter both the high and low gain values when both available
• The same DAC levels are used for all channels – could upload new list of values if needed.

Trial values:
• Consider pulse rate of 0.1 per second
• Assume 32 DAC levels with pseudo-logarithmic spacing that spans the full dynamic range and adequately covers the extremes of all ADCs
• Pulse only one detector within a given PHASIC chip at a time
• Pulse A and B sides simultaneously

Results:
• With pulse rate of 0.1 per second it takes 2.8 hours to cycle through all ADCs, giving two pulses per ADC at each of 32 DAC levels.

- In one day each L1 and L2 ADCs is pulsed 17 times at all 32 levels
- The 32 trial DAC levels result in 19 hi-gain and 25 lo-gain levels
- For expected noise levels (e.g., 25 keV for L1), uncertainty in the mean is nominally ~6 keV per day, much less than the channel width of 22 keV
- Lose <2% of particle data due to telemetry limitations
- Dead-time impact is negligible

2.2 In-Flight Livetime Calibration – Not yet complete

During periods of high count rates there will be dead-time caused by the time it takes to process valid events and to reject ADC triggers that do not satisfy the coincidence requirements. Although the nominal livetime for creating new events is measured and reported it appears useful to monitor the performance of this of the on-board lifetime determination by sending test events through the system to see what fraction of them are recorded under varying circumstances. To be effective, the livetime monitor must compete with valid events – it cannot be given higher priority. The results of the test are obtained by seeing what fraction of these stimulated events are read out over a given time period.

Approach:
- These events compete with normal rates for on-board analysis
- Either three or four pulse levels (H, He, C, Fe?)
- Include Range 2, Range 3, and penetrating events (Range 4) for completeness
- Calculate probability of readout vs background event rate
- Assume accuracy due to binomial stats (e.g., observe N of 100 expected)
- Evaluate precision as a function of pulse and background events rates
- Calculate loss of data due to these events using rundown lengths

Trial values:
- Consider pulse rates of 1 to 100 per second (see Figure 1)
- Consider background event rates of 1 to 10^6
- Assume pulses that are at levels of H, He, C and Fe in the unpopulated region of pulse-height space beyond the End of Range (EOR) line.

Results:

Figures 1 and 2 summarize the **xxxxxxxxxxxxxxxxxxxxx**

- With pulse rate of ~1/second can achieve <2% precision in 15-minute samples for “background” trigger rates up to 10^5/sec
- At 10^4/sec background rate the precision is 0.5% for 15 minutes
- Lose 1.6% of data if there are 12 different monitors (3 high-gain, 1 low-gain for both Range 2 and Range 3)
- Precision for 1-hour rates will be twice as good as for 15-minute rates

Table 1: Strawman Detector Pulsing Sequence for ADC Calibration

ADC	L1a															L2a										L3a		L1b															L2b										L3b	
Seq.	1			2			3			4			5															1			2			3			4			5														
#	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	4	5	6	7	8	9	#	1	2	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	4	5	6	7	8	9	#	1	2
1	o															x												o															x											
2		o														x													o														x											
3			o														x													o														x										
4				o													x														o													x										
5					o													x														o													x									
6						o												x															o												x									
7							o												x															o												x								
8								o											x																o											x								
9									o											x																o											x							
10										o										x																	o										x							
11											o										x																	o										x						
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18		o																						x					o																						x			
19			o																						x					o																						x		
20				o																					x						o																					x		
21					o																					1						o																						1	
22						o																				1							o																					1	
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28												o															1												o																1
29													o													1														o														1	
30														o												1															o													1	
31															o												1															o													1
32																											1																												1

Table 2: Pulse Pattern for LET ADC Calibration

Pulse Number	L1 Cap Level	L1 Test Cap	Divide by 20	DAC Level	SignalSize MeV	Hi-Gain Ch #	Lo-Gain Ch #	L2 Cap Level	L2 Test Cap	Divide by 20	DAC Level	SignalSize MeV	Hi-Gain Ch #	Lo-Gain Ch #	L2 Cap Size	L2 Test Cap	Divide by 20	DAC Level	SignalSize MeV	Hi-Gain Ch #
1	1	3.3	20	5	0.36	16	0	1	3.3	20	5	0.36	10	0	4	13.2	20	5	1.46	15
2	1	3.3	20	10	0.73	32	0	1	3.3	20	10	0.73	19	0	4	13.2	20	10	2.92	30
3	1	3.3	20	20	1.46	65	0	1	3.3	20	20	1.46	39	0	4	13.2	20	20	5.83	60
4	1	3.3	20	40	2.92	130	0	1	3.3	20	40	2.92	78	0	4	13.2	20	40	11.67	120
5	1	3.3	20	60	4.38	195	10	1	3.3	20	60	4.38	116	6	4	13.2	20	60	17.50	180
6	1	3.3	20	90	6.56	292	15	1	3.3	20	90	6.56	175	9	4	13.2	20	90	26.25	270
7	1	3.3	20	120	8.75	390	19	1	3.3	20	120	8.75	233	12	4	13.2	20	120	35.01	360
8	1	3.3	20	150	10.94	487	24	1	3.3	20	150	10.94	291	15	4	13.2	20	150	43.76	450
9	3	9.9	20	60	13.13	584	29	5	16.5	20	60	21.88	582	29	13	42.9	20	60	56.88	585
10	3	9.9	20	90	19.69	877	44	5	16.5	20	90	32.82	873	44	13	42.9	20	90	85.33	878
11	3	9.9	20	120	26.25	1169	58	5	16.5	20	120	43.76	1164	58	13	42.9	20	120	113.77	1171
12	3	9.9	20	140	30.63	1364	68	5	16.5	20	140	51.05	1358	68	13	42.9	20	140	132.73	1366
13	3	9.9	20	160	35.01	1559	78	5	16.5	20	160	58.34	1552	78	13	42.9	20	160	151.69	1561
14	3	9.9	20	180	39.38	1753	88	5	16.5	20	180	65.64	1746	88	13	42.9	20	180	170.65	1756
15	3	9.9	20	200	43.76	1948	97	5	16.5	20	200	72.93	1940	97	13	42.9	20	200	189.61	1951
16	3	9.9	20	220	48.13	0	107	5	16.5	20	220	80.22	0	107	13	42.9	20	220	208.58	0
17	1	3.3	1	5	7.29	325	16	1	3.3	1	5	7.29	194	10	4	13.2	1	5	29.17	300
18	1	3.3	1	10	14.59	649	32	1	3.3	1	10	14.59	388	19	4	13.2	1	10	58.34	600
19	1	3.3	1	20	29.17	1299	65	1	3.3	1	20	29.17	776	39	4	13.2	1	20	116.69	1201
20	1	3.3	1	40	58.34	0	130	1	3.3	1	40	58.34	1552	78	4	13.2	1	40	233.37	0
21	1	3.3	1	60	87.51	0	195	1	3.3	1	60	87.51	0	117	4	13.2	1	60	350.06	0
22	1	3.3	1	90	131.27	0	292	1	3.3	1	90	131.27	0	175	4	13.2	1	90	525.09	0
23	1	3.3	1	120	175.03	0	390	1	3.3	1	120	175.03	0	234	4	13.2	1	120	700.12	0
24	1	3.3	1	150	218.79	0	487	1	3.3	1	150	218.79	0	292	4	13.2	1	150	875.14	0
25	3	9.9	1	60	262.54	0	584	5	16.5	1	60	438	0	584	13	42.9	1	60	1138	0
26	3	9.9	1	90	393.82	0	877	5	16.5	1	90	656	0	876	13	42.9	1	90	1707	0
27	3	9.9	1	120	525.09	0	1169	5	16.5	1	120	875	0	1168	13	42.9	1	120	2275	0
28	3	9.9	1	140	612.60	0	1364	5	16.5	1	140	1021	0	1363	13	42.9	1	140	2655	0
29	3	9.9	1	160	700.12	0	1559	5	16.5	1	160	1167	0	1558	13	42.9	1	160	3034	0
30	3	9.9	1	180	787.63	0	1753	5	16.5	1	180	1313	0	1753	13	42.9	1	180	3413	0
31	3	9.9	1	200	875.14	0	1948	5	16.5	1	200	1459	0	1947	13	42.9	1	200	3792	0
32	3	9.9	1	220	962.66	0	0	5	16.5	1	220	1604	0	0	13	42.9	1	220	4172	0

Nominal Dynamic Range Data

Detector	Hi-Gain Thresh	Hi-Gain FullScale	Hi-Gain Dynami Range	Lo-Gain Thresh	Lo-Gain FullScale	Lo-Gain Dynamic Range	Full Dynamic Range
L1	0.20	46	230	1.8 - 4	920	500	8000
L2	0.25	77	308	3.1 - 4.8	1534	500	5111
L3	1	199	199	8. to 20.	3989	500	9973

Functional Test Mode

Ground Pulse Period (sec)	Fraction of PHA Data	8 pulses Full Cal (min)
0.2	0.909	13.7
0.5	0.364	34.1
1	0.182	68.3

Continuous Flight Mode

Flight Pulse Period (sec)	Fraction of PHA Data	Full Cal(2) (Hr)	# Full Cals per day
10	0.018	2.8	16.9
30	0.006	8.5	
60	0.003	17.1	

(1) Assume 100 bits/event

(2) Includes two pulses per detector per DAC level

There are 32 detector combinations and

Each detector actually pulsed once per 1

Table 3: Logic Test

Control Bits=>		ID Bits						Side Bits				DAC Bits (4 levels of each)		
		4		4		2		2				2	2	2
		L1		L2		L3		0	1	2	3	L1	L2	L3
		A	B	A	B	A	B	A	B	AB	skip	DAC	DAC	DAC
None		0	15									1	1	1
L1A	1	1	14					Use these				4	4	4
	2	2	13					to decide				64	64	64
	3	3	12					if doing				256	256	256
L2A	1	4	11					only one or						
	2	5	10					both sides						
	3	6	9											
L3A	1	7	8											
	2	8	7											
	3	9	6											
L4A	1	10	5											
	2	11	4											
	3	12	3											
L5A	1	13	2											
	2	14	1											
	3	15	0											
L2	1			0	15									
	2			1	14									
	3			2	13									
	4			3	12									
	5			4	11									
	6			5	10									
	7			6	9									
	8			7	8									
	9			8	7									
	10			9	6									
none				10	5									
none				11	4									
none				12	3									
none				13	2									
none				14	1									
none				15	0									
L3A	1					0	0							
	2					1	1							
none						2	2							
none						3	3							

This gives 64 pulse height combinations for L1L2L3
16 pulse height combinations for L1, L2

Time in minutes at a given rate

Total	Total pulses	3	10	30	100	300	1000	Rate
18	196608	1092	328	109	33	11	3	Minutes
Bits					Assume this			

Tests both rate and event data
Approximately 70% of these patterns result in an event
Question: Do pulses above full scale cause a coincidence?

Tentative Energy Levels for DAC Bits

Detector	DAC Level	MeV
L1	1	0.5
	4	2
	64	32
	256	128
L2	1	0.75
	4	3
	64	48
	256	192
L3	1	1.5
	4	6
	64	96
	256	384

Tentative Order for Changing Bits
(from lsb to msb)

6 DAC Bits
2 Side Bits
10 ID Bits

Table 4: Pulse Pattern for LET ADC Threshold Calibration

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Functional Test Mode

Note that after Dac Level 20 not all are shown

Detector	Hi-Gain Thresh	Hi-Gain FullScale	Hi-Gain Dynamic Range	Lo-Gain Thresh	Lo-Gain FullScale	Lo-Gain Dynamic Range	Full Dynamic Range	Ground Pulse Rate (/sec)	Fraction of PHA Data	AllatOnce Timefor 256x100 Pulses (min)	L1 separate Timefor 256x15x16 Pulses (min)
L1	0.25	46	184	1.8 - 4	920	500	8000	300	all	1.4	3.4
L2	0.25	77	308	3.1 - 4.8	1534	500	5111	100	all	4.3	10.2
L3	1	199	199	8. to 20.	3989	500	9973	30	all	14.2	34.1

Pulse Number	L1 Cap Level	L1 Test Cap	Divide by 20	DAC Level	SignalSize MeV	Hi-Gain Ch #	Lo-Gain#1 Ch #	Lo-Gain#2 Ch #	L2 Cap Level	L2 Test Cap	Divide by 20	DAC Level	SignalSize MeV	Hi-Gain Ch #	Lo-Gain Ch #	Lo-Gain Ch #	L3 Cap Size	Test Cap (pF)	Divide by 20	DAC Level	SignalSize MeV	Hi-Gain Ch #	Lo-Gain Ch #	Lo-Gain Ch #
1	1	3.3	20	1	0.07	0	0	0	1	3.3	20	1	0.07	0	0	0	2	6.6	20	1	0.15	0	0	0
2	1	3.3	20	2	0.15	0	0	0	1	3.3	20	2	0.15	0	0	0	2	6.6	20	2	0.29	0	0	0
3	1	3.3	20	3	0.22	0	0	0	1	3.3	20	3	0.22	0	0	0	2	6.6	20	3	0.44	0	0	0
4	1	3.3	20	4	0.29	**13**	0	0	1	3.3	20	4	0.29	**8**	0	0	2	6.6	20	4	0.58	0	0	0
5	1	3.3	20	5	0.36	16	0	0	1	3.3	20	5	0.36	10	0	0	2	6.6	20	5	0.73	0	0	0
6	1	3.3	20	6	0.44	19	0	0	1	3.3	20	6	0.44	12	0	0	2	6.6	20	6	0.88	0	0	0
7	1	3.3	20	7	0.51	23	0	0	1	3.3	20	7	0.51	14	0	0	2	6.6	20	7	1.02	**11**	0	0
8	1	3.3	20	8	0.58	26	0	0	1	3.3	20	8	0.58	16	0	0	2	6.6	20	8	1.17	12	0	0
9	1	3.3	20	9	0.66	29	0	0	1	3.3	20	9	0.66	17	0	0	2	6.6	20	9	1.31	14	0	0
10	1	3.3	20	10	0.73	32	0	0	1	3.3	20	10	0.73	19	0	0	2	6.6	20	10	1.46	15	0	0
11	1	3.3	20	11	0.80	36	0	0	1	3.3	20	11	0.80	21	0	0	2	6.6	20	11	1.60	17	0	0
12	1	3.3	20	12	0.88	39	0	0	1	3.3	20	12	0.88	23	0	0	2	6.6	20	12	1.75	18	0	0
13	1	3.3	20	13	0.95	42	0	0	1	3.3	20	13	0.95	25	0	0	2	6.6	20	13	1.90	20	0	0
14	1	3.3	20	14	1.02	45	0	0	1	3.3	20	14	1.02	27	0	0	2	6.6	20	14	2.04	21	0	0
15	1	3.3	20	15	1.09	49	0	0	1	3.3	20	15	1.09	29	0	0	2	6.6	20	15	2.19	23	0	0
16	1	3.3	20	16	1.17	52	0	0	1	3.3	20	16	1.17	31	0	0	2	6.6	20	16	2.33	24	0	0
17	1	3.3	20	17	1.24	55	0	0	1	3.3	20	17	1.24	33	0	0	2	6.6	20	17	2.48	26	0	0
18	1	3.3	20	18	1.31	58	0	0	1	3.3	20	18	1.31	35	0	0	2	6.6	20	18	2.63	27	0	0
19	1	3.3	20	19	1.39	62	0	0	1	3.3	20	19	1.39	37	0	0	2	6.6	20	19	2.77	29	0	0
20	1	3.3	20	20	1.46	65	0	0	1	3.3	20	20	1.46	39	0	0	2	6.6	20	20	2.92	30	0	0
22	1	3.3	20	22	1.60	71	0	0	1	3.3	20	22	1.60	43	0	0	2	6.6	20	22	3.21	33	0	0
24	1	3.3	20	24	1.75	78	0	0	1	3.3	20	24	1.75	47	0	0	2	6.6	20	24	3.50	36	0	0
26	1	3.3	20	26	1.90	84	**4**	0	1	3.3	20	26	1.90	50	0	0	2	6.6	20	26	3.79	39	0	0
28	1	3.3	20	28	2.04	91	5	0	1	3.3	20	28	2.04	54	0	0	2	6.6	20	28	4.08	42	0	0
30	1	3.3	20	30	2.19	97	5	0	1	3.3	20	30	2.19	58	0	0	2	6.6	20	30	4.38	45	0	0
32	1	3.3	20	32	2.33	104	5	0	1	3.3	20	32	2.33	62	0	0	2	6.6	20	32	4.67	48	0	0
34	1	3.3	20	34	2.48	110	6	0	1	3.3	20	34	2.48	66	0	0	2	6.6	20	34	4.96	51	0	0
36	1	3.3	20	36	2.63	117	6	0	1	3.3	20	36	2.63	70	0	0	2	6.6	20	36	5.25	54	0	0
38	1	3.3	20	38	2.77	123	6	0	1	3.3	20	38	2.77	74	0	0	2	6.6	20	38	5.54	57	0	0
40	1	3.3	20	40	2.92	130	6	0	1	3.3	20	40	2.92	78	0	0	2	6.6	20	40	5.83	60	0	0
45	1	3.3	20	45	3.28	146	7	0	1	3.3	20	45	3.28	87	**4**	0	2	6.6	20	45	6.56	68	0	0
50	1	3.3	20	50	3.65	162	8	0	1	3.3	20	50	3.65	97	5	0	2	6.6	20	50	7.29	75	0	0
55	1	3.3	20	55	4.01	179	9	**9**	1	3.3	20	55	4.01	107	5	0	2	6.6	20	55	8.02	83	**4**	0
60	1	3.3	20	60	4.38	195	10	10	1	3.3	20	60	4.38	116	6	0	2	6.6	20	60	8.75	90	4	0
65	1	3.3	20	65	4.74	211	11	11	1	3.3	20	65	4.74	126	6	0	2	6.6	20	65	9.48	98	5	0
70	1	3.3	20	70	5.11	227	11	11	1	3.3	20	70	5.11	136	7	**7**	2	6.6	20	70	10.21	105	5	0
75	1	3.3	20	75	5.47	244	12	12	1	3.3	20	75	5.47	145	7	7	2	6.6	20	75	10.94	113	6	0
80	1	3.3	20	80	5.83	260	13	13	1	3.3	20	80	5.83	155	8	8	2	6.6	20	80	11.67	120	6	0
85	1	3.3	20	85	6.20	276	14	14	1	3.3	20	85	6.20	165	8	8	2	6.6	20	85	12.40	128	6	0
90	1	3.3	20	90	6.56	292	15	15	1	3.3	20	90	6.56	175	9	9	2	6.6	20	90	13.13	135	7	0
95	1	3.3	20	95	6.93	308	15	15	1	3.3	20	95	6.93	184	9	9	2	6.6	20	95	13.86	143	7	0
100	1	3.3	20	100	7.29	325	16	16	1	3.3	20	100	7.29	194	10	10	2	6.6	20	100	14.59	150	7	0
110	1	3.3	20	110	8.02	357	18	18	1	3.3	20	110	8.02	213	11	11	2	6.6	20	110	16.04	165	8	0
120	1	3.3	20	120	8.75	390	19	19	1	3.3	20	120	8.75	233	12	12	2	6.6	20	120	17.50	180	9	0
130	1	3.3	20	130	9.48	422	21	21	1	3.3	20	130	9.48	252	13	13	2	6.6	20	130	18.96	195	10	0
140	1	3.3	20	140	10.21	455	23	23	1	3.3	20	140	10.21	272	14	14	2	6.6	20	140	20.42	210	10	**10**
150	1	3.3	20	150	10.94	487	24	24	1	3.3	20	150	10.94	291	15	15	2	6.6	20	150	21.88	225	11	11
160	1	3.3	20	160	11.67	520	26	26	1	3.3	20	160	11.67	310	16	16	2	6.6	20	160	23.34	240	12	12
170	1	3.3	20	170	12.40	552	28	28	1	3.3	20	170	12.40	330	17	17	2	6.6	20	170	24.80	255	13	13
180	1	3.3	20	180	13.13	584	29	29	1	3.3	20	180	13.13	349	18	18	2	6.6	20	180	26.25	270	13	13
190	1	3.3	20	190	13.86	617	31	31	1	3.3	20	190	13.86	369	18	18	2	6.6	20	190	27.71	285	14	14
200	1	3.3	20	200	14.59	649	32	32	1	3.3	20	200	14.59	388	19	19	2	6.6	20	200	29.17	300	15	15
210	1	3.3	20	210	15.32	682	34	34	1	3.3	20	210	15.32	407	20	20	2	6.6	20	210	30.63	315	16	16
220	1	3.3	20	220	16.04	714	36	36	1	3.3	20	220	16.04	427	21	21	2	6.6	20	220	32.09	330	16	16
230	1	3.3	20	230	16.77	747	37	37	1	3.3	20	230	16.77	446	22	22	2	6.6	20	230	33.55	345	17	17
240	1	3.3	20	240	17.50	779	39	39	1	3.3	20	240	17.50	466	23	23	2	6.6	20	240	35.01	360	18	18
250	1	3.3	20	250	18.23	812	41	41	1	3.3	20	250	18.23	485	24	24	2	6.6	20	250	36.46	375	19	19
256	1	3.3	20	256	18.67	831	42	42	1	3.3	20	256	18.67	497	25	25	2	6.6	20	256	37.34	384	19	19