STEREO IMPACT

PROBLEM REPORT
PR-7005
SEPT-Counting
2004-10-10

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Kiel, 8xxx=ESTEC, 9xxx=MPAe

Assembly : IMPACT SEPT-NS FM1	**SubAssembly : Electronics Box**
Component/Part Number: FPGA/RAM	**Serial Number:** A201 SN2
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Failure Occurred During (Check one √)

√ Functional test □ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

√ Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum □ Thermal-Vacuum □ EMI/EMC

Problem Description

On October 10, 2004, FM1 SEPT (both –E and –NS) were connected to FM1 SEP-Central and FM1 LVPS for the first time. Power consumption and a run in nominal observation mode were flawless, however, a run in test mode showed missing counts in two out of four histograms (dubbed PDFE 0 and 1) of SEPT-NS. When in test mode, an in-flight test pulse generator is running at 17.5 kHz. For an accumulation period of 60 seconds, the expected counting result is 1,047,552. This was shown by PDFE 2 and 3, but PDFE 0 and 1 showed a factor ~10 less. This failure may have been present from the time of assembly of the electronics, but went undetected, because the test pulse runs were shortened to one second to save time. Counts are not missing at low counting results (e.g. at 17,500), but only at high counting results.

Analyses Performed to Determine Cause

SEPT-NS was connected to the GSE and by varying the accumulation time, the erroneous behaviour could be tracked down to a stuck bit 15 in the 24 bit counting arithmetic. Possible failure sources are the Actel FPGA and the Static RAM. The FPGA was burned with the “old” algorithm. As this failure case does not invalidate the EMC test, SEPT-NS will continue with EMC. All other units (FM1 SEPT-E and FM2 SEPT-E/-NS) are checked at ambient and do not show the failure. Further investigations with newly designed test runs are detailed below. They point to a stuck bit in the FPGA adder circuitry.

Corrective Action/ Resolution

□ Rework √ Repair □ Use As Is □ Scrap

A quick repair is possible by exchanging the digital electronics board in SEPT-NS (A201 SN2) with the board in the flight spare (A195/201 S/N5). (see PR-7004 SEPT-Accident). This can be achieved in time before the scheduled vibration and TV tests. The FPGA (RT54SX32S-CQ208B, LDC0202 5, S/NT25JS001) will be replaced by a spare part burned with the new algorithm, and the repaired digital board (DB-A1-2G) together with the analog board (AB-A1-2D) will serve in the flight spare.

A review of the Actel design and board layout has determined that there were no issues with the design or layout. This review was performed by the Office of Logic Design. It is not certain whether or not the failure is due to an antifuse failure, but it does appear that it is something inside the part. There is nothing within the design or layout that contributed to the failure. This part will be submitted to Actel for failure analysis through the University of Kiel. The results of this analysis is not expected to be available until after launch.

This problem has not been seen on any of the other 3 flight units nor has it been seen through recent tests on this unit with the newly programmed part.

Date Action Taken: NOV-04 **Retest Results**: Board level test passed (15-NOV-04) and has successfully ompleted all instrument level environmental tests.

Corrective Action Required on other Units □ Serial Number(s): n/a

Closure Approvals

Subsystem Lead:	Reinhold Mueller-Mellin	Date: 08-DEC-04
IMPACT Project Manager:	_____	Date:_____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____

The following tests were performed in order to identify the origin of the problem:

FM1 SEPT-NS was connected to the ESTEC GSE. The first test was conducted by using different accumulation times (0.01, 0.1, 1, 2, 3, 4, 300, 600 and 800 seconds) with the on-board test pulse generator producing pulses at 17.579 kHz. The results show that for PDFE0 and PDFE1 channels, the recorded numbers of counts are wrong for t > 2 seconds. In fact, the recorded numbers of counts were the expected one modulo 32768 (with marginal noise on top). For PDFE2 and PDFE3 (as well as for all the other three units), the recorded numbers of pulses are exactly the expected ones. A second test was performed in order to see whether 32768 counts could be recorded. By tuning the different parameters such as accumulation time and gain of PDFE0, it was possible to obtain operating conditions for which the expected number of counts should statistically be 32768. The test was performed 1000 times to be statistically valid. The values 32766, 32767 as well as 1, 2 were obtained but not 32768, instead the value 0 was recorded. PDFE1 followed the same behaviour.

The energy histogram counters (32 bins in the present mode) of each channel are 24 bit wide (stored in 32-bit-word-aligned address in the SRAM). The SRAM is addressed byte-wise, consequently for each counter access, 3 byte reads are performed, followed by three byte writes. PDFE0 and PDFE1 channels share the same SRAM interface pins as well as the same FPGA implementation of the 24-bit adder performing the increment. The missing value 32768 strongly suggests that the problem is internal to the FPGA. Indeed, a hypothetical problem in the SRAM would appear on the 3 bytes of each histogram counter, however, the observed problem is independent of the SRAM address. Since the value 32767 can be read from the SRAM, the problem is very likely located in the adder where bit 15 could be stuck.

Rework completed (November 2004):

Both electronics boards (analog and digital) were disassembled from the flight spare unit and assembled into the SEPT-NS FM1 unit at ESTEC from 05-NOV-04 through 12-NOV-04. The digital board is equipped with a FPGA already burned with the new algorithm as a result of the SEPT accident (see PR-7004 SEPT-Accident). The failed digital board has received a new SRAM and was still failing pointing unambiguously to the FPGA as the culprit. The board will receive a new FPGA, also burned with the new algorithm, and together with its analog board serve as new flight spare electronics.

Retest completed (November 2004):

On 15-NOV-04 SEPT-NS FM1 was tested thoroughly with special attention to the counting arithmetic. It showed nominal performance and was declared ready for the repetition of the environmental tests. The new flight spare electronics is still awaiting rework and check-out.

Rework of Flight Spare completed (June 2005):

The stressed FPGA was replaced by a spare part burned with the new algorithm. The repaired digital board was installed into the E-box of SEPT Flight Spare, tested with one temperature cycle. The test was successful.