STEREO IMPACT

PROBLEM REPORT
PR-7004
SEPT-Accident
2004-05-04

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Kiel, 8xxx=ESTEC, 9xxx=MPAe

Assembly : IMPACT SEPT-NS FM2	**SubAssembly : Electronics Box**
Component/Part Number: FPGA	**Serial Number:** A201 SN4
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Failure Occurred During (Check one √)

√ Functional test □ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

√ Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum □ Thermal-Vacuum □ EMI/EMC

Problem Description

On May 4, 2004, the SEPT-NS FM2 was located on the vertical laminar flow bench in the Kiel clean room, connected via a 4 m long harness to its EGSE on a table nearby. The harness was fixed with tape to the clean bench near the SEPT-NS. The EGSE was connected to mains supply and switched on, but all SEPT-NS power supply rails were turned off. During repair work on a vacuum system nearby in the clean room not related to SEPT, the EGSE accidentally fell off the table to the floor, hitting a mains power cord (240 V, 50 Hz) of a dust particle counter on the clean bench. The power cord was cut through by the edge of the EGSE housing. A spark erupted before the mains fuse of the clean room supply was blown. Mechanically, the SEPT-NS was not involved. After the accident, SEPT-NS was connected to the spare EGSE. It performed nominally with all detectors alive and no changes compared to calibration records. The only change observed was the current on the 2.6 V rail which provides power to the core of the ACTEL FPGA. While it was 32 mA before the accident, it was 64 mA afterwards.

Analyses Performed to Determine Cause

The damaged EGSE was checked electrically with no malfunctions observable. The SEPT-NS electronics box was returned to ESTEC and opened to check whether some capacitors which could have been candidates for this failure mode (increased current) were affected. All related components were found inconspicuous. An engineer from ACTEL, visiting ESTEC for other reasons, was contacted and confirmed that this is a known failure mode when the FPGA is stressed by overvoltage.

Corrective Action/ Resolution

√ Rework □ Repair □ Use As Is □ Scrap

A parts stress analysis was performed and only the Actel was stressed. The stressed ACTEL FPGA (FPGA RT54SX32S-CQ208B LDC 0202 5, T25JS001 S/N 5461) was removed from the digital board (DB-A1-2E). A new FPGA RT54SX32S-CQ208B LDC 0202 5, T25JS001 S/N 5471 using the 4.37 software version was soldered into the board – now the Spare Board. Note that the FPGA was not soldered more than once before, because the change in FPGA programming was done on FM1 while FM2 was directly equipped with the new program version. The analogue and digital boards in SEPT-NS FM2 were replaced by the spare boards (DB-A1-2A and AB-A1-2B) from the spare unit (A195/201 SN5), the reworked electronics boards, (DB-A1-2E and AB-A1-1G), shall be used in the flight spare (A195/201 SN5), but where later used in A201-SN2 (see PR-7005). The “old” spare boards were tested with the flight unit and all tests were successful until EMC (Oct 2004) where a failure was discovered within the ACTEL FPGA (Reference: PR-7005).

Date Action Taken: August 31, 2004 **Retest Results**: Spare boards tested OK in FM2 SEPT-NS
Corrective Action Required on other Units √ Serial Number(s): A195/201 SN5 (Flight Spare)

Closure Approvals

Subsystem Lead:	Reinhold Mueller-Mellin	Date: 09-SEP-04
IMPACT Project Manager:	_____	Date _____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____