STEREO IMPACT

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag,
6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : HET Instrument	**SubAssembly :**
Component/Part Number:	**Serial Number: FM2**
Originator: von Rosenvinge	**Organization: GSFC**
Phone : 301-286-6721	**Email : tycho@milkway.gsfc.nasa.gov**

Failure Occurred During (Check one √)

 X Functional test   ☐ Qualification test   ☐ S/C Integration   ☐ Launch operations

Environment when failure occurred:

x Ambient   ☐ Vibration   ☐ Shock   ☐ Acoustic
☐ Thermal   ☐ Vacuum   ☐ Thermal-Vacuum   ☐ EMI/EMC

Problem Description

Upon first power-up of the board on 3/17/04, it was immediately noticed that the +3.4 V and +2.6 V supplies were not sourcing as much current as expected. +3.4 V supplies the Actel VCCI, as well as the oscillator and other logic on the board. +2.6 V supplies only the Actel VCCA. Here are the expected and actual currents on these two supplies (read on the power supply ammeter, with resolution to 1 mA):

+3.4 V   expect 34 mA   actual 9 mA
+2.6 V   expect 42 mA   actual 0 mA

An attempt was made to boot the flight code without success, and doing so caused no change in the power supply currents. The board was turned off. The board had been turned on for about 20-30 seconds.
The device that failed was an Actel RT54SX72S-CQ208BX3, LDC 0315, s/n 21654.

Analyses Performed to Determine Cause

Bob Baker, George Winkert, and Larry Ryan met this morning with Rich Katz, Goddard's Actel expert, to discuss the situation. He checked over our schematics and found nothing amiss. He looked at the board itself and was satisfied with he saw. He emphatically stated that this chip should have no problem with its I/O voltage (+3.4 V) coming up while its array voltage (+2.6 V) stays at ground, which is precisely what happened during the first power-up of this board. In fact, the chip was designed for just such an occurrence. He verified this fact yesterday with Actel. While that provides me some relief, the question now is, why does a chip that programmed successfully now appear to be totally dead? The part was submitted to failure analysis through Rich Katz to Actel. See attached failure analysis RT54SX72S-CQ208B, CASE NUMBER 1-6981277/ The analysis revealed an oxide pinhole in an N-channel transistor associated with an inverter circuit controlling the operation of a charge pump enable signal. It was concluded that an EOS event damaged the device. It appears that this was a part problem and was most likely shipped in this condition. Actel has instituted a check in their test program to verify that this condition does not exist in their devices prior to shipment.

Corrective Action/ Resolution

x Rework   ☐ Repair   X Use As Is   ☐ Scrap

Removed the failed device from HET FM2 on 3/24/04 and replaced with a RT54SX72S-CQ208BX3, LDC 0247, T25KS004, S/N 17599. Continued with board level testing. The board functioned nominally.

_____

Date Action Taken:__3/24/2005 **Retest Results**:__Success, board level and environmental tests.
Corrective Action Required/Performed on other Units ☐ Serial Number(s): ___n/a_____

	Closure Approvals

Subsystem Lead: _____ Date:_____

IMPACT Project Manager: _____ Date _____

IMPACT QA: _____ Date:_____

NASA IMPACT Instrument Manager: _____ Date:_____

From Larry Ryan, dated 3/19/2004, "HET FM2 Actel Failure"

A flight Actel RT54SX72S-CQ208BX3 FPGA was successfully programmed by Bob Baker & George Winkert using equipment in Bldg 23. Leads were formed by OSC, and the part was installed on the HET Electronics Flight Board #2. The board was installed in a known-good test setup. (The test setup had previously been used to test Flight Board #1.) The test setup includes Agilent laboratory power supplies all powered though an AC power strip, so all of the board supply voltages come up at about the same time.

Upon first power-up of the board on 3/17/04, I immediately noticed that the +3.4 V and +2.6 V supplies were not sourcing as much current as I expected. +3.4 V supplies the Actel VCCI, as well as the oscillator and other logic on the board. +2.6 V supplies only the Actel VCCA. Here are the expected and actual currents on these two supplies (read on the power supply ammeter, with resolution to 1 mA):

+3.4 V	expect 34 mA	actual 9 mA
+2.6 V	expect 42 mA	actual 0 mA

I attempted to boot the flight code without success, and doing so caused no change in the power supply currents. I then turned off the board. I estimate that the board had been turned on for about 20-30 seconds.

The incoming power supply voltages each go though an R-C low pass filter for bypassing. In the case of the +3.4 V and +2.6 V supplies, each has a 1.0 ohm series resistor and two capacitors, a 47 uF tantalum and a 0.1 uF ceramic, to ground. I performed continuity checks on the board and discovered that the 1.0 ohm series resistor for the +2.6 V supply was not installed. Both the assembler and I missed this in our inspections of the board prior to initial power-up. The result is that the +2.6 V power plane had no DC connection to the power supply, though it was AC connected to ground via the 47 uF capacitor and a total of ten 0.1 uF ceramic capacitors (including the VCCA decouplers at the Actel itself).

We installed the missing 1.0 ohm resistor, and upon subsequent power-up, the supply currents still were not correct. Here is what I measured:

+3.4 V	expect 34 mA	actual 4.5 mA
+2.6 V	expect 42 mA	actual 0.6 mA

(This time I measured the current more carefully, by measuring the voltage drop across 1.0 ohm series resistors.) Note that the oscillator is taking at least some, if not most, of the +3.4 V current. So I don't know how much is actually flowing into the Actel.

_____

I tried booting the flight code, again to no avail and with no change in power supply current.

Probing the appropriate Actel pins where they are attached to the body of the part, I verified the following:

All VCCI pins are receiving +3.4 V
All VCCA pins are receiving +2.6 V
All ground pins have continuity to the power return (checked later with power off)
The clock input pin is receiving the 32 MHz clock from the oscillator
The two reset inputs (command reset and power-up reset) are in their inactive states

I probed the two clock output test pins and found neither of them clocking. Both appear to be pulled up with a very weak drive. When I probed them with a 10 Mohm multimeter or scope probe, they read a few tenths of a volt, with no clocking observed. When I probed them with a 10 Gohm multimeter (HP 34401A), they read 3.3 V and 3.0 V, respectively.

Next, I separated the power supplies so that I could have a bit of control over the timing of when they come on. I tried powering up +2.6 V a fraction of a second before +3.4 V. I noticed on the power supply ammeter that the +2.6 V supply did show some current during the moment that it was on and +3.4 V was off. However, when the +3.4 V came up, the +2.6 V current dropped back to zero (actually, 0.6 mA). I powered down and tried again, this time with a bit more time between the power-up of +2.6 V and +3.4 V (perhaps one second). I saw the +2.6 V current rise to 40 mA before +3.4 V was turned on. It dropped back to 0.6 mA when the +3.4 V supply came up.

That was the extent of testing that I have performed on the board.

Bob Baker, George Winkert, and I met this morning with Rich Katz, Goddard's Actel expert, to discuss the situation. He checked over our schematics and found nothing amiss. He looked at the board itself and was satisfied with he saw. He emphatically stated that this chip should have no problem with its I/O voltage (+3.4 V) coming up while its array voltage (+2.6 V) stays at ground, which is precisely what happened during the first power-up of this board. In fact, the chip was designed for just such an occurrence. He verified this fact yesterday with Actel. While that provides me some relief, the question now is, why does a chip that programmed successfully now appear to be totally dead?

To that end, he is lending us his action probe, which will allow us to probe up the chip in situ and look at the internal nodes. He requested that we begin by trying to trace the clock where it enters the chip and goes through a divide-by-5 stage. We will begin that testing this afternoon or Monday.

_____

X-Sender: rkatz@mail.klabs.org
Date: Wed, 13 Oct 2004 12:50:15 -0400
To: Lillian Reichenthal <Lillian.S.Reichenthal@nasa.gov>
From: rk <rkatz@klabs.org>
Subject: Re: IMPACT Actel issues
Cc: rk@klabs.org, rbarto@klabs.org, ikleyner@klabs.org

Hi Lil,

I was up at Actel this week and we went through the status of the failure analysis. Thank you for your patience, these guys are working hard. This is for the part that failed in Building 2 and looked like it was just all dead.

Dug into their first results of the parts passing DC I/O testing. This didn't make sense based on our lab results so we reviewed all of the tests that were done. This Actel quick-look test is very quick-look and doesn't test all of the parameters. It should have failed Voh/Vol testing, for example. But that wasn't run so the pass for that analysis step is now understood.

Now, my initial thought on this was that it looked like that the charge pump was not running. We have never seen any of those fail, unless killed by radiation. That's why we had Actel write that special routine to see if the "p-fuse" was programmed which enables the charge pump. the software said that it was programmed but it could have been an in between value.

the actel engineers analyzed the divide-by-five circuit that was being used to demonstrate the problem. no lockup states. so we're in agreement there that there's not a logic problem.

electrically probing the input cell gave us a bad result. however, and it's not documented (either well or at all) that the probe points for this family were deleted after the input cell. the software lets you think you are probing them. so now we have those funky values explained.

there are a number of over ride modes that the factory people can use to turn the charge pump on and off. when these were utilized the part started up just fine. so our initial hypothesis of no charge pump running is correct.

next they checked the p-fuse using a technique called the "manual fuse checker." this is a better test then what we ran at GSFC. the p-fuse and the j-fuse both passed this.

going through the chip's schematics, we can say where the failure is not. thus, it can be concluded at this point that there was no board level application issue for STEREO, there was no programmer issue, and the design of the device's logic was not implicated. so this gives you a clean bill of health. for the most part!

we still have to determine root cause and chase that down. so we went through the device schematics and were discussing probe points. "FIB pads" will have to be put down to explore this further. This is what we did for the CalTech design where they programmed the security fuse and therefore we could not use the device's diagnostic's features. This is not a zero risk thing but it is routinely done. So, we will continue until we find the failing structure.

Just wanted to keep you up to date with regards to this failure analysis.

Cheers, RK

Actel

2061 Stierlin Court
Mountain View, CA 94043-4655
650-318-4200

FAILURE ANALYSIS REPORT FOR DEVICE TYPE
RT54SX72S-CQ208B
CASE NUMBER 1-6981277

Prepared for

Goddard Space Flight Center
National Aeronautics and Space Administration
(NASA GSFC)

April 15, 2005

BY

Don Kinell
Khoi Tran

Failure Analysis Group

1.

CASE NUMBER   **1-6981277**   **DATE: 4/15/05**

CUSTOMER: **Goddard Space Flight Center**
National Aeronautics and Space Administration
(NASA GSFC)

2. DEVICE TYPE: RT54SX72S-CQ208B

WAFER LOT #:   **T25KS008**   **DATE CODE: 0315**

DESIGN NAME: **cpu24actel.adb**

NUMBER OF UNITS: **One Unit, Serial Number 21654**

TO: **Richard Katz (rkatz@klabs.org)**
Head, Office of Logic Design

CC: **Dan Elftmann, Werner van den Abeelen, Minal Sawant, Mo Mawla, Khoi Tran, Raj Kamdar**

FROM: **Don Kinell**
Khoi Tran
Failure Analysis Group

REASON FOR FAILURE ANALYSIS

NASA reported a functional failure on one RT54SX72S-CQ208B device. In particular, NASA observed no activity on the output pin #189 of the FPGA. This pin is the output of a "Divide By Five" counter circuit that takes a 32 MHz input on pin #174 (*tclk_in*) and generates a 6.4 MHz on output pin #189 (*eclk_out*). NASA also observed no activity on the internal nodes of the FPGA using the Silicon Explorer. The device was sent to Actel for further analysis.

_____

EXECUTIVE SUMMARY

NASA reported a functional failure on one RT54SX72S-CQ208B device. In particular, NASA observed no activity on output pin #189 of the FPGA. This pin is the output of a "Divide By Five" counter circuit that takes a 32 MHz input on pin #174 (*tclk_in*) and generates a 6.4 MHz on output pin #189 (*eclk_out*). NASA also observed no activity on the internal nodes of the FPGA using the Silicon Explorer. The device was sent to Actel for further analysis. The returned device was tested using Actel's Post Programming Test (PPT) that checks for shorts/open continuity, standby Idd and tri-state leakage failures. The returned device passed the PPT test indicating that the returned device had no DC parametric type of damage.

Using the Silicon Explorer II tool, Actel was able to observe the reported failure mechanism. Next, Actel performed analysis on the "Divide By Five" circuit to see whether the circuit could be stuck at any legal state that could cause the observed failure. The analysis found no design related problem indicating the "Divide By Five" circuit was properly designed. Further examination of the failure signature, (no activities at internodes and tri-stated outputs), suggested that the observed failure may be due to the charge pump not running. To check the status of the charge pump, Actel wrote a test program to command the charge pump and was able to make the returned device work correctly. This technique confirmed the charge pump was not running due to the charge pump enable signal, *PMPEN* not being in the right logic state. Since the state of *PMPEN* is controlled by logic from the *FUS_BLK* circuitry, FIB (Focus Ion Beam) pads were added to selected locations within the *FUS_BLK* to observe their logic states. Measurements found one logic gate within this circuitry (NOR gate *U8*) to be at the wrong logic state, thus preventing the charge pump from turning on. Further measurements gave an indication of a short to V_{CCA} from the output of the NOR gate. De-processing was then performed to find the actual failure site. The de-processing steps were performed with removal of one layer at a time with measurements made at each step to find where the short or other failure mechanism may be. Following the removal of the top layer metal, the V_{CCA} short was no longer observed as this layer contained the V_{CCA} metal interconnect. Suspecting that the observed short was related to the FIB process having to penetrate through the V_{CCA} layer, de-processing was continued to examine for other possible defects.

Following removal of all metal interconnect layers, leaving only poly-silicon and contact metals. Before removing the poly-silicon layer a PVC (Passive Voltage Contrast) examination was implemented. This is a test in which low energy electrons are used to image the unit. If the poly-silicon is floating electrically it will charge up with a display that is a different image from a poly-silicon gate that is shorted to the substrate. It was observed at this step a possible short between the poly-silicon on the n-channel transistor in FUS_BLK inverter U4. Subsequent de-processing to silicon confirmed a pin-hole in the gate oxide, thus the source of failure. This short was likely loading down the input signal, VSVRDETB, leaving the inverter output in an intermediate voltage level insufficient to provide a logic low to the following NOR gate stage. This prevented the signal FUS3 from reaching a logic high state and thus the charge pump was disabled resulting in the observed functional failure. The cause of failure is most likely an EOS event on the V_{CCA} voltage supply.

_____

1. <u>VISUAL INSPECTION</u>

The Failure Analysis Group received one RT54SX72S-CQ208B device in the following physical condition (**Figure 1 and Figure 2) on April 28, 2004:**

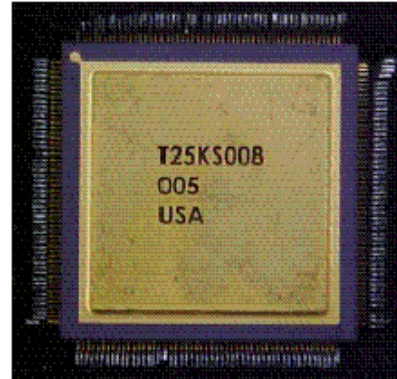**Figure 1: Top View of Returned Unit**

Figure 2:   Bottom View Of Returned Unit

A detailed visual inspection of the unit showed that all the pins were bent. On April 28, 2004, the returned device was sent to an outside laboratory to have it manually soldered onto a CQ208 lead frame (ceramic quad flat pack with 208 leads) for further testing. On May 4, 2004, Actel received the reworked device (Figure 3 and Rework **Figure 4) in the following physical condition:**
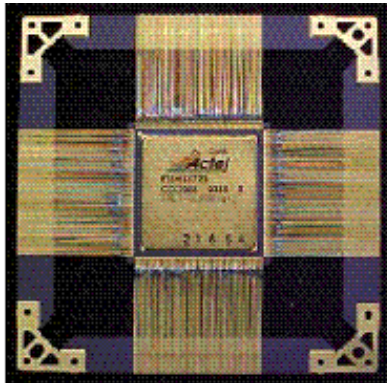
Figure 3: Top View Of Device After Rework
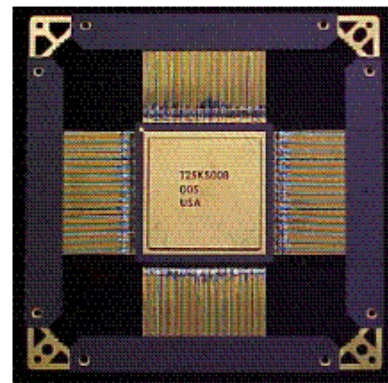
Figure 4: Bottom View Of Device After Rework

A visual inspection of the device following package rework showed that all the leads were properly soldered to the lead frame.

1. DC PARAMETRIC VERIFICATION

The returned device was tested using Actel's Post Programming Test (PPT) that checks for shorts/open, continuity, standby I_{dd} and tri-state leakage failures. The returned device passed the PPT test indicating that the returned device had no DC parametric type of damage.

2. FUNCTIONAL TEST WITH SILICON EXPLORER

Following the receipt of the design file and the test bench setup from Actel's Applications Consulting Group, the returned device and a reference device were mounted on an Actel test board one at a time and subjected to the functional test using the given bench setup information This test applies a clock signal to input pin #174 and measures the frequency at output pin #189. The frequency of output pin #189 should be equal to the frequency applied to the input pin #174 divided by 5. Also, to

observe the internal nodes of the returned device, a Silicon Explorer II test unit was connected to the load board via the JTAG pins. Silicon Explorer II is an Actel tool that enables real-time observation and analysis of the device internal logic nodes, using the probe circuit designed into the architecture. Two internal output nodes of the logic modules can be accessed simultaneously at any given time using the probe A and probe B pins. **Figure 5** illustrates the state machine of this "Divide By Five" circuit. The output *eclk_out* is the inverse of the second bit (highlighted in red) of the three-bit counter.
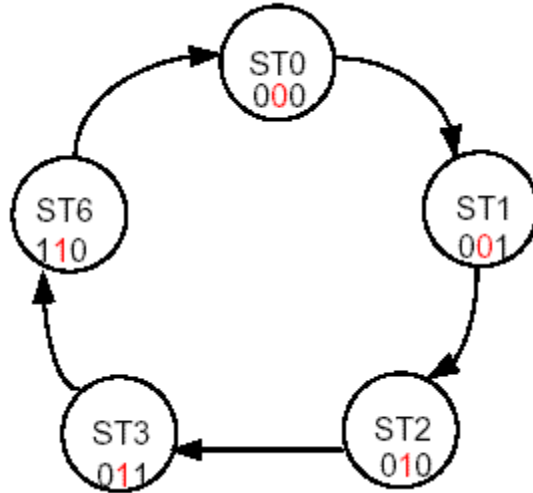
Figure 5:   The State Machine of The "Divide By Five" Circuit

Figure 6 below shows the logic circuit of the "Divide By Five" Counter.
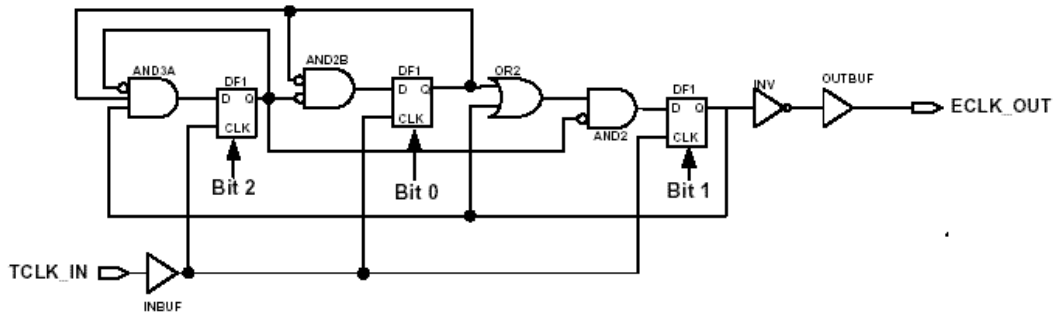
Figure 6: Circuit of the "Divide By Five" Design

To determine if there are possible illegal states in the "*Divide By Five*" circuit an analysis of the design was performed and it was found that the circuit would not lock up. Illegal states (100, 101, and 111) will be cleared in the first cycle.

Actel was able to observe the reported failure mode using the Silicon Explorer. The internal nodes of the "Divide By Five" circuit (**Figure 6**) and the output pin #189 showed no activity, while the internal nodes and output pin #189 of the reference device toggled as expected. Output pin #189 of the returned device was verified to be tri-stated using a 10 K pull-up resistor connected to V_{cci} Shown in **Figure 7** are scope plots of signals on input pin #174 and output pin #189 of the FPGA.
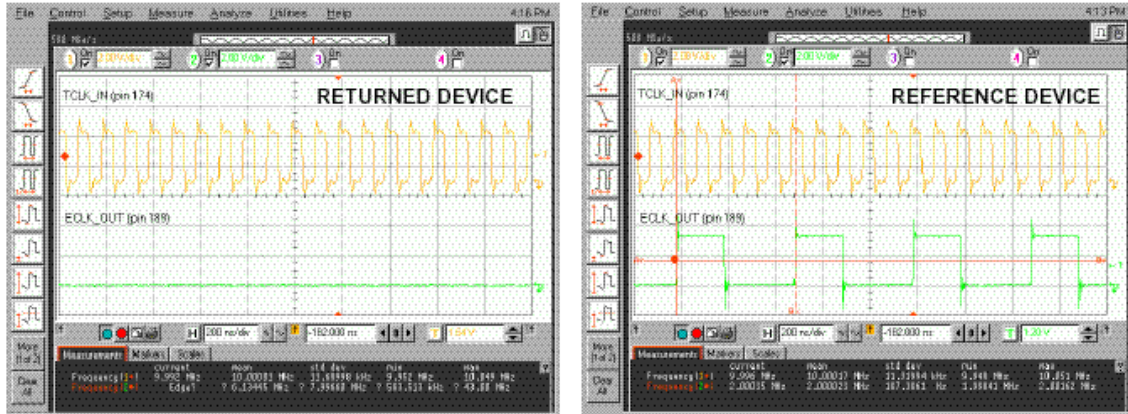
Figure 7: Scope plots of the output signal eclk_out (pin 189) with respect to the input signal

3. CHARGE PUMP TESTING RESULTS

The observed failure is most likely caused by the charge pump not running. This is based on the observed symptoms of the internal nodes showing no activities, and the external outputs being tri-stated. If the pumped voltage is not reaching the right level, the controller will fail to output the correct global controlled signals as indicated in Figure 8. As a result, input signals cannot propagate into the core of the FPGA and all outputs will be tri-stated.
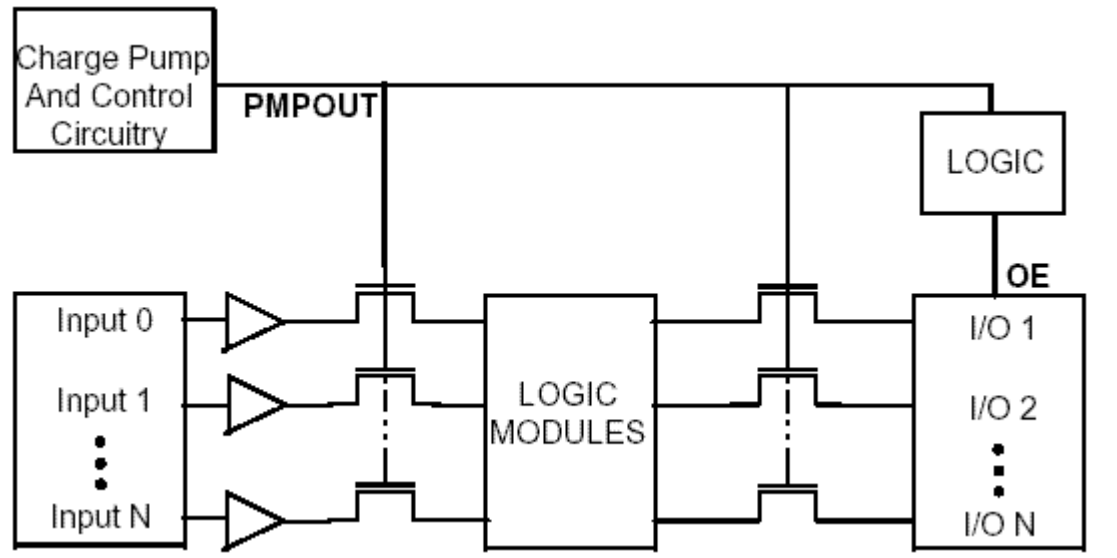
Figure 8: Charge pump and global control signals of an Actel FPGA

Determining the status of the charge pump is thus a necessary step in order to narrow down the failure to a single transistor. To verify the state of the charge pump, a program to modify device internal control registers was generated. This program turns the charge pump on or off by setting certain register bits in the device mode register. With this program, Actel was able to turn on the charge pump and thus the returned device began functioning correctly. In particular, the "Divide By Five" circuit started generating the correct output signal. As shown below in Figure 9 the signals of input pin #174 and output pin #179 of the two devices is the same when using the test program to turn on the charge pump.

STEREO IMPACT

Figure 9: Scope plot of the output signal eclk_out (pin 189) of the returned device (LEFT) is identical to that of the reference device (RIGHT) when the charge pump is turned on by the test program

Since the output signal *eclk_out* **(pin #189) of the returned device functions correctly when the charge pump is enabled through software this indicates there is a problem in the circuit that controls the charge pump. Analyzing the FPGA transistor circuit, it is found that the charge pump enable (***PMPEN***) signal is controlled by signal *MR22* (Mode Register bit 22) and signal *FUS3*. Figure 10 below shows the simplified circuit generating the *PMPEN* signal.**

Figure 10: Circuit generating the PMPEN (pump enable signal)

According to **Figure 10**, *PMPEN* **is asserted (HIGH) only when** *MR22* **and** *FUS3* **are at different logic levels. For instance,** *PMPEN* **is asserted only when** *MR22* **is at logic HIGH and** *FUS3* **is at logic LOW or vice versa, an XOR function.**

4. MANUAL FUSE CHECK

The findings and analysis above indicated that signal *FUS3* **is likely in the wrong state. To determine the source of this incorrect state, the schematic of Figure 11 was examined. As shown in the figure, the** *FUS3* **signal is dependent on signals** *SFUS*, *PFUS*, *JFUS* **and** *VSVRDETB*. **Any changes in the states of these signals would result in a change in the state on the** *FUS3* **signal. The next step to narrow down the failure was to check the statuses of the** *PFUS* **and the** *JFUS* **by performing the in-house tool MANUAL fuse-check that addresses a specified antifuse. A single 1V magnitude pulse and duration of 250 ns is applied to the VPP pin of the device through a 120Ω resistor as illustrated in Figure 12. By measuring the voltage across the 120Ω resistor, the programming path resistance, which includes the antifuse resistance, can be determined. If an antifuse is damaged such that the path resistance increases significantly, the voltage drops across the 120 resistor will be smaller than that of a reference.**
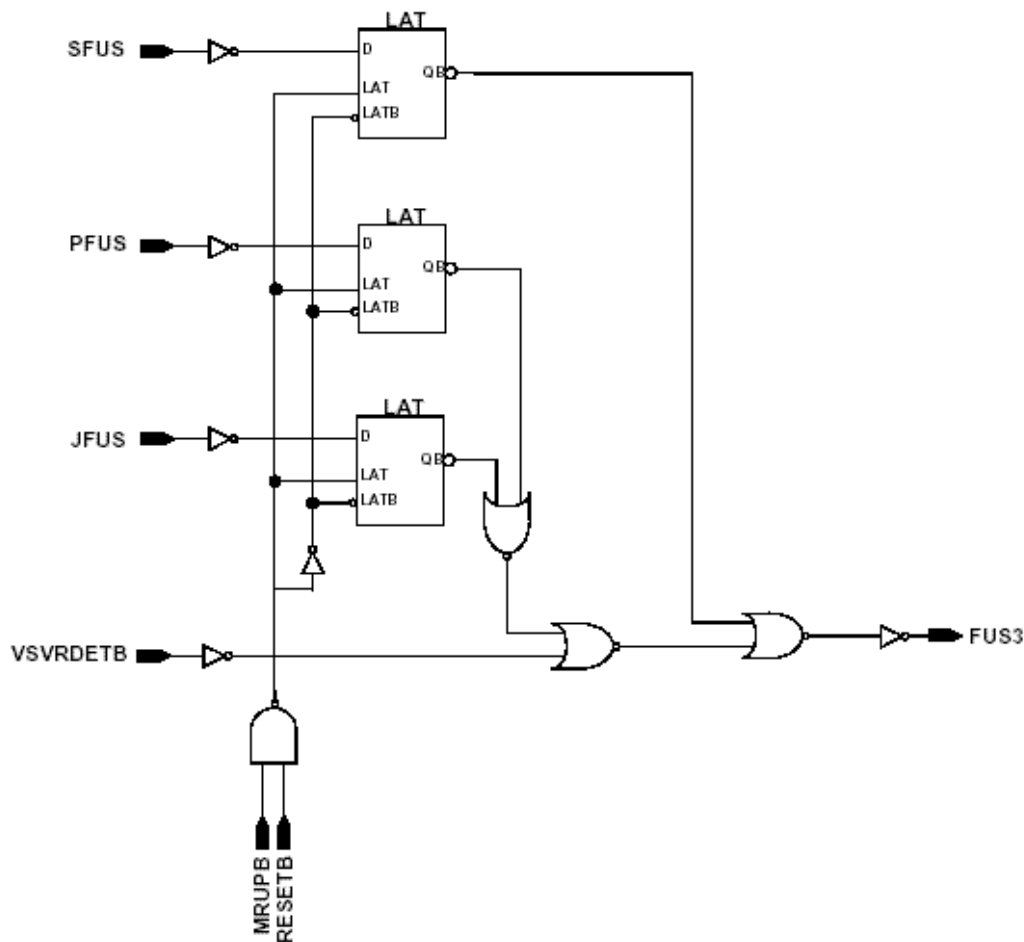
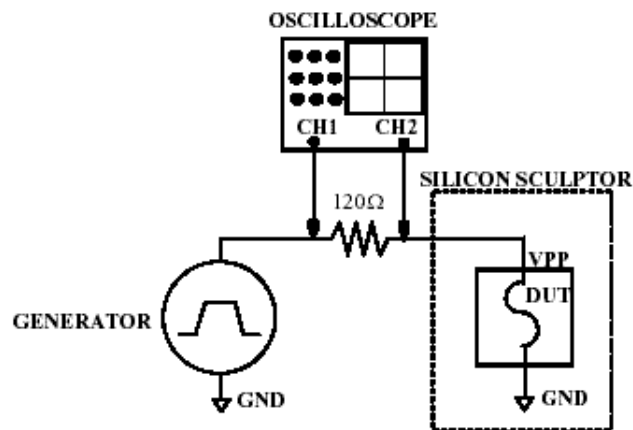**Figure 11: Logic circuit generating the FUS3 signal**

Figure 12: Setup for performing manual Fuse-check

The results of the MANUAL fuse-check test on antifuse J and antifuse P showed no high resistance, indicating that the two antifuses were not damaged.

STEREO IMPACT

5.   FIB PAD ADDITION AND MICRO PROBING RESULTS

To further narrow the failure to a logic module, the charge pump control circuitry was analyzed thoroughly and FIB (Focus Ion Beam) pads were added to selected locations to observe their logic states. **Figure 13** below shows the locations of the added FIB pads. A choice of *Accurel Systems International* was made for the addition of FIB pads as they have the capability to accept relevant Actel design files from which Accurel will overlay the image of the device. This overlay plus the provided coordinates of the desired FIB pad location allows Accurel to accurately position the desired FIB pad.
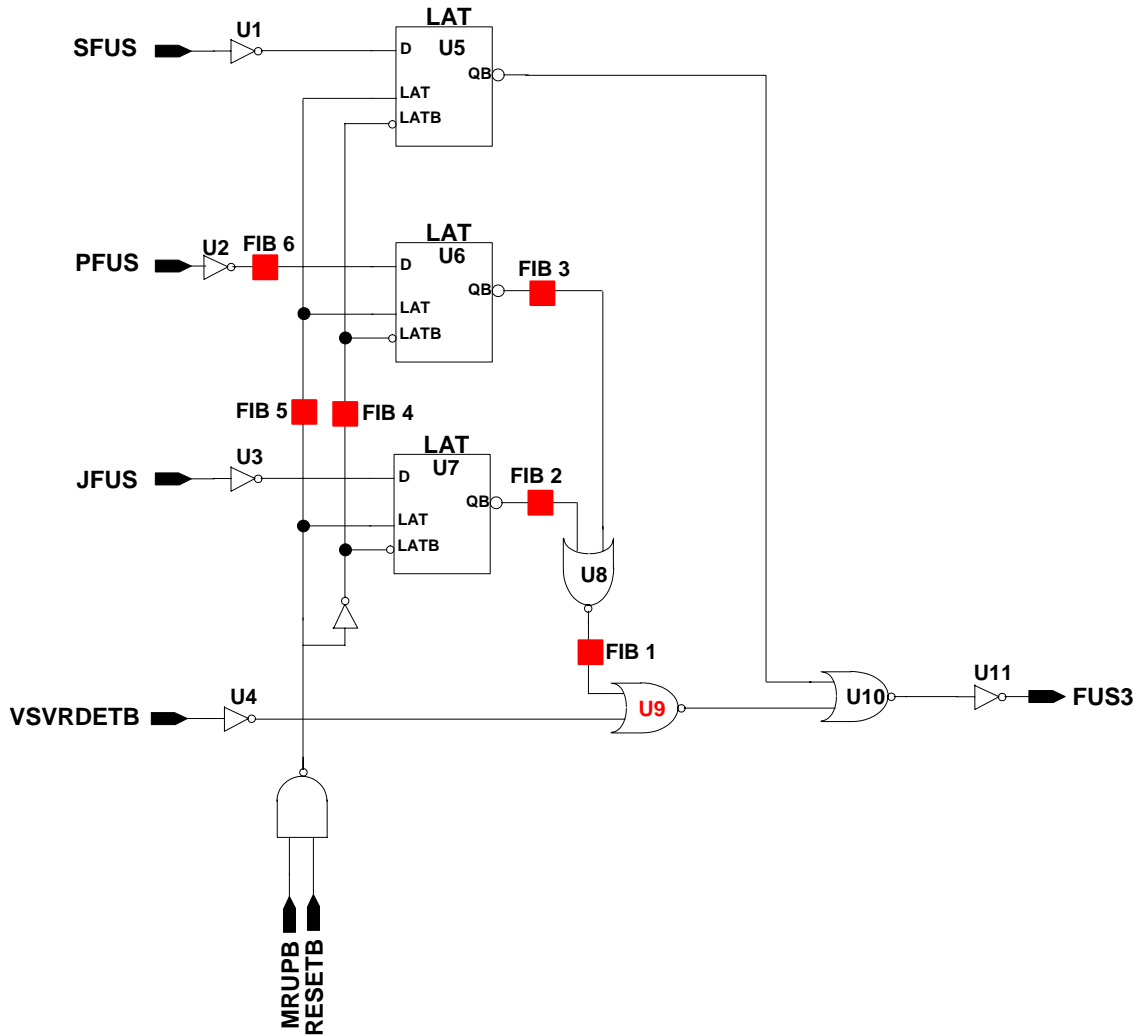
Figure 13: *Locations of the FIB pads within the FUS_BLK Circuit*

According to the architecture specification of the RT54SX72S product, a functional device should have the signals *PFUS, JFUS*, and *VSVRDETB* at logic HIGH and the signals *MRUPB*, and *RESETB* at logic LOW.   Therefore, FIB 1, FIB4 and FIB 6 should be at logic LOW, and other FIB pads should be at logic HIGH as shown below in **Table 1**.

FIB Number	Correct Logic State
FIB1	LOW

FIB2	HIGH
FIB3	HIGH
FIB4	LOW
FIB5	HIGH
FIB6	LOW

Table 1: *Correct logic states for FIB pads*

The logic levels of FIB2, FIB3, FIB4, FIB5, and FIB6 in the returned device and the reference device were measured to be identical. However, FIB1 in the returned device was measured to be in an incorrect logic state. **Table 2** shows the summary of the these measurement

FIB Number	Reference Device	Returned Device
FIB1	LOW	*** HIGH ***
FIB2	HIGH	HIGH
FIB3	HIGH	HIGH
FIB4	LOW	LOW
FIB5	HIGH	HIGH
FIB6	LOW	LOW

Table 2: Measured logic levels of FIB1 to FIB6 in the returned device and the reference device

FIB2, FIB3, FIB4, FIB5 were electrically probed and the curve results showed a good I/V characteristic indicating that U3, U2, U6, U7 and U8 were functional. Figure 14 on the left below shows the I/V curve that was performed on these pads. The curve result of Figure 15 however reveals a short between the output of NOR gate U9 and V_{CCA}.
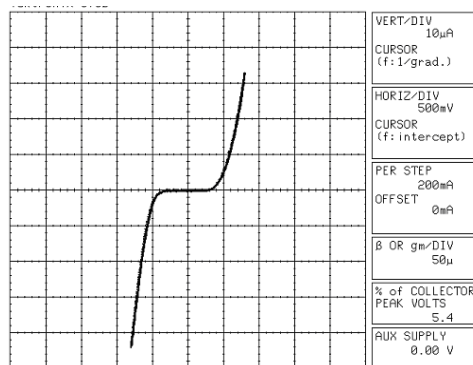
Figure 14: *I/V characteristic of FIB2, FIB3, FIB4, FIB5 and FIB6*
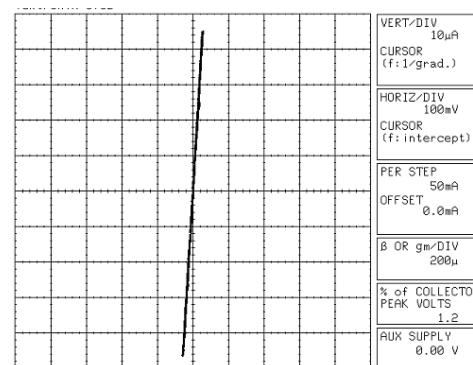
Figure 15: I/V Characteristics of U9 (NOR gate) shorted to V_{CCA}

6.   DE-PROCESSING

Based on all the observed measurements pointing to a possible short within the *FUS_BLK* circuit, a decision was made to proceed with de-processing in the region of *NOR gates U8, U9* in order to locate the specific fault site and thus determine root cause of the failure. De-processing removes one processed layer at a time followed by optical and SEM imaging for possible regions where there may be a short or any other defect. Additional steps for verification of the fault included application of additional FIB pads with subsequent electrical measurements. A choice of *Riga Analytic Labs* was made for the de-processing activities as this lab has previously demonstrated excellent skills at layer removal without damaging the device under analysis. A first step at Riga is a die examination for any obvious gross level defects. From the photo shown below in
Figure 16 the surface does not exhibit any surface scratches or contamination.
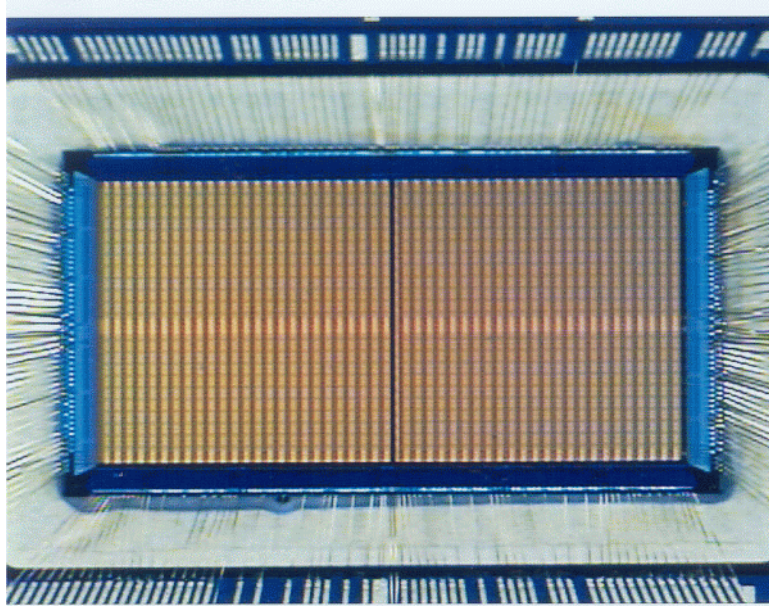
STEREO IMPACT

Figure 16: NASA unit as Received by Riga Labs

The next action by *Riga Analytic Labs* **was to examine the region where FIB pads 1-6 were placed. The 6 pads are shown below in Figure 17 where 1000x magnification of the FUS_BLK section is shown.**
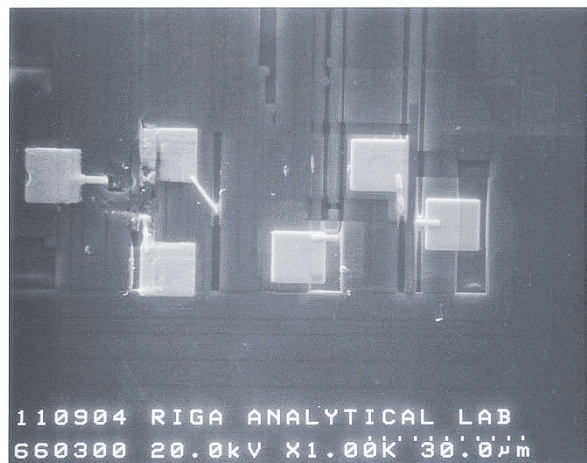

Figure 17: Original 6 FIB Pads

Further examination of the FIB pads on the left side of Figure 17 revealed possible surface damage resulting from the first application of FIB pads and subsequent micro probing. This damage may have resulted in the earlier indication of a short between V_{CCA} and the output of *NOR gate U8***. This possibility was further confirmed in examination of the device layout where it was observed that a V_{CCA} metal layer is present in the FIB area along with a V_{SV} metal interconnect line. Shown magnified below in Figure 18 are FIB Pads 1-3 indicating possible corruption of metal layers. As a result of this observation a decision was made to remove the top metal layer followed by addition of a new FIB pad to determine if the FIB1 to V_{CCA} short was still present.**
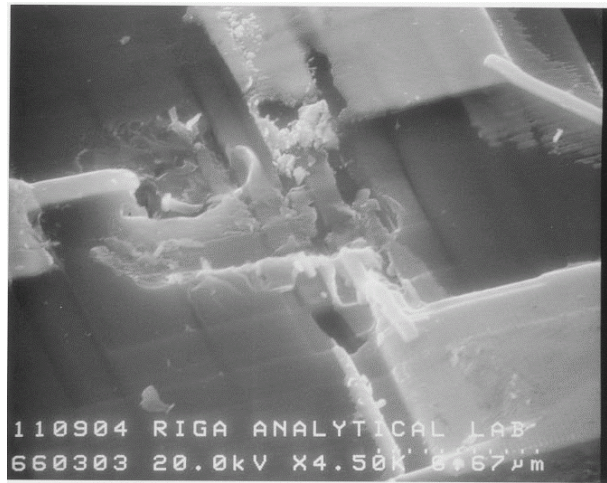
Figure 18: Possible FIB Pad damage

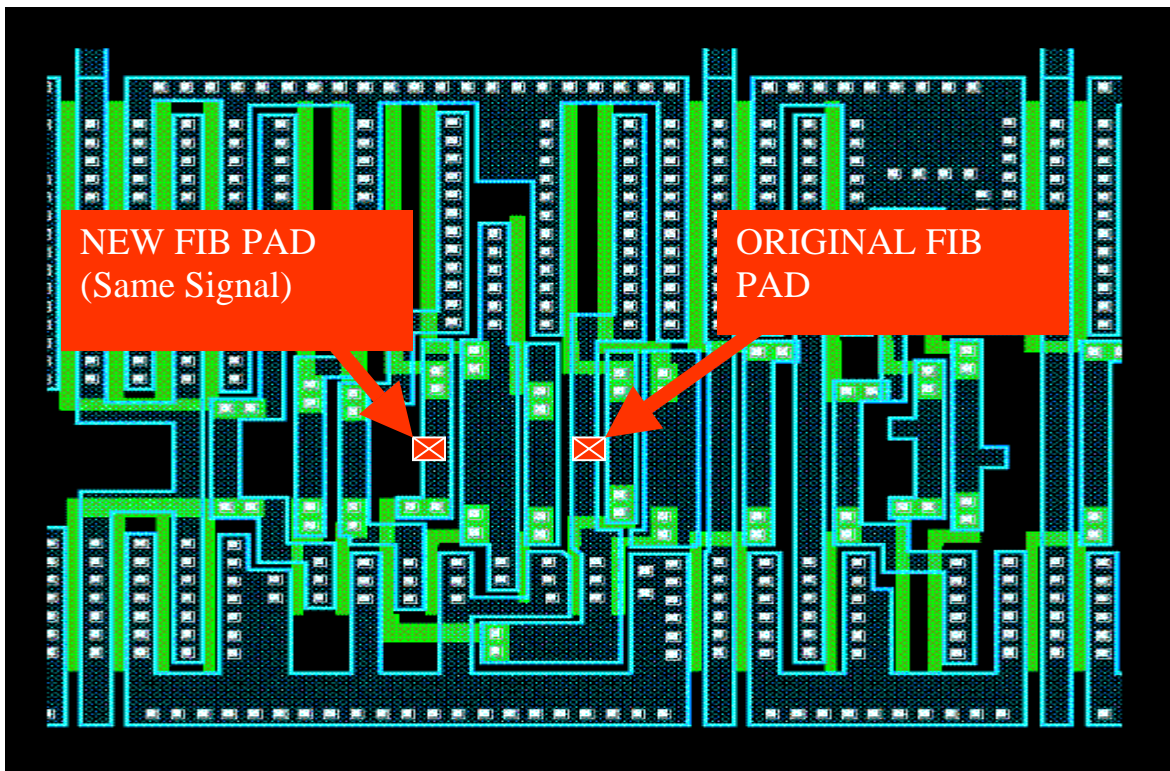**Placement of new FIB pad following removal of top Metal layer 4 is shown below in Figure 19.**

Figure 19: New FIB Location

The new FIB pad added by Riga as shown in **Figure 20** is electrically the same as the original FIB1 shown in **Figure 13** as it is connected to the original FIB1 via a poly silicon line and Metal 1. Subsequent micro probing of this FIB connection to U9 no longer indicated a short to V_{CCA} as indicated in the curve trace photo shown below in **Figure 21** thus providing additional evidence that the short originally measured was a FIB related short.

STEREO IMPACT
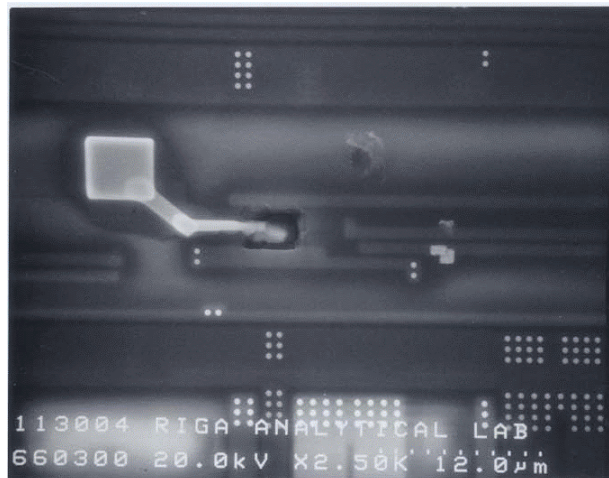
Figure 20: Secondary FIB1 Pad to NOR GATE U9
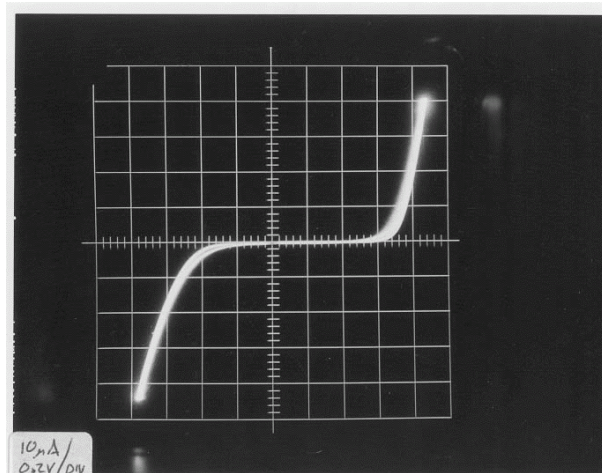

Figure 21: Curve Trace of Secondary FIB1 to V$_{CCA}$

Since a short was not found after top level Metal 3 was removed a decision was made to place 3 additional FIB pads in the *FUS_BLK* circuit in order to investigate other possibilities for the observed failure. These are:

FIB "A" -- Inverter U4 input

FIB "B" -- NOR Gate U9 Output

FIB "C" -- NOR Gate U10 output

The physical locations of these FIB pads are shown in the micro photo shown below in **Figure 22**. The additional unlabelled FIB pad shown in the figure is the FIB1 replacement discussed above.
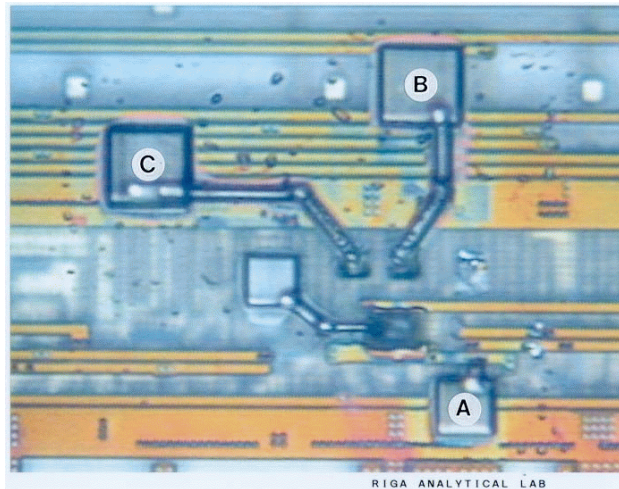
Figure 22: Surface Location of FIB Pads A, B,& C (Metal 3 Removed)

To examine for faults at these locations, micro probing was performed with measured results indicating good I/V characteristics, similar to the results of the secondary FIB shown in **Figure 21.**

7.   Additional De-processing – Metal Layers M3, M2, and M1

Following secondary micro probing operations, a decision was made to continue de-processing down to metal layer M1. Here the sample was mechanically lapped and at each level the area of interest was inspected for defects or damages and none were found. At the M1 layer, a Passive Voltage Contrast (PVC) test was performed to examine for any poly silicon shorts. This is a test in which low energy electrons are used to image the unit. If the poly-silicon is electrically floating it will charge up with a contrasting bright image display that is a different image from a poly-silicon gate that is shorted to the substrate. During the test the M1 lines that have source/drain contacts appeared dark (grounded). The Metal 1 lines that are connected only to poly gates appeared bright (floating) except for one gate. The dark poly silicon line shown below in **Figure 23** is connected to the N-channel gate input of Inverter U4 (FIB "A") shown in **Figure 13**. This dark poly silicon indicates a possible leakage to the under laying substrate.
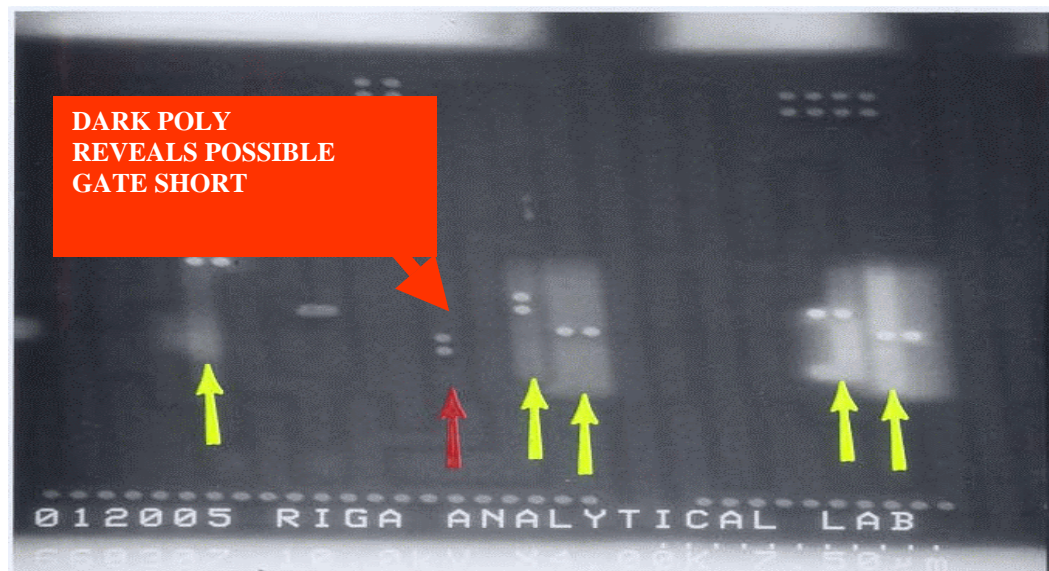

Figure 23: PVC Test Reveals Evidence of Gate Short

Next the sample was lapped through the M1 layer to the contact level where the PVC test was repeated. At this level contacts to the poly silicon are exposed with all metal layers now removed. Close examination as shown in Figure 24 revealed two poly contacts to the N-Channel gate input of Inverter U4 that were dark.
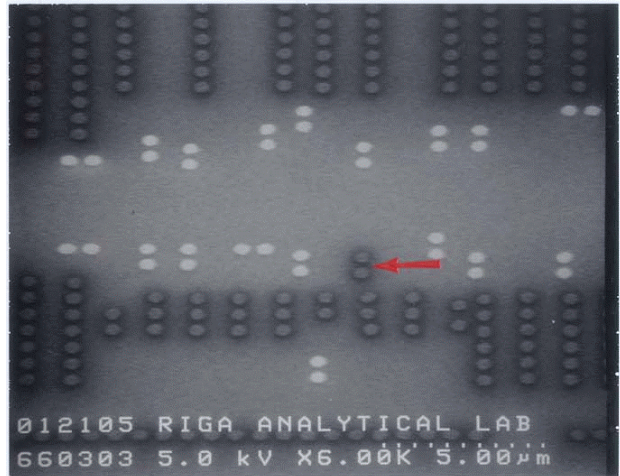

Figure 24: Anomalous Poly Contacts to U4 Inverter

De-processing continued with the failed unit sample mechanically lapped to the poly level and a final voltage contrast test was performed at this level. As shown in Figure 25 the gate corresponding to the dark contacts, as observed in previous PVC tests, appeared dark. This indicates that the gate has leakage or is shorted to the substrate.
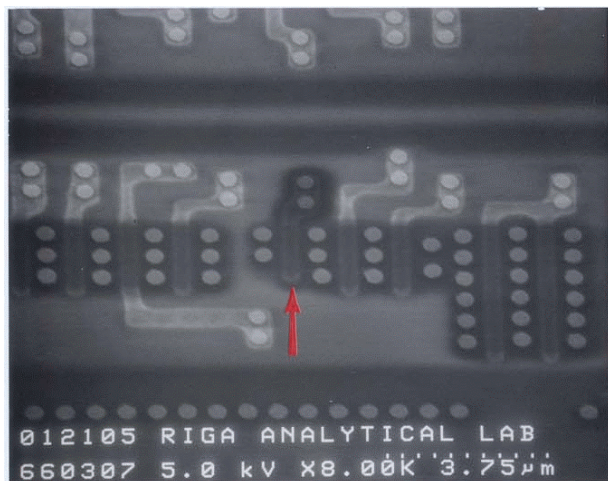

Figure 25: Detailed View of N-channel Gate to U4

Following removal of the poly level an inspection of the region where the anomalous gate was observed revealed a crack in the field oxide region between a source/drain contact and the poly sidewall. In addition, gate oxide damage was observed near the lower edge of the gate. These transistor damages are shown in the photos of Figure 26 and Figure 27.

STEREO IMPACT

CRACK REVEALS DAMAGE

GATE OXIDE DAMAGE

Final De-processing stripped all oxide to the silicon level. As shown below in Figure 28 a small pinhole at the poly edge of the N-channel transistor of Inverter U4 exhibits a small pinhole.
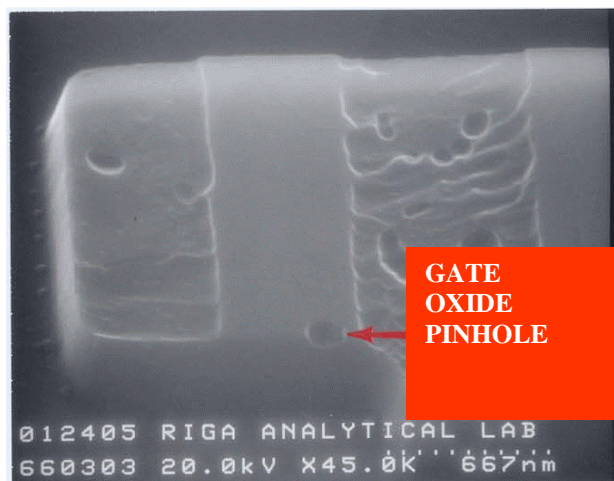

GATE OXIDE PINHOLE

Figure 28: N-Channel of U4 Gate Damage

STEREO IMPACT

8.   CONCLUSIONS

Based on the results of the FA investigation, it is concluded that this unit failed due to an EOS event that damaged the N-channel transistor of Inverter U4. This inverter has as its input, signal *VSVRDETB* that normally would be at logic level High. Thus if this signal is virtually stuck low by the n-channel input gate fault the signal *FUS3* will no longer be at Logic High and the charge pump will turn off.

9.   RECOMMENDATIONS

Because of EOS events of this type, it is recommended that close attention be applied to power supply spikes that may occur during device programming or system operation.

To screen for this type of EOS event if it occurs during Sculptor programming, Actel is to release a revision to the Sculptor software (v4.52.03.89), which is planned for May 24, 2005. The revision will include programming an unused Silicon Signature Bit, (*SSIG2, Bit0*) allowing a test of the *VSVRDETB* signal controlling *FUS3,* which in turn enables the charge pump to be activated. This test will fail if the *VSVRDETB* signal is in a stuck high or low condition and will also fail if the output of logic gate U8 following the path of the PFUS and JFUS signals shown in **Figure 13** is stuck high or low. This new test would have discovered an inoperable *VSVRDETB* signal resulting from the EOS event if the EOS event had occurred during Sculptor programming.

Actel is committed to providing the best support and solutions. Please feel free to contact Actel technical support or me if there are any questions or concerns. Thank you for your patience and support.

Sincerely,

2.1.1 Don Kinell

2.1.2 Khoi Tran
Failure Analysis Group

2.1.3 Actel Corporation