STEREO IMPACT

PROBLEM REPORT
PR-3001
Walpole
4/29/04

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SIT	**SubAssembly : SIT Energy Board**
Component/Part Number: Amptek PH300RH	**Serial Number: S/N 01**
Originator: Walpole	**Organization: UMd**
Phone : 301-405-4517	**Email : wapole@umd.edu**

Failure Occurred During (Check one √)

X Functional test ☐ Qualification test ☐ S/C Integration ☐ Launch operations

Environment when failure occurred:

X Ambient ☐ Vibration ☐ Shock ☐ Acoustic
☐ Thermal ☐ Vacuum ☐ Thermal-Vacuum ☐ EMI/EMC

Problem Description

During initial functional testing/trimming of the newly-built SIT Energy Board S/N01 (=FM1), it was noted that the peak detector output of the low-gain channel was small and did not change when the input level was changed. The output of the high-gain channel behaved normally. Signal tracing on the board revealed normal operation of all circuits until the peak detector, an Amptek PH300RH hybrid, was reached. It had correct input, but incorrect output. The part designation is U4.

Analyses Performed to Determine Cause

The power supply for the test setup was checked and voltages were found to be correct. Substituting the energy ETU board for the flight SN01 verified that the test setup was not at fault. Substituting the flight SN02 board verified that the board design was not at fault. All components surrounding U4 were checked and found good and the currents drawn by the chip were within expectations and identical to those on the other channel.
Conclusion: a fault within the PH300 chip, probably in the input gate. The part was submitted to failure analysis. Chip is PH300RH, D/C0224, S/N 1351, from Amptek Inc., 6 De Angelo Drive,Bedford MA, 01730. Tel 781-275-2242. Purchased by UC Berkeley, PO# 1-0000601778.

On June 9, 2004, a FRB review was held to discuss the failure of an analog peak hold detector manufactured by Amptek, part number PH300RH, LDC 0224, S/N 1351. "Evidence of electrical overstress (EOS) damage in the metallization and silicon substrate associated with Pin 1 (IN)" was the conclusion given by the failure analysis report. The report also suggests the possibility of an "ESD event preceded the EOS failure." The failure site was located near an unprotected bond pad connected directly to Pin 1. The reviewers in the parts analysis group recommended EXTREME CAUTION during the handling and installation of the PH300 hybrid. Reference failure analysis Report Q40139FA.

Corrective Action/ Resolution

X Rework ☐ Repair ☐ Use As Is ☐ Scrap

The cause of the problem was most likely ESD to an unprotected pin, and PH300RH, LDC 0224, S/N 1351 U4 was replaced with LDC 0224.. Extra care was used on the device during handling due to the unprotected input.

Date Action Taken:_____6/11/2004_______ **Retest Results**:__Success at board level test ____

STEREO IMPACT

Corrective Action Required/Performed on other Units ☐ Serial Number(s): ___n/a_____

Closure Approvals

Subsystem Lead:	________________________	Date:____________
IMPACT Project Manager:	________________________	Date ____________
IMPACT QA:	________________________	Date:____________
NASA IMPACT Instrument Manager:	________________________	Date:____________

Problem Failure Report Continuation Sheet

PFR # SIT 01
Rev 01, 5/21/04

Rev log:
Rev   4/29/04 – original release
Rev 01 5/21/04 – corrected typo in S/N of suspected bad part

1. Anomaly Description

During initial functional testing/trimming of the newly-built SIT Energy Board S/N01 (=FM1), it was noted that the peak detector output of the low-gain channel was small and did not change when the input level was changed. The output of the high-gain channel behaved normally. Signal tracing on the board revealed normal operation of all circuits until the peak detector, an Amptek PH300RH hybrid, was reached. It had correct input, but incorrect output. The part designation is U4.

2. Cause of the Anomaly

The power supply for the test setup was checked and voltages were found to be correct. Substituting the energy ETU board for the flight SN01 verified that the test setup was not at fault. Substituting the flight SN02 board verified that the board design was not at fault.

Signal and power pins of the chip were investigated and comparisons were made between the faulty channel and the good channel on this board as well as on the ETU and SN02 flight board. (See attached data sheet for the PH300) Input voltages and signals were all correct. Timing of the input signal was such that its peak was well within the width of the Gate logic signal. Differences found were on output pins 12, 3 and 16. Pin 12 nominally goes low at the peak of the input signal and stays low during the discharge of the hold capacitor (some 10's of us's). On U4 it went down promptly at the beginning of the gate signal, before the peak of the input signal, and returned high at the end of the gate. Pins 3 and 16 nominally display the held pulse. On U4 they were at 0v and flat. The impedances of all output pins to ground were measured and found to be nominal.

All components surrounding U4 were checked and found good and the currents drawn by the chip were within expectations and identical to those on the other channel.

Conclusion: a fault within the PH300 chip, probably in the input gate.

Chip is PH300RH, D/C0224, S/N 1351, from Amptek Inc., 6 De Angelo Drive,Bedford MA, 01730. Tel 781-275-2242. Purchased by UC Berkeley, PO# 1-0000601778

Corrective Action Taken:

1. Obtained RMA number from Amptek RMA 042904-B

STEREO IMPACT

FAILURE ANALYSIS

X-Sender: dwc@apollo.ssl.berkeley.edu
Date: Fri, 11 Jun 2004 11:02:33 -0700
To: "Lillian S. Reichenthal" <Lillian.S.Reichenthal@nasa.gov>,
Peter Wapole <walpole@sampex.umd.edu>,
Chris Waterman <waterman@uleis.umd.edu>,
Larry Gibb <lgibb@pop400.gsfc.nasa.gov>,
Ron Jackson <ronj@ssl.berkeley.edu>
From: David Curtis <dwc@ssl.berkeley.edu>
Subject: Re: Fwd: FRB on Amptek Part Number PH300RH, D/C 0224

Lil:
So the upshot is probably ESD to an unprotected pin, and the solution is replacement with extra care taken when handling this device due to the unprotected input, correct?
Dave

At 10:53 AM 6/11/2004, Lillian S. Reichenthal wrote:
Dear All,
Attached is the Part Failure Review Board held for the PH300 device that failed on the SIT Energy Board. This device has since been replaced on the board. Please review the cause of failure and recommendations below and attach this paperwork with the SIT Energy board documentation.
Lil

Date: Wed, 9 Jun 2004 19:04:39 -0400
To: Vinod_Patel
From: Antonio Reyes <areyes@pop400.gsfc.nasa.gov>
Subject: FRB on Amptek Part Number PH300RH, D/C 0224
Cc: Frederick_Felt, Alexander_Toverovsky
Bcc:
X-Attachments: :Macintosh HD:264012:Q40139FA Stereo Hybrid AR.doc:

Vinoid,

On June 9, 2004, at 10:00AM, Bldg 22/R020, a FRB review was held in your office to discuss the failure of an analog peak hold detector manufactured by Amptek, part number PH300RH, LDC 0224, S/N 1351. "Evidence of electrical overstress (EOS) damage in the metallization and silicon substrate associated with Pin 1 (IN)" was the conclusion given by the failure analysis report. The report also suggests the possibility of an "ESD event preceded the EOS failure." The failure site was located near an unprotected bond pad connected directly to Pin 1.

The above results have prompted the reviewers to recommend to all end-users EXTREME CAUTION during the handling and installation of the PH300 hybrid. As pointed out by the device data sheet, Pin 1 lacks of an input protection diode, making the device sensitive to ESD damage. Therefore, the usage of a Schottky diode input protection is suggested. It should also be mentioned that the manufacturer has not quantified the ESD sensitivity of the hybrid and proper training of personnel on ESD precautions is also a must.

If you have any question or concerns about this review, please feel free to contact me at your earliest convenience.

Regards,

Antonio Reyes
STEREO Parts Engineer
X65927

Attendees: Vinod Patel, Fred Felter, Alexander Toverovsky and Antonio Reyes

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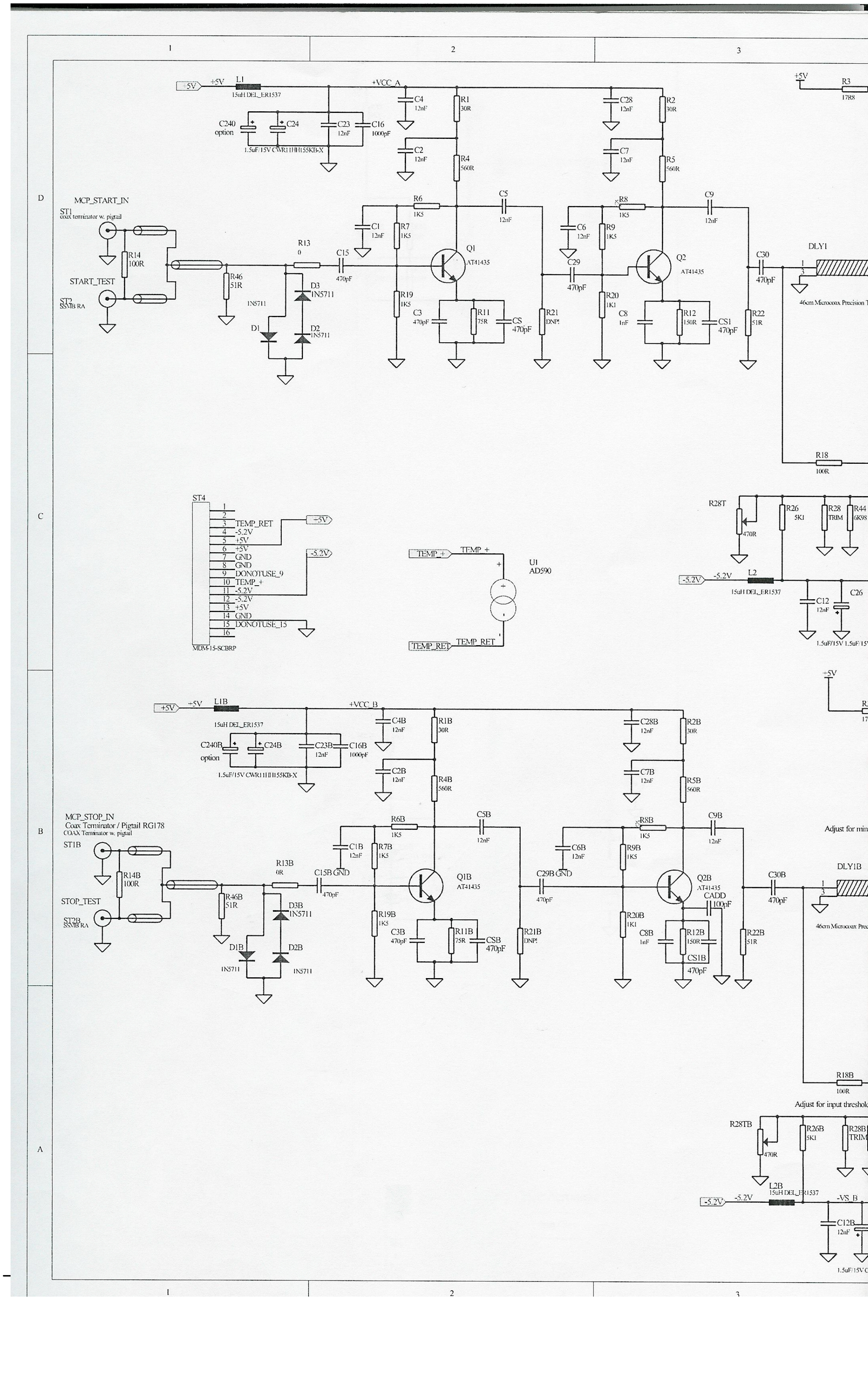

GODDARD SPACE FLIGHT CENTER

Failure Analysis Report

Project:	Stereo	Part Type:	Hybrid
Subsystem:	IMPACT-SIT Energy	Manufacturer:	Amptek
Date:	07 June 2004	Part Number:	PH300RH
Investigator:	F. Felt 286-9634	Date Code:	0224
Requestor:	A. Reyes 286-5927	Serial Number:	1351

Background

The STEREO SIT Energy Board, SN01, was found to be nonfunctional during initial testing. Trouble-shooting isolated the problem to the U4 circuit element, an Amptek PH300RH hybrid that had correct input, but incorrect output. The part was forwarded to the NASA GSFC Failure Analysis Laboratory for investigation.

Part Description

The PH300RH is an analog peak hold detector manufactured by Amptek. The hybrid package consists of a metal can, and lid, and 16 glass-sealed pins in a DIP configuration. The PH300RH features low power, high speed, low droop, and fast reset. It is rated for operation between –55C and +125C. The part is screened for high reliability.

Analysis and Results

External optical inspection was performed. The device consists of a metal can with a stitch-welded metal lid. The part markings are also made using a stitch-welding tool. The hybrid has sixteen (16) pins in a DIP arrangement. The pins are sealed to the metal body with frit glass.

Fine leak test was performed. After bombing overnight in helium, the part initially indicated in the E-7 atm cc sec^{-1} range, with a slow decay over four hours. The part was immersed in acetone to dissolve any possible external polymers that might absorb helium. The leak tester was recalibrated, and subsequent testing indicated the part had a leak rate of 8.2E-7 atm cc sec^{-1}. Despite the leak rate, the project decided to not perform residual gas analysis (RGA).

Gross leak test was conducted and the part passed, with no observable bubble stream.

Radiography was conducted. In x-ray images the hybrid appears to consist of multiple chip capacitors, dice, and gold wire bonds—some of which seem to have wire excess/smears.

PIND testing indicated vibration of internal components in fixed locations, but no evidence of a loose particle(s) was seen.

Curve tracer electrical testing found that many of the pin-to-pin combinations have tortured V-I signatures, with strange shapes, capacitance and hysteresis, including most combinations of pins 2 and 7 through 11.

The package lid was removed and the dice inside the hybrid were optically inspected. The dice were confirmed to be diodes, transistors, and microcircuits. A small metallization void in the aluminum was found near an input pin on the second largest microcircuit in the hybrid (labeled Die 1 for this analysis). The defect area was traced to a nearby gold pin (without input protection) and, from there, along the gold metallization of the hybrid to Pin 1—the input pin connected to the gate of the Peak Hold Detector. Inspection found that the void on Die 1 occurred where metal stepped across what appeared to be the base region of a bipolar transistor.

SEM inspection was conducted. Glassivation obscured the metal void. However a long crack was observed in the glassivation on one side of the aluminum trace. The crack extended approximately 50 microns from the location of the void, terminating near a roughly spherical mass of aluminum 7-microns in diameter, which appeared to have extruded from the crack.

The glassivation was stripped using plasma, chemical, and fluid pressure techniques. At the location of the aluminum void, a 1-micron pit in the silicon was found. SEM zoom and contrast established that the bottom of the pit had a rubble-like appearance, consistent with electrical overstress damage.

The remote location of the melted aluminum ball from the void site argues that the aluminum trace between the void and the ball was in a molten state, or at an elevated temperature near melting. This fact further suggests that this failure was caused by electrical overstress (EOS). The cracked glass is explained by thermal expansion during electrical overstress.

Although the coincidence of a leaky package and high phosphorous content in the BPSG glass initially suggested aluminum corrosion, the aluminum melt ball actually indicates that melting, not corrosion, took place.

It is important to note that while evidence of electrical overstress was found, EOS damage is relatively large compared to electrostatic discharge (ESD) damage, and could easily have obliterated the smaller evidence. The location of this failure site on the edge of a die near an unprotected bond pad connected directly to Pin 1 of the hybrid, is suggestive of electrostatic discharge. Moreover, failure across a dielectric layer between substrate and metallization is typical of ESD.

For these reasons it is possible an ESD event may have occurred during handling, providing a shorting path and resulting in electrical overstress at first power-up of the device. This is consistent with the report that the device failed immediately upon first usage.

Conclusion

Evidence of electrical overstress (EOS) damage was found in the metallization and silicon substrate of a microcircuit element associated with Pin 1 of the hybrid—the gate IN pin.

No direct evidence of electrostatic discharge was seen. But the circumstances of the failure suggest that it is possible an ESD event preceded EOS failure.

Appended Photographs:

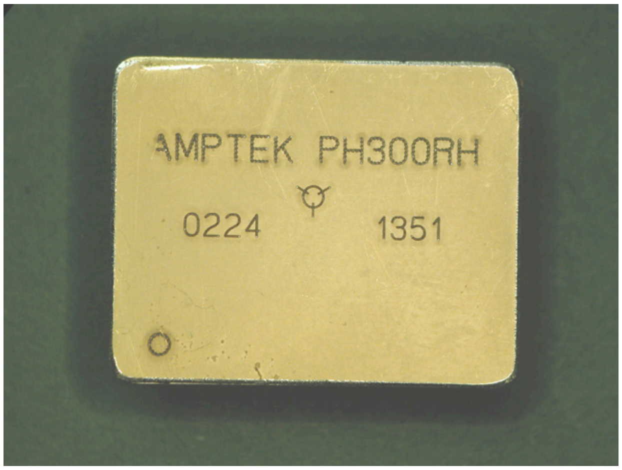

Figure 1. A top-down view of the Amptek hybrid, showing part markings.

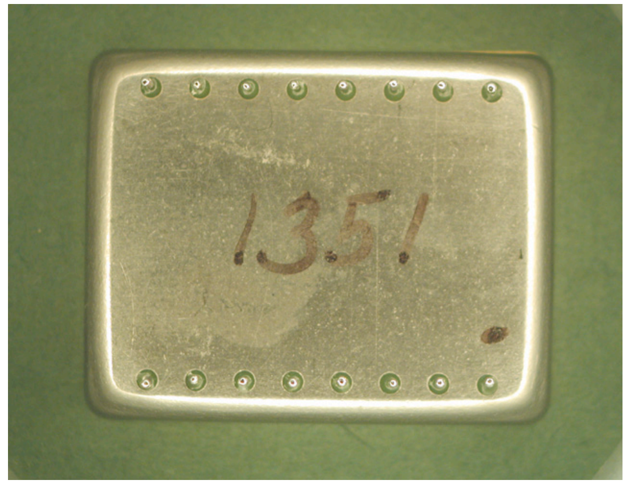

Figure 2. A bottom view of the 16-pin device. The marking indicates the serial number.

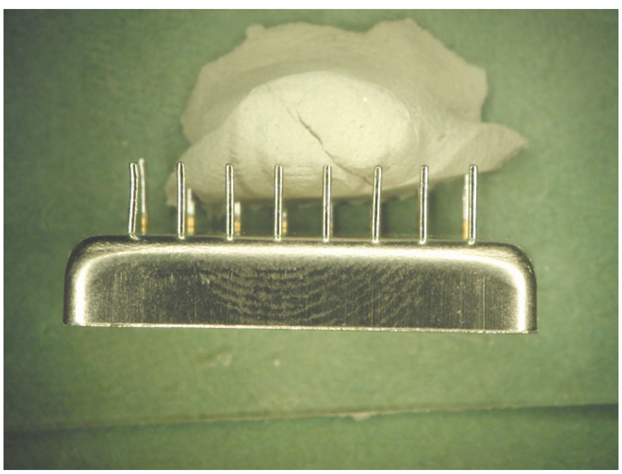

Figure 3. A side view of the 16-pin DIP hybrid.

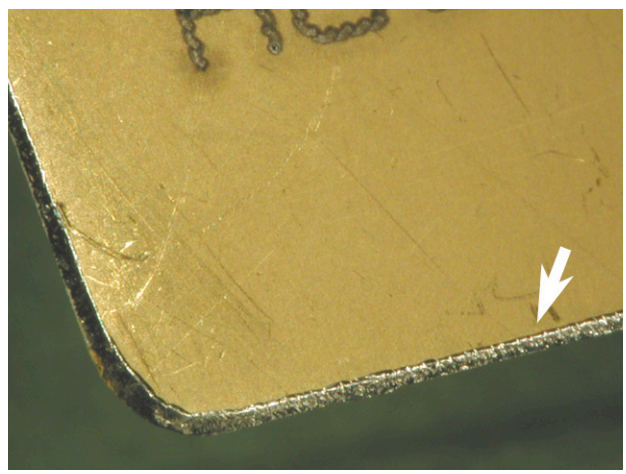

Figure 4. The arrow points to stitch welding which secures the lid to the body. Leak testing indicated a small leak in the package at an unknown location, possibly the frit glass, as some crazing was noted.

Appended Photographs:

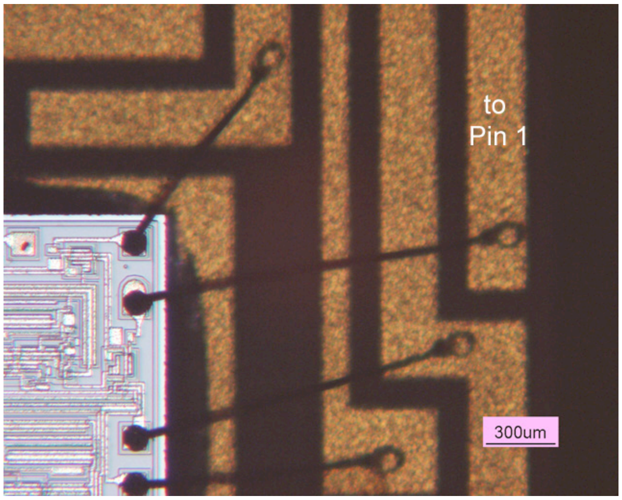

Figure 5. This view shows the corner of Die 1. The second bond wire from the top goes to the gold trace, which leads to Pin 1 of the hybrid.

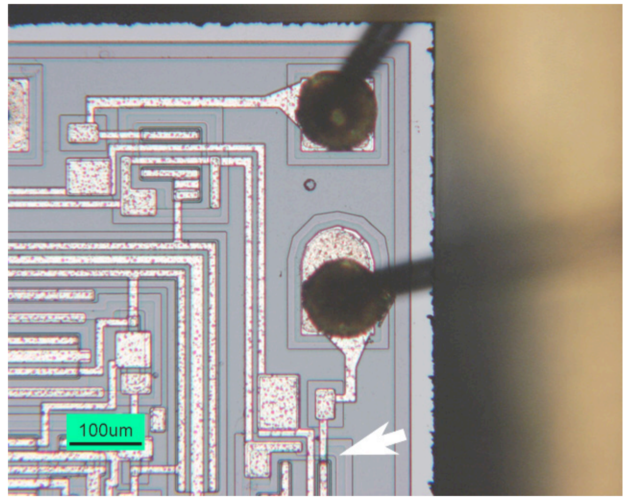

Figure 6. An anomaly was found on Die 1 at the arrow. The second bond wire from the top leads to Pin 1, and is connected to the defect site. No input protection is seen at this bond pad.

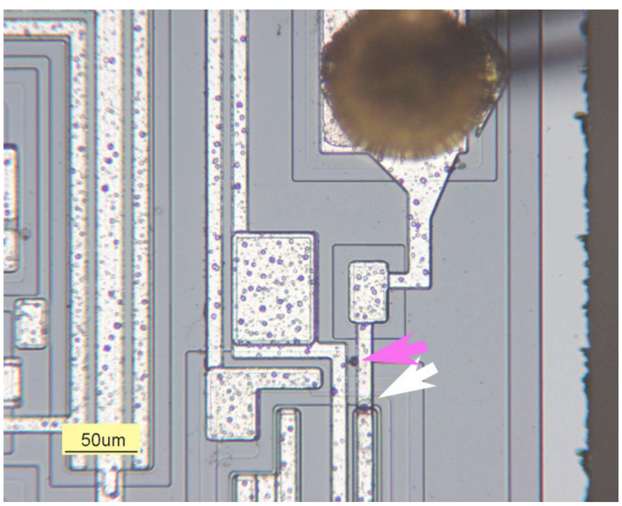

Figure 7. The defect resolves into two anomalies at higher magnification. The white arrow points to an apparent void in the metallization, seen through the transparent glass. The pink arrow points to an unusual feature noted adjacent to the wire.

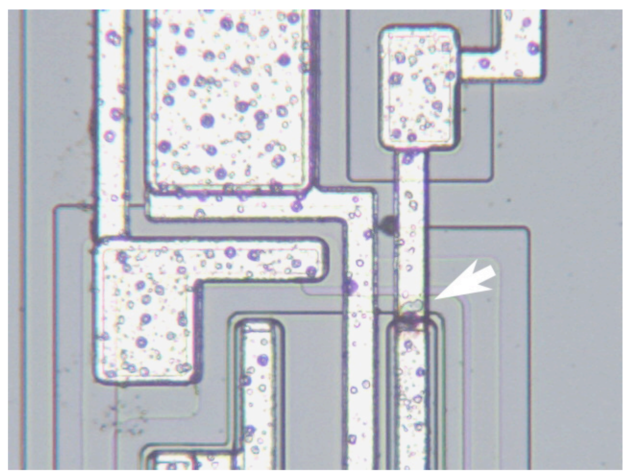

Figure 8. A zoom view of the metallization anomaly clearly shows a patch of missing metal at the arrow.

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Part Type	Hybrid	Part Number	PH300RH
Manufacturer	Amptek	Date Code	0224

Appended Photographs:

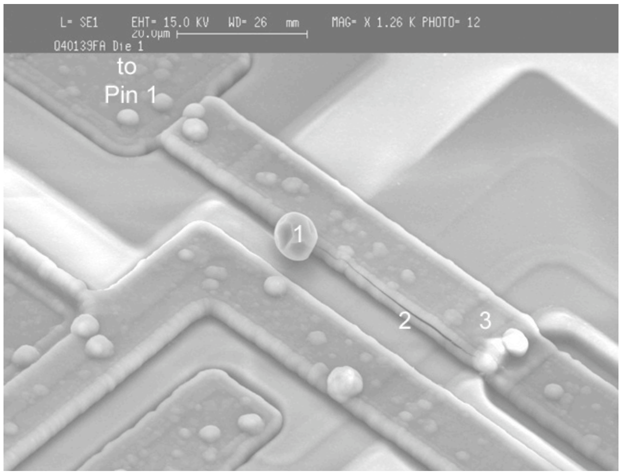

Figure 9. This labeled image shows the area of the defect.: (1) indicates a sphere at the end of a (2) crack, which terminates at, (3) the location of the void. The void is still covered by glassivation in this image.

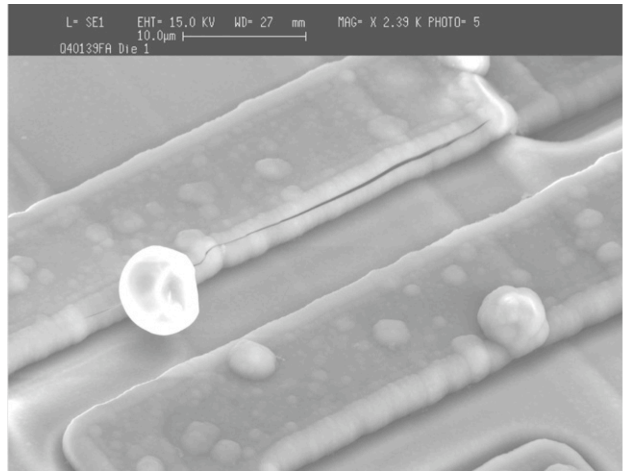

Figure 10. A different view of the defect area, clearly showing the cracked glassivation.

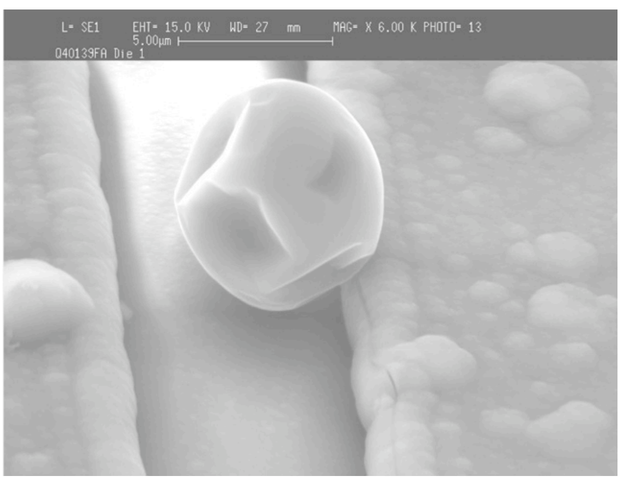

Figure 11. A close-up view of the soccer-ball like sphere near the end of the crack. The scale shows the sphere is approximately 7 microns in diameter.

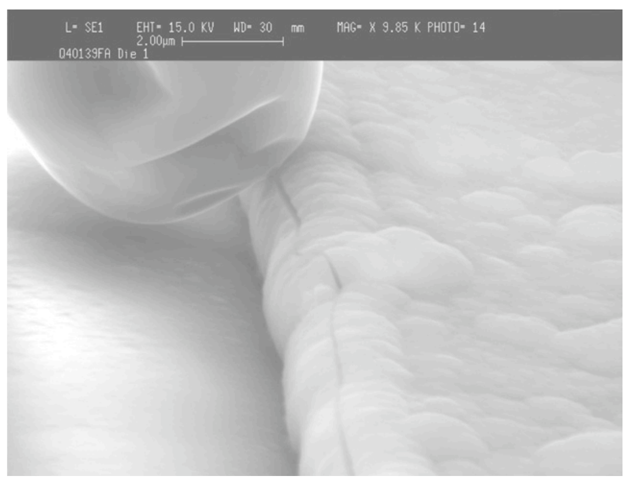

Figure 12. A slightly different angle of view shows that the sphere is connected exactly at the crack.

GODDARD SPACE FLIGHT CENTER

Part Type	Hybrid	Part Number	PH300RH
Manufacturer	Amptek	Date Code	0224

Appended Photographs:

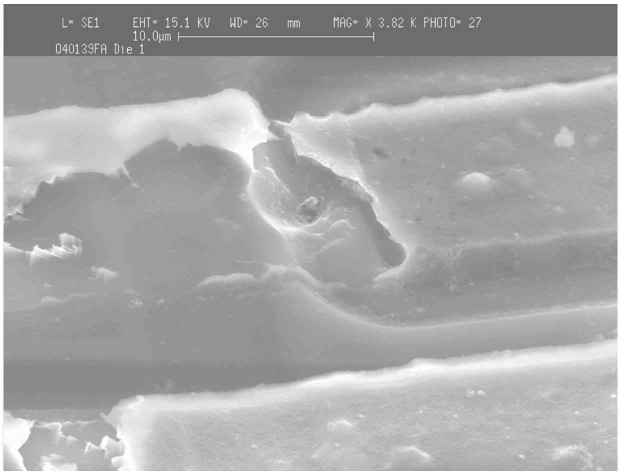

Figure 13. Plasma, chemical, and fluid pressure techniques were used to remove the glassivation. The fluid pressure also removed a wedge-shaped section of the aluminum between the location of the sphere and the metallization void, leading to the suspicion that this section had been thermally weakened.

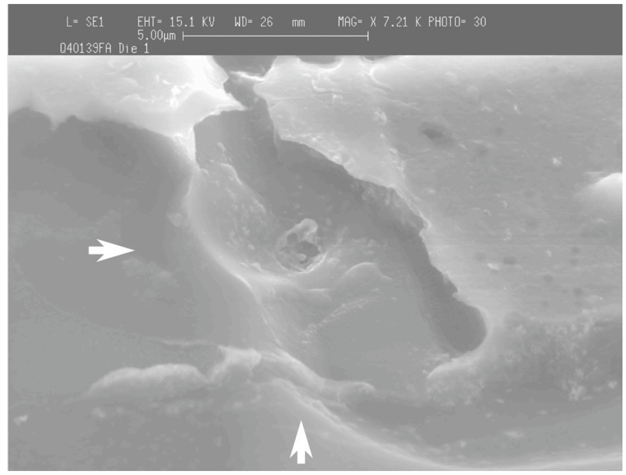

Figure 14. The arrows crosshair on a damage site in the silicon under the area of the void. This defect is seen in Figure 15.

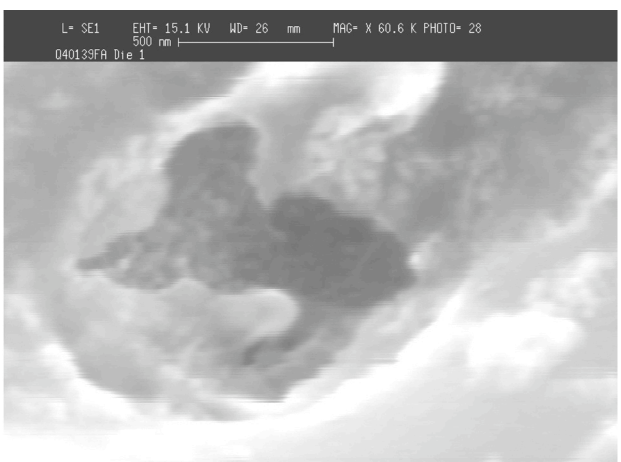

Figure 15. A Texas-shaped, but tiny, pit in the silicon is seen at high-magnification. Inspection of its bottom reveals a rubble-like appearance, consistent with electrical overstress damage.