STEREO IMPACT

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly: SEP	**SubAssembly: SEP Central**
Component/Part Number:	**Serial Number: FM1**
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Failure Occurred During (Check one √)

□ Functional test √ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

□ Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum √ Thermal-Vacuum □ EMI/EMC

Problem Description

During thermal balance test (May 2005) and thermal vac testing (June/July 2005) near -15 ºC, always as the temperature was rising from a cold soak, several seemingly unrelated problems kept occurring infrequently: Bias Supply would collapse – as described in PFR 2009; LET wouldn't reboot – PFR 2010; SEP Central would crash – PFR 2011. They were eventually tied to the same cause – particular bit flip on SEP Central SRAM's data buss. This was similar to the SRAM bit-flip problem in FM2 LET (see PFR 2013) that occurred in a slightly different temperature range and was easily reproducible.

Analyses Performed to Determine Cause

Having done the analysis of SRAM bit-flip problem in FM2 LET (as described in PFR 2013) in parallel with this investigation helped us a great deal in diagnosing the failure, although the ultimate cause of the problem still remains unknown. Same as in FM2 LET case, during T/V test we had additional diagnostic firmware loaded into the FM1 SEP Central microprocessor. In order to capture the problem the instrument temperature was typically set to -25 ºC and dwell time to 30 minutes. Then the temperature is slowly raised to -10 ºC, and if the bit flipped during the transition (typically at -15 ºC), a core dump would be obtained for FM1 SEP Central memory, and then compared with the "normal" memory core dump. This process had to be repeated several times since it was not easy catching the bit-flip in the act (later on, it was also used to verify that the problem has been solved once the suspect SRAM part was replaced).

7/27/2005 e-mail message (below) from Rick Cook summarizes the analyses performed:

Yesterday a bit-flip episode was successfully captured on FM1 in the thermal vac at JPL. The bit flip was detected by the routine once/min checksum calculation in SEP Central. A few minutes after the detection, an attempt to command SEP Central showed that it no longer properly interpreted commands. Then a core dump of SEP Central memory was obtained, and finally SEP Central was rebooted by sending a "hardware" reboot command (which reboots from the EEPROM). Then an attempt was made to check whether the LET and HET processors had been also affected by whatever caused the bit-flip event. It was noted that after the bit-flip event detection in SEP Central, packets continued to flow out, apparently in normal fashion. LET packets continued in the right number (16 per minute) and without perturbation. However, after the SEP Central reboot, the number of packets per minute from LET dropped to 9 and at the time this was considered anomalous. Also, when the attempt was made (post SEP Central reboot) to command LET, the LET prompt was seen correctly, but no echo or execution of commands. So, a core dump was also obtained for LET memory.

Analysis of the FM1 SEP Central core dump shows the presence of bit flips similar to those observed in FM2 LET episodes. However, for SEP Central the affected bit is bit 9 (it was bit 8 for FM2 LET). The flipped bits are again in blocks of 256 words and only at (address mod 8) = 2. Recall for FM2 LET there was a similar pattern of affected addresses, but with (address mod 8) = 6. Also, the start addresses of the affected 256 byte blocks is different for FM1 SEP Central, but shows a similar repeating pattern to FM2

LET. The particular pattern of flipped bits in FM1 accounts for the observations that most processing continued normally, while the ability to interpret commands was lost.

Analysis of the FM1 LET core dump does not show the now typical bit flip patterns. In fact, this core dump appears to represent a normally functioning LET. It now seems likely the drop in the number of packets per minute to 9 was caused by the turning off of the detector bias, which happens when SEP Central is rebooted.
The question remains as to why the commanding of LET appeared anomalous. Examination of LET's character input buffer in the core dump shows that only four CR characters ($D) were received (and no other characters) and this is compatible with the command log which shows four attempts to command LET. Further investigation is needed to determine if the commanding anomaly was due to a GSE problem, or some as yet undiagnosed LET or SEP Central problem.

The possible misinterpretation of the LET commanding anomaly to indicate a LET "crash", suggests that a careful re-examination of earlier FM1 crashes is needed. In those earlier crashes the evidence of multiple processor crashes is based on the lack of appropriate command response from the sensors following a SEP Central reboot. There may be an alternate explanation for this lack of response -- there may really be only a single problem in FM1 traceable to bit flips in the SEP Central SRAM.

The proposed path forward is to install a flight spare SRAM into FM2 LET and head back into thermal vac ASAP to determine if the bit flip problem is still present. Continued experimentation on LET EM will attempt to recreate bit flips. Investigation of more detailed GSE commanding records will attempt to shed light on the post SEP Central reboot commanding anomalies and clarify whether or not there is actually any evidence for multiple processors crashes on FM1.

Corrective Action/ Resolution

√ Rework □ Repair □ Use As Is □ Scrap

1. 7/31/2005 Replaced the offending SRAM device U3 (Honeywell P/N HLX6228TSR, S/N 00002, LDC 0314) on FM1 SEP Central Logic Board with S/N 00030 from the same lot, but without the four by-pass capacitors.
2. FM1 SEP Main Assembly passed re-qualification T/V test between 8/8/2005 – 8/11/2005 and subsequent 1-axis vibration test.
3. The failed device was sent to Honeywell for failure analysis, along with the one from FM2 LET (PFR 2013). The failure analysis is still pending. So far, they have not been able to reproduce the problem and determine the cause of malfunction.
4. In case of a negative result from the failure analysis, the investigation will continue at Caltech. We will install the failed device on the EM SEP Central Logic Board and instrument it for the test in thermal chamber, possibly with support from Honeywell engineers.

Update 6/2/2006 LR:
Although the failure could easily be replicated at Caltech, Honeywell was unable to reproduce the same thermal conditions to recreate the original failure. There was a schematic review between Caltech and Honeywell in an attempt to determine the root cause prior to any destructive analysis. The suspect device (from PFR 2013) was then delidded and Honeywell found a possible correlation between the failed locations and the spare fuse circuits. Although, at this time, the root cause of the failure is still unknown. This issue will be forwarded to the GSFC parts group for possible further analysis with Honeywell.

Since the SRAM devices were replaced, both FM1 and FM2 SEP Central/LET/HET have successfully passed instrument level and observatory level vibration and thermal vacuum testing. In addition, due to other rework, both instrument assemblies successfully passed an additional single axis vibration and four additional thermal vacuum cycles in May 2006. FM2 also saw one more additional single axis vibration. All flight units have been working nominally since the original repair in July 2005.

Date Action Taken: 7/31/2005 **Retest Results**: Passed
Corrective Action Required/Performed on other Units ☐ Serial Number(s): N/A

Closure Approvals

Subsystem Lead:	Branislav Kecman	Date: 8/31/2005
IMPACT Project Manager:	_____	Date:_____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____