STEREO IMPACT

PROBLEM REPORT
PR-1036
SEP LVPS
2005-02-27

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SEP LVPS	**SubAssembly :** Top and Middle Board
Component/Part Number: SEP_TOP_F001 and SEP_Middle_F001	**Serial Number:** FM2 and FM1
Originator: Selda Heavner	**Organization:** U.C. Berkeley
Phone : 510-643-8640	**Email :** selda@ssl.berkeley.edu

Failure Occurred During (Check one √)

√Functional test ☐ Qualification test ☐ S/C Integration ☐ Launch operations

Environment when failure occurred:

√Ambient ☐ Vibration ☐ Shock ☐ Acoustic
☐ Thermal ☐ Vacuum ☐ Thermal-Vacuum ☐ EMI/EMC

Problem Description

SEP LVPS FM2 was intermittently consuming high current at turn-on. The high-current at turn-on did not reach 0.90A which is the recommended current limit for the bench supply. It typically remained at 580-600mA range. The 28V line did not change when the Supply was consuming 580mA and remained at 28.0V. The supply was not left in the high current state for longer than 30 seconds.
The high-current at turn on caused some of the transistors to heat excessively. The conformal coating around the transistors and the shrink tubing covering the ferrite beads were burnt due to excessive heat generated by the transistors.

Analyses Performed to Determine Cause

SEP ETU Unit was tested using the bench supply from Caltech KIKUSUI PMC35-1A. SEP ETU was turned on and off until the problem was reproduced. When the high-current occurred the switching FETS became extremely hot. The FETs were still functional after leaving the high-current on a long time. Therefore, the problem is with the FET drivers (for the switching FETs that drive the transformers). When the drivers first come on they set their output to high impedance until their supply voltage exceeds some threshold. So the FET gate floats, and depending on leakage currents the FET can turn on providing a low impedance short (through the transformer windings) on the primary regulator. This in turn causes the voltage regulator to go into current limit so the voltage never gets over the turn-on threshold for the FET driver. So the difference between supplies (and between bench supplies that come up slower or faster) is if the leakage current is large enough to charge up the gate before the primary regulator voltage gets high enough to turn on the driver.

Corrective Action/ Resolution

√Rework ☑Repair ☐ Use As Is ☐ Scrap

100KΩ resistor from the FET gate to ground can hold the FETs off when the driver is in high impedance mode. This solution was incorporated on ETU and the problem could not be reproduced. Figure 1 indicates where the new resistors (Rnew) will be connected for the Top and Middle Board. Please see PFR 1036 addendum for detailed instructions.

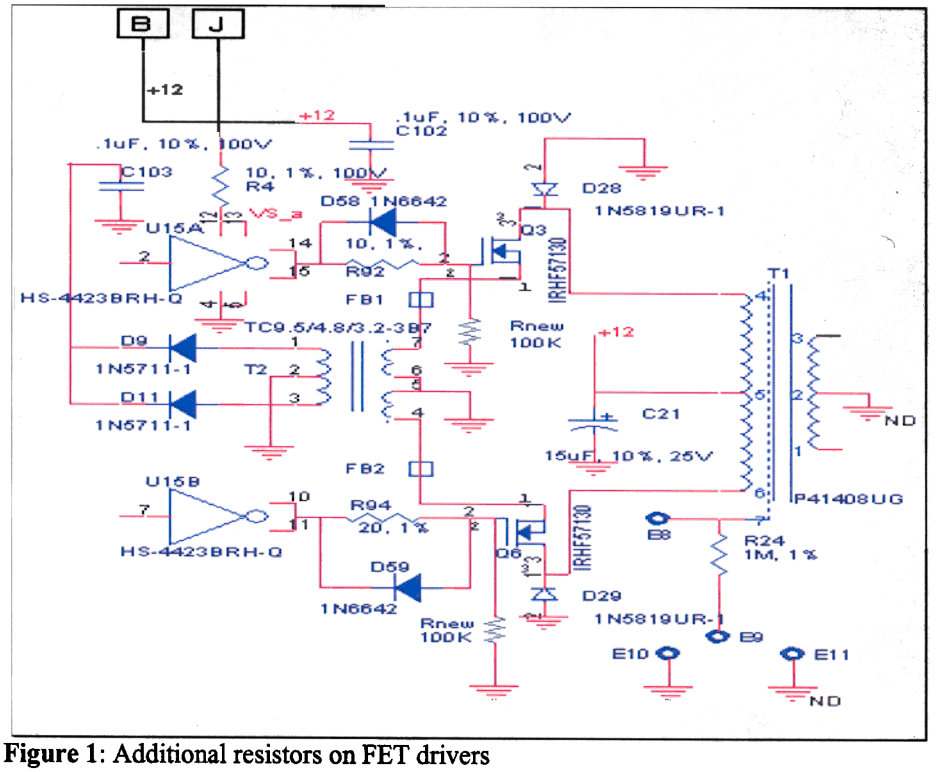

Figure 1: Additional resistors on FET drivers

Date Action Taken: _____ **Retest Results**: _____

Corrective Action Required/Performed on other Units : √Serial Number(s):SEP LVPS ETU

Closure Approvals

Subsystem Lead:	_____	Date:
IMPACT Project Manager:	_____	Date
IMPACT QA:	_____	Date:
NASA IMPACT Instrument Manager:	_____	Date: _____

STEREO PFR 1036

Date: March 8, 2005

STEREO SEP LVPS MIDDLE BOARD PFR 1036 INSTRUCTIONS

ASSEMBLY NUMBER: FM1

Requesting Engineer: Selda Heavner

1. Corrective Action for MIDDLE BOARD

1) Bake the boards at 60°C.

Start Time: 6:00PM Stop Time: 8:00AM

Completed by: HY **Date:** 3-8-05

2) Remove transistors with reference designators Q3, Q6, Q14, Q11, Q22, Q15, Q18, and Q20 (IRHF57130SCS) from the middle board. Do **NOT** use metallic tools to remove conformal coating.

2a) Remove the two wires interconnecting the two boards. 3-9-05 HY

Completed by: N/A **Date:** March 8, 2005 3-11-05

3) Remove burnt shrink tubing covering the ferrite beads. Record the location of removed ferrite beads.

No burnt transistors, shrink tubing SSH

Completed by: SSH **Date:** March 8, 2005

4) Remove burnt wires. Record the location of removed wires.

no burnt wires

Completed by: SSH **Date:** March 8, 2005

5) Remove 1N6642 diodes with reference designator D58, D59, D60, D62, D64, D65, D66, D68. Do **NOT** use metallic tools to remove conformal coating over the diodes.

Completed by: HY **Date:** 3-14-05

6) The middle board must be inspected.

Completed by: [illegible] **Date:** 3-14-05

7) Prepare 8 100K (RNC50H1003FR) resistors on bench prior to soldering by cutting one side of the resistor's lead short and connecting #24AWG stranded insulated wire with lash splice. Use #30AWG bus wire to perform lash splice. The other lead will connect directly on the diode anode side. Have the lash splice inspected before putting shrink tubing over the lash splice.

Date:

Completed by: HY **Date:** 3-15-05

QA Inspection by: RJ **Date:** 3-17-05

GSFC Inspection by: Ricardo Elliott **Date:** 3/17/05

8) Install ferrite beads (BDS3.5/1.3/3.3/4S2) on Q3, Q6, Q11, Q18, Q14 and Q15 (Do NOT Install on Q20 and Q22. Their ferrite beads are installed on current transformers).

Completed by: ~~HY~~ N/A RJ **Date:** 3-21-05

9) Solder transistors Q3, Q6, Q14, Q11, Q22, Q15, Q18, and Q20 (IRHF57130SCS) on the board.

Completed by: N/A **Date:** 3-21-05

10) Put shrink tubing around the ferrite beads that were removed at item #2

Completed by: N/A **Date:** 3-21-05

11) Solder the wires on the board that were removed at item #3.

Completed by: N/A **Date:** 3-21-05

12) Record D/C of the 100K (RNC50H1003FR) resistors.

D/C: 9847

Completed by: ~~3-15-05~~ HY 3-15-05 **Date:** ~~9847~~

13) Plug new D58 on its pads. **Do <u>NOT</u> SOLDER** until the resistor is connected on the anode side. Do **<u>NOT</u>** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D58: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

14) Connect the 100K resistor (lead side) on the anode side of D58 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

Date:

15) Install a post on E10. E9

Completed by: HY **Date:** 3-17-05

16) Connect the other side of the 100K resistor to E10.

Completed by: HY **Date:** 3-17-05

17) Plug new D59 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D59: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

18) Connect the 100K resistor (lead side) on the anode side of D59 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

19) Connect the other side of the 100K resistor to E10.

Completed by: HY **Date:** 3-17-05

E10 & E9 must remain connected. Connect E10 to the resistor using bus wire #32 AWG. SSH 3-21-05

20) Plug new D60 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

3-21-05

D60: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

21) Connect the 100K resistor (lead side) on the anode side of D60 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

22) Install a post on E22 E2

Completed by: HY **Date:** 3-17-05

23) Connect the other side of the 100K resistor to E22. E21

E21 & E22 must remain connected. Connect E21 & E22 to the resistor using bus wire #32 AWG SSH 3-21-05

3-21-05

Date:

Completed by: HY **Date:** 3-17-05

24) Plug new D62 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D62: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

25) Connect the 100K resistor (lead side) on the anode side of D62 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** H9847

26) Connect the other side of the 100K resistor to E22.

Completed by: HY **Date:** 3-17-05

27) Plug new D64 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D64: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

28) Connect the 100K resistor (lead side) on the anode side of D64 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

29) Install a post on E44.

Completed by: HY **Date:** 3-17-05

30) Connect the other side of the 100K resistor to E44. E41

Completed by: HY **Date:** 3-17-05

E44 & E41 must remain connected Connect E21 & E22 to the resistor using bus wire #32AWG. 3-21-05 SSH

31) Plug new D65 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below. 3-21-05

D65: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

Date:

32) Connect the 100K resistor (lead side) on the anode side of D65 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

33) Connect the other side of the 100K resistor to E44.

Completed by: HY **Date:** 3-17-05

34) Plug new D66 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D66: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

35) Connect the 100K resistor (lead side) on the anode side of D66 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

36) Install a post on E52. E

Completed by: HY **Date:** 3-17-05

37) Connect the other side of the 100K resistor to E52.

Completed by: HY **Date:** 3-17-05

E52 & E51 must remain connected. Connect E52 and E51 to the resistor using a bus wire #32 AWG SSH 3-21-05 3-21-05

38) Plug new D68 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D68: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

39) Connect the 100K resistor (lead side) on the anode side of D69 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

Date:

40) Connect the other side of the 100K resistor to E52.

Completed by: HY **Date:** 3-17-05

41) Thoroughly clean the board.

Completed by: HY **Date:** 3-17-05

	QA Inspector	GSFC Inspector
Solder Inspection	3-21-05	
Part Orientation		
Layout		
Installation		

QA Inspection by: [signature] **Date:** 3-21-05

GSFC Inspection by: _____ **Date:** _____

42) Apply staking material (Uralane 5753) to all additional resistors per NASA-STD-8739.1

3-22-05 Staked 5753 1:00PM

Mix ratio: 1-20-05 3-22-05 **Expiration Date:** 5/05

Start Time: 5:00PM (bake) **Stop Time:** 8:00AM 3-23-05 60°C

Completed by: HY **Date:** 3-22-05

43) Apply staking material on the wires per NASA-STD-8739.1

Completed by: HY **Date:** 3-22-05

44) Stake the ferrite beads on the transistor leads and the transistors (tri-star stake) per NASA-STD-8739.1

Completed by: H **Date:**

45) Conformally coat all new diodes, resistors and the transistors using Uralane 5750.

Completed by: HY **Date:** 3-23.24-05

46) Take pictures of the completed rework/repair.

Completed by: _____ **Date:** _____

Approved by: _____ **Date:** _____

Approved by: _____ **Date:** _____

QA Inspection by: _____ **Date:** _____

GSFC Inspection by: _____ **Date:** _____

Date:

2. **Corrective Action for TOP BOARD**

1) Remove transistors with reference designators Q10, Q12, Q19 and Q21 (IRHF57130SCS) from the top board. Do **NOT** use metallic tools to remove conformal coating.

Completed by: N/A **Date:** 03/14/05

2) Remove burnt shrink tubing covering the ferrite beads. Record the location of removed ferrite beads.

no burnt shrink tubing

Completed by: N/A **Date:** 03/14/05

3) Remove burnt wires. Record the location of removed wires.

no burnt wires

Completed by: N/A **Date:** 03/14/05.

4) Remove 1N6642 diodes with reference designator D67, D69, D61 and D63. Do **NOT** use metallic tools to remove conformal coating over the diodes

Completed by: HY **Date:** 3-14-05

5) Top board must be inspected by QA.

Completed by: [signature] **Date:** 3-14-05

6) Prepare 4 100K (RNC50H1003FR) resistors on bench prior to soldering by cutting one side of the resistor's lead short and connecting #24AWG stranded insulated wire with lash splice. Use #30AWG bus wire to perform lash splice. The other lead will connect directly on the diode anode side. Have the lash splice inspected before placing shrink tubing

7) **Completed by:** HY **Date:** 3-15-05

QA Inspection by: [signature] **Date:** 3-17-05

QA Inspection by: [signature] **Date:** 3/17/05

~~8)~~ Install ferrite beads (BDS3.5/1.3/3.3/4S2) on Q10, Q12, Q19 and Q21.

Completed by: **Date:**

N/A [signature] 3-21-05

Date _____

9) Solder transistors Q10, Q12, Q19 and Q21 on the board

Completed by: _____ **Date:** _____

10) Put shrink tubing around the ferrite beads that were removed at item #2

Completed by: _____ **Date:** _____ N/A 3-21-05

11) Solder the wires on the board that were removed at item #3.

Completed by: _____ **Date:** _____

12) Record D/C of the 100K (RNC50H1003FR) resistors.

D/C: _____

Completed by: _____ **Date:** _____

13) Plug new D67 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D67: JANTXV1N6642 D/C: H9847

Completed by: HT **Date:** 3-17-05

14) Connect the 100K resistor (lead side) on the anode side of D67 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HT **Date:** 3-17-05

15) Install a post on E56.

E56 & E55 must remain connected. Connect the resistor to E56 (or E55) using #32 AWG bus wire. SSH 3-21-05

Completed by: HT **Date:** 3-17-05 3-21-05

16) Connect the other side of the 100K resistor to E56.

Completed by: HT **Date:** 3-17-05

17) Plug new D69 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D69: JANTXV1N6642 D/C: H9847

Completed by: HT **Date:** 3-17-05

Date:

18) Connect the 100K resistor (lead side) on the anode side of D69 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

19) Connect the other side of the 100K resistor to E56.

Completed by: HY **Date:** 3-17-05

20) Form a pigtail on D61 anode. Solder D61. Record D/C below.

D61: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

21) Connect the 100K resistor (lead side) on the anode side of D61 and loop the resistor around. Solder the diode the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

22) Install a post on E32. E30

Completed by: HY **Date:** 3-17-05

23) Connect the other side of the 100K resistor to E32.

Completed by: HY **Date:** 3-17-05

E32 & E30 must remain connected. Connect E32 & E30 with resistor using #32AWG bus wire SSH 3-21-05 RH 3-21-05

24) Plug new D63 on its pads. **Do <u>NOT</u> SOLDER** until the resistor is connected on the anode side. Do **<u>NOT</u>** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D63: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-17-05

25) Connect the 100K resistor (lead side) on the anode side of D63 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-17-05

Date:

26) Connect the other side of the 100K resistor to E32.

Completed by: HY **Date:** 3-17-05

27) Thoroughly clean the board.

Completed by: HY **Date:** 3-17-05

	QA Inspector	GSFC Inspector
Solder Inspection	RJ 3-21-05	
Part Orientation	RJ	
Layout	RJ	
Installation	RJ	

QA Inspection by: RJ **Date:** 3-21-05

QA Inspection by: _____ **Date:** _____

28) Apply staking material (Uralane 5753) to all additional resistors per NASA-STD-8739.1.

Mix ratio: 1-20-05 **Expiration Date:** 5/05

Start Time: Coupon(3-22-05) Start bake **Stop Time:** Book#4(3-23-05) bake 60C°

Completed by: HY **Date:** 3-22-05

29) Apply staking material on the wires per NASA-STD-8739.1

Completed by: HY **Date:** 3-22-05

30) Stake the ferrite beads on the transistor leads and the transistors (tri-star stake) per NASA-STD-8739.1

Completed by: **Date:**

31) Conformally coat all new diodes, resistors and the transistors using Uralane 5750.

Completed by: HY **Date:** 3-23-24-05

32) Take pictures of the completed rework/repair.

Completed by: **Date:**

Date:

Approved by: _____ **Date:** _____

Approved by: _____ **Date:** _____

QA Inspection by: _____ **Date:** _____

Date:

3. **Corrective Action for all Board with Repairs**

1) Add more points of staking along the repair wires especially where the wire changes direction per NASA-STD-8739.1

Completed by: **Date:**

2) Make sure all transistors have tri-star stake.

Completed by: **Date:**

3) Apply staking to the leads of any transistors that are in dead-bug position. Apply tri-star staking to the transistors.

Completed by: _____ **Date:** _____

4) Apply more staking to the capacitors per NASA-STD-8739.1

Completed by: **Date:**

5) Apply staking fillets to any parts that are laying on the board.

Completed by: **Date:**

6) Apply more staking to the wires that connect the thermistor to the top board (SLH and TH)

Completed by: **Date:**

7) Apply more staking to the wires that lay between J1 connector and the OP_HTR and OP_HTR_RTN.

Completed by: **Date:**

8) Apply more staking to the wires of the inductors and transformers.

Completed by:

9) Apply staking to cambion pins on top board.

Completed by:

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Date:

Approved by: _____ **Date:** _____

Approved by: _____ **Date:** _____

QA Inspection by: _____ **Date:** _____

GSFC Inspection by: _____ **Date:** _____

1. Due to insufficient boards space the resistor jumper wires are currently staked above the PCB surface area forming a bridge along the side and over components - DSC000053, DSC000062, DSC000072 & DSC000092. USE AS IS(I do not see any reliability issues because wires are staked loose bewteen components).

2. Two resistor leads insulated with shrink tubing, staked over three surface mount resistors that are covered with conformal coat material FM1- DSC00010 & DSC00011. USE AS IS (I do not see any reliability issues with FM2 resistors wire are insulated with kapton tape to prevent shorting.

3. Bridging staking material around transistor leads - DSC000042 & DSC000092. Rework by removing staking material from lead.

4. Resistor jumper wire mounted under the transistor package, forming a potential short - DSC000072 & DSC000082. Repair by adding staking material along the side of the transistor to protect and support jumper wire against exposure to short.

5. Cleanliness testing

All PCB's shall be tested prior to conformal coating.

Two basic test methods are recommended.
a. resistivity of solvent extract
b. Sodium chloride salt equivalent ionic contamination test
USE AS IS - all boards are cleaned using Isopropyl Alcohol and dried prior to adding staking and conformal coating.
Ron

Delivered-To: ronj@apollo.ssl.berkeley.edu
Date: Fri, 11 Mar 2005 17:26:46 -0500
To: ronj@ssl.berkeley.edu
From: Mike Jones <mijones@pop700.gsfc.nasa.gov>
Subject: Wire removal
Cc: Ricardo.Rodriquez@honeywell-tsi.com, lgibb@pop400.gsfc.nasa.gov,
Lil Reichenthal <lreichen@pop700.gsfc.nasa.gov>
X-CanItPRO-Stream: admin
X-Spam-Score: 0 ()
X-Scanned-By: CanIt (www . canit . ca)

Ron,

Both Larry and myself agree with the decision to remove the two wires interconnecting the two boards to allow for ease of rework. And, later to reinstall at a later time in the PR instructions. Please red line your PR instructions (sign /date redline).

Thanks,
Mike Jones

Delivered-To: ronj@apollo.ssl.berkeley.edu
X-ASG-Debug-ID: 1111166069-15872-92-0
X-Barracuda-URL: http://mailwall.ssl.berkeley.edu:8000/cgi-bin/mark.cgi
Date: Fri, 18 Mar 2005 12:14:22 -0500
To: "Lillian S. Reichenthal" <Lillian.S.Reichenthal@nasa.gov>,
David Curtis <dwc@ssl.berkeley.edu>, ronj@ssl.berkeley.edu
From: Mike Jones <mijones@pop700.gsfc.nasa.gov>
X-ASG-Orig-Subj: Re: Fwd: SEP visual rejection items by GSFC.
Subject: Re: Fwd: SEP visual rejection items by GSFC.
Cc: lgibb@pop400.gsfc.nasa.gov, Laurie Kleppin <lkleppin@pop300.gsfc.nasa.gov>,
Ricardo.Rodriquez@honeywell-tsi.com,
"Rodriguez, Ricardo G" <Ricardo.Rodriguez@honeywell-tsi.com>
X-Virus-Scanned: by Barracuda Spam Firewall at ssl.berkeley.edu
X-Barracuda-Spam-Score: -5.40
X-Barracuda-Spam-Status: No, SCORE=-5.40 using global scores of TAG_LEVEL=1.0
QUARANTINE_LEVEL=3.0 KILL_LEVEL=1000.0 tests=BAYES_00
X-Barracuda-Spam-Report: Code version 2.64, rules version 2.1.1942
Rule breakdown below pts rule name description
---- ---------- ----------
-5.40 BAYES_00 BODY: Bayesian spam probability is 0 to 1%
[score: 0.0000]
X-Qmail-MasqDomain: False

Dave, Ron, and Lil,

Item #1 and #3 should be fine, recommend approval (valid findings).

Item #2 related photograph concerns me greatly.

I agreed that the leads could be used as terminals. However, the attaching conductor should have been in contact with the base, the pad in your case (standard practice). The way these conductor leads are at the end of the lead (terminal) brings much concern about lead fatigue (where solder joint to lead interfaces). Also, the shrink tubing is very short on the one side raising shorting concerns.

Currently, I do not recommend using as is. Need additional information from your team.

Please call, we need to talk/work this issue.

Regards,
Mike Jones
301-286-3198

X-Sender: dwc@apollo.ssl.berkeley.edu
Date: Thu, 17 Mar 2005 14:31:59 -0800
To: Lillian Reichenthal <lreichen@pop700.gsfc.nasa.gov>
From: David Curtis <dwc@ssl.berkeley.edu>
Subject: Fwd: SEP visual rejection items by GSFC.
Cc: Ron Jackson <ronj@ssl.berkeley.edu>
X-Proofpoint-Spam-Details: rule=notspam policy= score=0 mlx=-1 adultscore=0 adjust=0 engine=2.5.0-05031400 definitions=2.5.0-05031700

Lil:
The inspector rejected the FM2 SEP LVPS board for 3 issues listed below (see also attached pictures). Let me know if you want it written up on a PFR form. He agreed that these are really cosmetic, but wanted an official waiver. I authorized the board to proceed to conformal coat as is, with an MRB to run in parallel. I apologize for the focus on picture 17; it shows the splice of the resistor to the diode lead, the concern being how high the diode lead extends above the board. Picture 18 shows the poor strain relief (diode in the back). The other end of this diode has good strain relief, so we feel that there is not a real issue. Picture 18 also shows (poorly) the bridging of the diode lead by conformal coat (diode in front). It is not clear to me why this is an issue; Uralane is pliable enough that it should not impact strain relief.
Dave

Delivered-To: dwc@apollo.ssl.berkeley.edu
X-Sender: ronj@apollo.ssl.berkeley.edu
X-Mailer: QUALCOMM Windows Eudora Version 5.0
Date: Thu, 17 Mar 2005 14:10:28 -0800
To: David Curtis <dwc@ssl.berkeley.edu>
From: Ron Jackson <ronj@ssl.berkeley.edu>
Subject: SEP visual rejection items by GSFC.
X-Qmail-MasqDomain: True
X-Qmail-MasqDomain: True

Dave,
Item #1 The stress relief bend radius shall not be less than the lead diameter per NASA-Std-8739.3

Item #2 Straight-through termination, lead protrusion exceeds max (0.090 inch) per NASA-Std-8739.3

Item #3 Conformal coating bridges stress relief areas there negating stress relief NASA-Std-8739.1

Ron Jackson
UC Berkeley,Space Sciences Laboratory
7 Gauss Way MC 7450
Berkeley, CA 94720-7450

Tel: (510) 643-2625
AST:7731^29u18e3

==========:
David Curtis
Space Sciences Laboratory
University of California at Berkeley
7 Gauss Way
Berkeley, CA 94720-7450
(510) 642-5998 FAX: (510) 643-8302
==========:
AST:7731^29u18e3

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Lillian Reichenthal
STEREO Instrument Manager

NASA Goddard Space Flight Center
Building 6, Room S126
Mail Code 463
8800 Greenbelt Road
Greenbelt, Maryland 20771

(office) 301-286-5634
(fax) 301-286-1696
(cell) 443-745-2716

Attachment converted: Macintosh HD:DSC00018.JPG (JPEG/JVWR) (0005EA0C)
Attachment converted: Macintosh HD:DSC00017.JPG (JPEG/JVWR) (0005EA0D)

APPENDIX 4: SEP LVPS TEST PROCEDURE

Part Number SEPLVPS FM1 Serial Number FM1 Date 3-18-05

Operator Selda Heavner Inspector _____

APPENDIX 4:

5. Post-Conformal Coat Tests:

Repeating tests after resistor installion.

5.1 Weight Measurement

Weight: N/A grams

5.2 Functional tests

5.2.1 Presence of Output Voltages

Output Voltages				
Signal name	**Min**	**Max**	**Output**	**Unit**
SEPT-NS 5.3 Digital	5.04	5.57	5.306	
SEPT-NS 2.6 Digital	2.47	2.73	2.553	
SEPT-NS 5.6 Analog	5.32	5.88	5.643	
SEPT-E 5.3 Digital	5.04	5.57	5.386	
SEPT-E 2.6 Digital	2.47	2.73	2.549	
SEPT-E 5.6 Analog	5.32	5.88	5.706	V
SIT HET LET +13 Analog	12.35	13.65	13.47	V
SIT HET LET -13 Analog	-13.65	-12.35	-13.61	V
SIT HET LET +6 Analog	5.70	6.30	5.937	
SIT HET LET -6 Analog	-6.30	-5.70	-6.233	V
SIT HET LET 2.6V Digital	2.47	2.73	2.513	V
SIT HET LET 3.4V Digital	3.23	3.57	3.313	V
SIT HET LET +5.1V Digital	4.85	5.36	5.06	V
SIT HET LET -5.2V Digital	-5.46	-4.94	-5.199	V

5.2.2 Efficiency

Signal name	Voltage	Current	Power (W)
SEPT-NS 5.3 Digital			
SEPT-NS 2.6 Digital			
SEPT-NS 5.6 Analog			
SEPT-E 5.3 Digital			
SEPT-E 2.6 Digital			
SEPT-E 5.6 Analog			
SIT HET LET +13 Analog			
SIT HET LET -13 Analog			
SIT HET LET +6 Analog			
SIT HET LET -6 Analog			
SIT HET LET 2.6V Digital			
SIT HET LET 3.4V Digital			

STEREO IMPACT

PROBLEM REPORT
PR-1036
SEP LVPS
2005-02-27

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SEP LVPS	**SubAssembly :** Top and Middle Board
Component/Part Number: SEP_TOP_F001 and SEP_Middle_F001	**Serial Number:** FM2 and FM1
Originator: Selda Heavner	**Organization:** U.C. Berkeley
Phone : 510-643-8640	**Email :** selda@ssl.berkeley.edu

Failure Occurred During (Check one √)

√Functional test ☐ Qualification test ☐ S/C Integration ☐ Launch operations

Environment when failure occurred:

√Ambient ☐ Vibration ☐ Shock ☐ Acoustic
☐ Thermal ☐ Vacuum ☐ Thermal-Vacuum ☐ EMI/EMC

Problem Description

SEP LVPS FM2 was intermittently consuming high current at turn-on. The high-current at turn-on did not reach 0.90A which is the recommended current limit for the bench supply. It typically remained at 580-600mA range. The 28V line did not change when the Supply was consuming 580mA and remained at 28.0V. The supply was not left in the high current state for longer than 30 seconds.
The high-current at turn on caused some of the transistors to heat excessively. The conformal coating around the transistors and the shrink tubing covering the ferrite beads were burnt due to excessive heat generated by the transistors.

Analyses Performed to Determine Cause

SEP ETU Unit was tested using the bench supply from Caltech KIKUSUI PMC35-1A. SEP ETU was turned on and off until the problem was reproduced. When the high-current occurred the switching FETS became extremely hot. The FETs were still functional after leaving the high-current on a long time. Therefore, the problem is with the FET drivers (for the switching FETs that drive the transformers). When the drivers first come on they set their output to high impedance until their supply voltage exceeds some threshold. So the FET gate floats, and depending on leakage currents the FET can turn on providing a low impedance short (through the transformer windings) on the primary regulator. This in turn causes the voltage regulator to go into current limit so the voltage never gets over the turn-on threshold for the FET driver. So the difference between supplies (and between bench supplies that come up slower or faster) is if the leakage current is large enough to charge up the gate before the primary regulator voltage gets high enough to turn on the driver.

Corrective Action/ Resolution

√Rework √Repair ☐ Use As Is ☐ Scrap

100KΩ resistor from the FET gate to ground can hold the FETs off when the driver is in high impedance mode. This solution was incorporated on ETU and the problem could not be reproduced. Figure 1 indicates where the new resistors (Rnew) will be connected for the Top and Middle Board. Please see PFR 1036 addendum for detailed instructions.

STEREO IMPACT

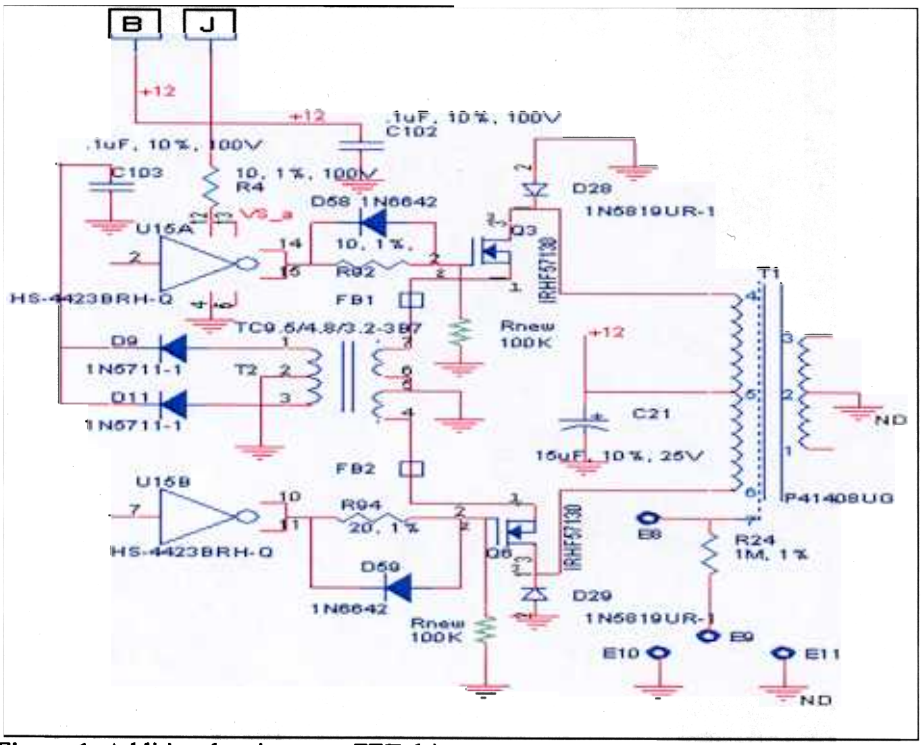

Figure 1: Additional resistors on FET drivers

Date Action Taken: _____ **Retest Results**:_____

Corrective Action Required/Performed on other Units : √Serial Number(s):SEP LVPS ETU

Closure Approvals

Subsystem Lead:	_____	Date:_____
IMPACT Project Manager:	_____	Date _____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____

STEREO PFR 1036

Date:

STEREO SEP LVPS MIDDLE BOARD PFR 1036 INSTRUCTIONS

ASSEMBLY NUMBER: FM2

Requesting Engineer: _____

1. **Corrective Action for MIDDLE BOARD**
   1) Bake the boards at 60°C. ~~24 hours~~. Total Hrs 19 HRS 3-10-05

      Start Time: 1:30 PM 3-9 Stop Time: 8:50 AM 3-10

      Completed by: HY **Date:** 10-3-05 1 2

   2) Remove transistors with reference designators Q3, Q6, Q14, Q11, Q22, Q15, Q18, and Q20 (IRHF57130SCS) from the middle board. Do **NOT** use metallic tools to remove conformal coating.

   2a) remove the Two wires interconnecting the two boards 3-10-05

      Completed by: HY **Date:** 3-10-05 3-11-05

   3) Remove burnt shrink tubing covering the ferrite beads. Record the location of removed ferrite beads.

      wire number 2. 3 from connP1

      Completed by: HY **Date:** 3-10-05

   4) Remove burnt wires. Record the location of removed wires.

      No burnt wires 3-10-05

      Completed by: N/A **Date:** 3-14-05

   5) Remove 1N6642 diodes with reference designator D58, D59, D60, D62, D64, D65, D66, D68. Do **NOT** use metallic tools to remove conformal coating over the diodes.

      Completed by: HY **Date:** 3-10-05

   6) The middle board must be inspected. 3/14/05 Ref = PFR # 1037

      Completed by: [illegible] **Date:** 3-14-05

   6a) Bake the board @ 60°C for 24 hours START Time N/A stop time N/A 3-14-05

   7) Prepare 8 100K (RNC50H1003FR) resistors on bench prior to soldering by cutting one side of the resistor's lead short and connecting #24AWG stranded insulated wire with lash splice. Use #30AWG bus wire to perform lash splice. The other lead will connect directly on the diode anode side. Have the lash splice inspected before putting shrink tubing over the lash splice.

PROBLEM REPORT
PR-1037
SEP LVPS Middle FM1
2005-03-10

STEREO IMPACT

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SEP LVPS	**SubAssembly : Top and Middle board**
Component/Part Number: SEP_F001 and SEP Middle_F001	**Serial Number: FM2**
Originator: Ron Jackson	**Organization: UC Berkeley**
Phone : (510) 643-2625	**Email : ronj@ssl.berkeley.edu**

Failure Occurred During (Check one √)

☒ Functional test ☐ Qualification test ☐ S/C Integration ☐ Launch operations

Environment when failure occurred:

☐ Ambient ☐ Vibration ☐ Shock ☐ Acoustic
☐ Thermal ☐ Vacuum ☐ Thermal-Vacuum ☐ EMI/EMC

Problem Description

Soldermask substrate scraped exposing top layer.

Analyses Performed to Determine Cause

Soldermask damaged during conformal coating removable @ Q3 and Q6 – Top layer(1.5mils) of soldermask damaged only. Second layer of glass fiber material not damaged.

Corrective Action/ Resolution

☐ Rework ☒ Repair ☐ Use As Is ☐ Scrap

Cover exposed soldermask areas with conformal coat material to repair damage.
use 3M Scotch-Weld # 1838 B/A Rf Epoxy Exp 2/20/06

Date Action Taken: 3-11-05 HY **Retest Results:**
Corrective Action Required/Performed on other Units ☐ Serial Number(s):

Closure Approvals

Subsystem Lead: _____ Date:
IMPACT Project Manager: _____ Date
IMPACT QA: _____ Date:
NASA IMPACT Instrument Manager: _____ Date:

Star bake 6:30pm 3/17/05
60C
Stop 8:00AM 3/18/05

1838 B/A green Epoxy Exp 2/20/06
Lot 3388J3A part A (green) 5 parts
3413J3A part B (white).

 HY 3/17/05

Date:

Completed by: HY **Date:** 3-14-05

QA Inspection by: RJ **Date:** 3-14-05

GSFC Inspection by: Richard D Rudy **Date:** 3/14/05

8) Install ferrite beads (BDS3.5/1.3/3.3/4S2) on Q3, Q6, Q11, Q18, Q14 and Q15 (Do NOT Install on Q20 and Q22. Their ferrite beads are installed on current transformers). P/C 0237 Ferrite beads are installed on source lead. RJ 3-16-05

Completed by: HY **Date:** 3-15-05

9) Solder transistors Q3, Q6, Q14, Q11, Q22, Q15, Q18, and Q20 (IRHF57130SCS) on the board

Completed by: HY **Date:** 3-15-05

9a Inspection of transistors will be from back side of board for source lead

10) Put shrink tubing around the ferrite beads that were removed at item #2 staking only

Completed by: N/A **Date:** 03/14/05 SSH. 5753-B Lot# HK4K 40-4646 Exp: 05/05 60.04g

11) Solder the wires on the board that were removed at item #3.

Completed by: HY **Date:** 3-16-05 5753-A Lot # HK4K PO-DJ1802 Exp: 06/05 12.05g 3/17/05 Cab-O-Sil 4.2g RJ

12) Record D/C of the 100K (RNC50H1003FR) resistors.

D/C: 9847

Completed by: HY **Date:** 3-14-05 Add start 3-15-05 SSH stop 3-16-05 3/17/05 6:00PM to next day 8:00AM

13) Plug new D58 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board. Record D/C below.

D58: JANTXV1N6642 H9847 D/C: H9847

Completed by: HY **Date:** 3-15-05

14) Connect the 100K resistor (lead side) on the anode side of D58 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-15-05

Date:

15) Install a post on E10.

Completed by: HY **Date:** 3-15-05

16) Connect the other side of the 100K resistor to E10.

Completed by: HY **Date:** 3-15-05

17) Plug new D59 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D59: JANTXV1N6642 D/C: 19847

Completed by: HY **Date:** 3-15-05

18) Connect the 100K resistor (lead side) on the anode side of D59 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-15-05

19) Connect the other side of the 100K resistor to E10. Insure

Completed by: HY **Date:** 3-15-05

E10 & E9 must remain connected. Therefore, connect E10 to the resistor using bus wire #32AWG. SSH. 3-16-05

20) Plug new D60 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D60: JANTXV1N6642 D/C: 19847

Completed by: HY **Date:** 3-15-05

21) Connect the 100K resistor (lead side) on the anode side of D60 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-15-05

22) Install a post on E22.

Completed by: HY **Date:** 3-15-05

E21 & E22 must remain connected. Connect E21 & E22 to the resistor using bus wire # 32AWG. SSH 3-17-05 3-17-05

23) Connect the other side of the 100K resistor to E22.

Date:

Completed by: HY **Date:** 3-15-05

24) Plug new D62 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not solder ...n the board on the board. Record D/C below.

D62: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-15-05

25) Connect the 100K resistor (lead side) on the anode side of D6... ...nd the anode (leaving at least 2x lead diameter distance) and cut th... ...de lead and the resistor. *Note: Avoid placing the additional resistor*

Completed by: HY **Date:** 3-15-05

26) Connect the other side of the 100K resistor to E22.

Completed by: HY **Date:** 3-15-05

27) Plug new D64 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D64: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-15-05

28) Connect the 100K resistor (lead side) on the anode side of D64 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-15-05

29) Install a post on E44.

Completed by: HY **Date:** 3-15-05

30) Connect the other side of the 100K resistor to E44.

E44 & E41 must remain connected. Connect E21 & E22 to the resistor using bus wire # 32AWG. 3-17-05 SSH

Completed by: HY **Date:** 3-15-05

31) Plug new D65 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

3-17-05

D65: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-15-05

Date:

32) Connect the 100K resistor (lead side) on the anode side of D65 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-15-05

33) Connect the other side of the 100K resistor to E44.

Completed by: HY **Date:** 3-15-05

34) Plug new D66 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D66: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-16-05

35) Connect the 100K resistor (lead side) on the anode side of D66 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-16-05

36) Install a post on E52.

Completed by: HY **Date:** 3-16-05

37) Connect the other side of the 100K resistor to E52.

Completed by: HY **Date:** 3-16-05

E52 & E51 must remain connected. Connect E52 & E51 to the resistor using bus wire #32AWG 3-17-05

38) Plug new D68 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

SSH 3-17-05

D68: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-16-05 SSH

39) Connect the 100K resistor (lead side) on the anode side of D68 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-16-05

Date:

40) Connect the other side of the 100K resistor to E52.

Completed by: HY **Date:** 3-16-05

41) Thoroughly clean the board.

Completed by: HY **Date:** 3-17-05

	QA Inspector	GSFC Inspector
Solder Inspection	3-21-05	
Part Orientation		
Layout		
Installation		

QA Inspection by: _____ **Date:** 3-21-05

GSFC Inspection by: _____ **Date:** 3/21/05

42) Apply staking material (Uralane 5753) to all additional resistors per NASA-STD-8739.1.

Lot # ~~40-4046~~ RJ 3-17-05

3-22-05 star 5753 9:00AM

Mix ratio: 1/29/05 **Expiration Date:** 5/05

Start Time: ~~9:00AM~~ (3-22-05) bake ↳ 5 ccpm **Stop Time:** 8:00AM (3-23-05) bake 60c

Completed by: HY **Date:** 3-22-05

43) Apply staking material on the wires per NASA-STD-8739.1

Completed by: HY **Date:** 3-22-05

44) Stake the ferrite beads on the transistor leads and the transistors (tri-star stake) per NASA-STD-8739.1 Ref step # 9 RJ 3-23-05

Completed by: HY **Date:** 3-15-05

45) Conformally coat all new diodes, resistors and the transistors using Uralane 5750.

Completed by: HY **Date:** 3-23,24-05

46) Take pictures of the completed rework/repair.

Completed by: **Date:**

Date:

Approved by: _____ **Date:** _____

Approved by: _____ **Date:** _____

QA Inspection by: _____ **Date:** _____

GSFC Inspection by: _____ **Date:** _____

Date:

2. **Corrective Action for TOP BOARD**

1) Remove transistors with reference designators Q10, Q12, Q19 and Q21 (IRHF57130SCS) from the top board. Do **NOT** use metallic tools to remove conformal coating.

Completed by: HY **Date:** 3-11-05

2) Remove burnt shrink tubing covering the ferrite beads. Record the location of removed ferrite beads.

no burnt shrink tubing

Completed by: HY **Date:** 3-11-05

3) Remove burnt wires. Record the location of removed wires.

no burnt wire

Completed by: HY **Date:** 3-11-05

4) Remove 1N6642 diodes with reference designator D67, D69, D61 and D63. Do **NOT** use metallic tools to remove conformal coating over the diodes

Completed by: HY **Date:** 3-11-05

5) Top board must be inspected by QA.

Completed by: RJ **Date:** 3-14-05

FS RJ 3-14-05

6) Prepare 4 100K (RNC50H1003FR) resistors on bench prior to soldering by cutting one side of the resistor's lead short and connecting #24AWG stranded insulated wire with lash splice. Use #30AWG bus wire to perform lash splice. The other lead will connect directly on the diode anode side. Have the lash splice inspected before placing shrink tubing

7) **Completed by:** HY **Date:** 3-14-05

QA Inspection by: RJ **Date:** 3-14-05

QA Inspection by: [signature] **Date:** 3/14/05

8) Install ferrite beads (BDS3.5/1.3/3.3/4S2) on Q10, Q12, Q19 and Q21. P/C 8237
Ferrite beads are installed on source leads of transistors. RJ 3-16-05

Completed by: HY **Date:** 3-15-05

Date:

9) Solder transistors Q10, Q12, Q19 and Q21 on the board.

9a) Inspection of transistors will be from backside of board for source lead only. **Completed by:** HY **Date:** 3-15-05 item N/A RJ 3-17-05 RJ 3-16-05

10) Put shrink tubing around the ferrite beads that were removed at item ~~#2~~ #3 RJ 3-16-05

Completed by: HY **Date:** 3-16-05

11) Solder the wires on the board that were removed at item #3.

Completed by: HY **Date:** 3-16-05

12) Record D/C of the 100K (RNC50H1003FR) resistors.

D/C: 9847

Completed by: HY **Date:** 3-14-05

13) Plug new D67 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board. Record D/C below.

D67: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-16-05

14) Connect the 100K resistor (lead side) on the anode side of D67 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-16-05

15) Install a post on ~~E56~~ E55 * RJ 3-17-05

Completed by: HY **Date:** 3-16-05

16) Connect the other side of the 100K resistor to E56.

Completed by: HY **Date:** 3-16-05

* E56 & E55 must remain connected. Connect E56 & E55 using #30 AWG bus wire with shrink tubing around the wire. SSH 3-17-05 RJ 3-17-05

17) Plug new D69 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board. Record D/C below.

D69: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-16-05

Date:

18) Connect the 100K resistor (lead side) on the anode side of D69 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-16-05

19) Connect the other side of the 100K resistor to E56.

Completed by: HY **Date:** 3-16-05

20) Form a pigtail on D61 anode. Solder D61. Record D/C below.

D61: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-16-05

21) Connect the 100K resistor (lead side) on the anode side of D61 and loop the resistor around. Solder the diode the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-16-05

22) Install a post on E32.

Completed by: HY **Date:** 3-16-05

23) Connect the other side of the 100K resistor to E32.

Completed by: HY **Date:** 3-16-05

E32 & E30 must remain connected. Connect E32 to E30 with buswire #30AWG use shrink tubing. SSH 3-17-05

24) Plug new D63 on its pads. **Do NOT SOLDER** until the resistor is connected on the anode side. Do **NOT** cut the leads of the diodes until the resistor is placed (not soldered) on the board on the board. Record D/C below.

D63: JANTXV1N6642 D/C: H9847

Completed by: HY **Date:** 3-16-05

25) Connect the 100K resistor (lead side) on the anode side of D63 and loop the resistor around the anode (leaving at least 2x lead diameter distance) and cut the diode lead. Solder the diode lead and the resistor. *Note: Avoid placing the additional resistors on traces.*

Completed by: HY **Date:** 3-16-05

Date:

26) Connect the other side of the 100K resistor to E32.

Completed by: HY **Date:** 3-16-05

27) Thoroughly clean the board.

Completed by: HY **Date:** 3-17-05

	QA Inspector	GSFC Inspector
Solder Inspection	3-21-05	
Part Orientation		
Layout		
Installation		

QA Inspection by: RJ **Date:** 3-21-05

QA Inspection by: _____ **Date:** _____

28) Apply staking material (Uralane 5753) to all additional resistors per NASA-STD-8739.1.

3-22-05 Staked 5753 9:00AM

Mix ratio: 1-20-05 **Expiration Date:** 5/05

Start Time: 5:00PM (3-22-05) **Stop Time:** 8:00AM (3-23-05) bake 60 C°

Completed by: HY **Date:** 3-22-05

29) Apply staking material on the wires per NASA-STD-8739.1

Completed by: HY **Date:** 3-22-05

30) Stake the ferrite beads on the transistor leads and the transistors (tri-star stake) per NASA-STD-8739.1

Completed by: HY **Date:** 3-25-05

31) Conformally coat all new diodes, resistors and the transistors using Uralane 5750.

Completed by: HY **Date:** 3-23,24-05

32) Take pictures of the completed rework/repair.

Completed by: **Date:**

Date:

Approved by: _____ **Date:** _____

Approved by: _____ **Date:** _____

QA Inspection by: _____ **Date:** _____

Date:

3. **Corrective Action for all Board with Repairs**

1) Add more points of staking along the repair wires especially where the wire changes direction per NASA-STD-8739.1

Completed by: **Date:**

2) Make sure all transistors have tri-star stake.

Completed by: _____ **Date:** _____

3) Apply staking to the leads of any transistors that are in dead-bug position. Apply tri-star staking to the transistors.

Completed by: **Date:**

4) Apply more staking to the capacitors per NASA-STD-8739.1

Completed by: **Date:**

5) Apply staking fillets to any parts that are laying on the board.

Completed by: **Date:**

6) Apply more staking to the wires that connect the thermistor to the top board (SLH and TH)

Completed by: _____ **Date:** _____

7) Apply more staking to the wires that lay between J1 connector and the OP_HTR and OP_HTR_RTN.

Completed by: _____ **Date:** _____

8) Apply more staking to the wires of the inductors and transformers.

Completed by:

9) Apply staking to cambion pins on top board.

Completed by: _____ ___

Date:

Approved by: _____ **Date:** _____

Approved by: _____ **Date:** _____

QA Inspection by: _____ **Date:** _____

GSFC Inspection by: _____ **Date:** _____

Delivered-To: ronj@apollo.ssl.berkeley.edu
Date: Fri, 11 Mar 2005 17:26:46 -0500
To: ronj@ssl.berkeley.edu
From: Mike Jones <mijones@pop700.gsfc.nasa.gov>
Subject: Wire removal
Cc: Ricardo.Rodriquez@honeywell-tsi.com, lgibb@pop400.gsfc.nasa.gov,
Lil Reichenthal <lreichen@pop700.gsfc.nasa.gov>
X-CanItPRO-Stream: admin
X-Spam-Score: 0 ()
X-Scanned-By: CanIt (www . canit . ca)

Ron,

Both Larry and myself agree with the decision to remove the two wires interconnecting the two boards to allow for ease of rework. And, later to reinstall at a later time in the PR instructions. Please red line your PR instructions (sign /date redline).

Thanks,
Mike Jones

APPENDIX 4: SEP LVPS TEST PROCEDURE

Part Number FM2 Serial Number _____ Date March 16, 2005

Operator Selda Heavner Inspector Ron Jackson 3-16-05

APPENDIX 4:

5. Post-Conformal Coat Tests: No load current = 0.17A

5.1 Weight Measurement

Weight: N/A grams

5.2 Functional tests Repeating Functional Test After PFR 1036

Presence of Output Voltages

Output Voltages				
Signal name	**Min**	**Max**	**Output**	**Unit**
SEPT-NS 5.3 Digital	5.04	5.57	5.716	V
SEPT-NS 2.6 Digital	2.47	2.73	2.545	V
SEPT-NS 5.6 Analog	5.32	5.88	5.35	V
SEPT-E 5.3 Digital	5.04	5.57	5.336	V
SEPT-E 2.6 Digital	2.47	2.73	2.55	V
SEPT-E 5.6 Analog	5.32	5.88	5.71	V
SIT HET LET +13 Analog	12.35	13.65	13.40	V
SIT HET LET -13 Analog	-13.65	-12.35	-13.5	V
SIT HET LET +6 Analog	5.70	6.30	5.9	V
SIT HET LET -6 Analog	-6.30	-5.70	-6.17	V
SIT HET LET 2.6V Digital	2.47	2.73	2.52	V
SIT HET LET 3.4V Digital	3.23	3.57	3.319	V
SIT HET LET +5.1V Digital	4.85	5.36	5.053	V
SIT HET LET -5.2V Digital	-5.46	-4.94	-5.16	V

Efficiency This section will not be performed after PFR 1036

Signal name	Voltage	Current	Power (W)
SEPT-NS 5.3 Digital			
SEPT-NS 2.6 Digital			
SEPT-NS 5.6 Analog			
SEPT-E 5.3 Digital			
SEPT-E 2.6 Digital			
SEPT-E 5.6 Analog			
SIT HET LET +13 Analog			
SIT HET LET -13 Analog			
SIT HET LET +6 Analog			
SIT HET LET -6 Analog			
SIT HET LET 2.6V Digital			
SIT HET LET 3.4V Digital			

Delivered-To: ronj@apollo.ssl.berkeley.edu
X-ASG-Debug-ID: 1111166069-15872-92-0
X-Barracuda-URL: http://mailwall.ssl.berkeley.edu:8000/cgi-bin/mark.cgi
Date: Fri, 18 Mar 2005 12:14:22 -0500
To: "Lillian S. Reichenthal" <Lillian.S.Reichenthal@nasa.gov>,
David Curtis <dwc@ssl.berkeley.edu>, ronj@ssl.berkeley.edu
From: Mike Jones <mijones@pop700.gsfc.nasa.gov>
X-ASG-Orig-Subj: Re: Fwd: SEP visual rejection items by GSFC.
Subject: Re: Fwd: SEP visual rejection items by GSFC.
Cc: lgibb@pop400.gsfc.nasa.gov, Laurie Kleppin <lkleppin@pop300.gsfc.nasa.gov>,
Ricardo.Rodriquez@honeywell-tsi.com,
"Rodriguez, Ricardo G" <Ricardo.Rodriguez@honeywell-tsi.com>
X-Virus-Scanned: by Barracuda Spam Firewall at ssl.berkeley.edu
X-Barracuda-Spam-Score: -5.40
X-Barracuda-Spam-Status: No, SCORE=-5.40 using global scores of TAG_LEVEL=1.0
QUARANTINE_LEVEL=3.0 KILL_LEVEL=1000.0 tests=BAYES_00
X-Barracuda-Spam-Report: Code version 2.64, rules version 2.1.1942
Rule breakdown below pts rule name description
---- ---------- ----------
-5.40 BAYES_00 BODY: Bayesian spam probability is 0 to 1%
[score: 0.0000]
X-Qmail-MasqDomain: False

Dave, Ron, and Lil,

Item #1 and #3 should be fine, recommend approval (valid findings).

Item #2 related photograph concerns me greatly.

I agreed that the leads could be used as terminals. However, the attaching conductor should have been in contact with the base, the pad in your case (standard practice). The way these conductor leads are at the end of the lead (terminal) brings much concern about lead fatigue (where solder joint to lead interfaces). Also, the shrink tubing is very short on the one side raising shorting concerns.

Currently, I do not recommend using as is. Need additional information from your team.

Please call, we need to talk/work this issue.

Regards,
Mike Jones
301-286-3198

X-Sender: dwc@apollo.ssl.berkeley.edu
Date: Thu, 17 Mar 2005 14:31:59 -0800
To: Lillian Reichenthal <lreichen@pop700.gsfc.nasa.gov>
From: David Curtis <dwc@ssl.berkeley.edu>
Subject: Fwd: SEP visual rejection items by GSFC.
Cc: Ron Jackson <ronj@ssl.berkeley.edu>
X-Proofpoint-Spam-Details: rule=notspam policy= score=0 mlx=-1 adultscore=0 adjust=0 engine=2.5.0-05031400 definitions=2.5.0-05031700

Lil:
The inspector rejected the FM2 SEP LVPS board for 3 issues listed below (see also attached pictures). Let me know if you want it written up on a PFR form. He agreed that these are really cosmetic, but wanted an official waiver. I authorized the board to proceed to conformal coat as is, with an MRB to run in parallel. I apologize for the focus on picture 17; it shows the splice of the resistor to the diode lead, the concern being how high the diode lead extends above the board. Picture 18 shows the poor strain relief (diode in the back). The other end of this diode has good strain relief, so we feel that there is not a real issue. Picture 18 also shows (poorly) the bridging of the diode lead by conformal coat (diode in front). It is not clear to me why this is an issue; Uralane is pliable enough that it should not impact strain relief.
Dave

Delivered-To: dwc@apollo.ssl.berkeley.edu
X-Sender: ronj@apollo.ssl.berkeley.edu
X-Mailer: QUALCOMM Windows Eudora Version 5.0
Date: Thu, 17 Mar 2005 14:10:28 -0800
To: David Curtis <dwc@ssl.berkeley.edu>
From: Ron Jackson <ronj@ssl.berkeley.edu>
Subject: SEP visual rejection items by GSFC.
X-Qmail-MasqDomain: True
X-Qmail-MasqDomain: True

Dave,
Item #1 The stress relief bend radius shall not be less than the lead diameter per NASA-Std-8739.3

Item #2 Straight-through termination, lead protrusion exceeds max (0.090 inch) per NASA-Std-8739.3

Item #3 Conformal coating bridges stress relief areas there negating stress relief NASA-Std-8739.1

Ron Jackson
UC Berkeley,Space Sciences Laboratory
7 Gauss Way MC 7450
Berkeley, CA 94720-7450

Tel: (510) 643-2625
AST:7731^29u18e3

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David Curtis
Space Sciences Laboratory
University of California at Berkeley
7 Gauss Way
Berkeley, CA 94720-7450
(510) 642-5998 FAX: (510) 643-8302

==========:
AST:7731^29u18e3

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Lillian Reichenthal
STEREO Instrument Manager

NASA Goddard Space Flight Center
Building 6, Room S126
Mail Code 463
8800 Greenbelt Road
Greenbelt, Maryland 20771

(office) 301-286-5634
(fax) 301-286-1696
(cell) 443-745-2716

Attachment converted: Macintosh HD:DSC00018.JPG (JPEG/JVWR) (0005EA0C)
Attachment converted: Macintosh HD:DSC00017.JPG (JPEG/JVWR) (0005EA0D)

Delivered-To: ronj@apollo.ssl.berkeley.edu
X-ASG-Debug-ID: 1111440409-11086-11-0
X-Barracuda-URL: http://mailwall.ssl.berkeley.edu:8000/cgi-bin/mark.cgi
X-Sender: lreichen@pop700.gsfc.nasa.gov
Date: Mon, 21 Mar 2005 16:26:45 -0500
To: David Curtis <dwc@ssl.berkeley.edu>,
Mike Jones <mijones@pop700.gsfc.nasa.gov>, ronj@ssl.berkeley.edu
From: "Lillian S. Reichenthal" <Lillian.S.Reichenthal@nasa.gov>
X-ASG-Orig-Subj: Re: More SEP LVPS
Subject: Re: More SEP LVPS
Cc: Ricardo.Rodriquez@honeywell-tsi.com
X-Virus-Scanned: by Barracuda Spam Firewall at ssl.berkeley.edu
X-ASG-Whitelist: BODY (AST:7731\^29u18e3)
X-Barracuda-Spam-Score: 0.00
X-Barracuda-Spam-Status: No, SCORE=0.00 using global scores of TAG_LEVEL=1.0
QUARANTINE_LEVEL=3.0 KILL_LEVEL=1000.0
X-ASG-Whitelist: BODY (AST:7731\^29u18e3)
X-Qmail-MasqDomain: False

Dear Dave, Ron, Ricardo,
Mike and Larry are both in meetings right now. Perhaps what Ron is suggesting is ok, however, can we add a piece of kapton to one of the wires to insure there isn't a short.

I'll give Ron a call.

Lil

At 1:08 PM -0800 3/21/05, David Curtis wrote:
Mike, Lil:
More on the SEP LVPS. Ricardo is concerned about the point where two resistors cross (see picture). The concern is that if the heat shrink tube moves the wires could short. Ron feels that once the boards are conformally coated we should be OK. Ricardo wants your opinion / buy-off. Please take a look and give Ron a call.
Dave

Attachment converted: Macintosh HD:DSC00005a.JPG (JPEG/JVWR) (0008FDFD)
==========
David Curtis
Space Sciences Laboratory
University of California at Berkeley
7 Gauss Way
Berkeley, CA 94720-7450
(510) 642-5998 FAX: (510) 643-8302
==========
AST:7731^29u18e3

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Lillian Reichenthal
STEREO Instrument Manager

NASA Goddard Space Flight Center
Building 6, Room S126
Mail Code 463
8800 Greenbelt Road
Greenbelt, Maryland 20771

(office) 301-286-5634
(fax) 301-286-1696
(cell) 443-745-2716

UCB / SPACE SCIENCES LAB

MIXING RECORD

DATE 3/23/05

MIXTURE S/N 001

1. MIXING PROCEDURE: SOP rework

LOCATION OF MIXING: ☐ ☐ OTHER

☐ PRELIMINARY WRITTEN PROCEDURE ATTACHED TO THIS RECORD

☐ MFR. INSTRUCTIONS OR SPECIFICATION COPY ATTACHED TO THIS RECORD.

☐ VERBAL INSTRUCTIONS

Mid Top — SPECIFICATION NO.

board — DRAWING NO.

bottom — MFG. MIXING INSTRUCTION

2. UNIT IDENTIFICATION

D/N S/N OTHER

3.

NO.	INGREDIENT	FURNISHED BY	MANUFACTURER	LOT NO.	MFG. DATE	EXPIR. DATE	PTS. BY WT.	WT. GRAMS	QA.
	E750 B			AK5AB80 95%	'05	7/05	100PBW 18PBW	15.02	
	E750A			2K4L13 804A	'05	7/05		2.71	
	Tolu							5grams	
	Methl								

4. DEGASSING PERFORMED ☐ YES ☐ NO Date: TOTAL WT. GMS.

(IF YES DESCRIBE HOW DEGASSING WAS DONE. INCLUDE TIME. TEMPERATURE. NO. OF CYCLES. ETC

5. MATERIAL CONDITIONING PERFORMED ☐ YES ☐ NO Date:

(IF YES. DESCRIBE HOW CONDITIONING WAS PERFORMED. INCLUDE MATERIAL PRE-HEATING, DILUTING, DRYING, ETC.)

6. APPLICATION PROCEDURE (LIST GENERAL PROCEDURE FOLLOWED. NOTE ALL DEVIATIONS FROM REQUIREMENTS)

Mix by hand Brush Coating

7. CURE stay bake 1/200RA Date: 3-27-05

8. CONTROL SAMPLE DATA (AS APPLICABLE)

Control sample No : 1 Dated: 3-23-0

9. REQUESTOR: NAME SECT ROOM PHONE

TECHNICIAN: Helen NAME ROOM PHONE

QUALITY ASSURANCE: NAME Stamp ROOM PHONE

10. REMARKS & LIMITATIONS

t completion copy to :
Requestor
QA/QC
Section Head

UCB / SPACE SCIENCES LAB

MIXING RECORD

DATE: 2/24/05 | sep rework | MIXTURE S/N: 002

1. MIXING PROCEDURE | LOCATION OF MIXING ☐ ☐ OTHER

☐ PRELIMINARY WRITTEN PROCEDURE ATTACHED TO THIS RECORD — Mild. Top — SPECIFICATION NO.

☐ MFR. INSTRUCTIONS OR SPECIFICATION COPY ATTACHED TO THIS RECORD. — board — DRAWING NO.

☐ VERBAL INSTRUCTIONS — Top — MFG. MIXING INSTRUCTION

☐

D/N S/N OTHER

3. MIXTURE INGREDIENTS

NO.	INGREDIENT	FURNISHED BY	MANUFACTURER	LOT NO.	MFG. DATE	EXPIR. DATE	PTS. BY WT.	WT. GRAMS	QA
	5750B			AK5AB80 95A	1/05	7/05	100 PBW 18 PBW	15.04	
	5750A			LK4L13 804A	1/05	7/05		2.7	
	Tolu Methol							5 grams	

4. DEGASSING PERFORMED ☐ YES ☐ NO Date: | TOTAL WT. GMS. 22.74 grams

(IF YES DESCRIBE HOW DEGASSING WAS DONE. INCLUDE TIME. TEMPERATURE. NO. OF CYCLES. ETC.)

5. MATERIAL CONDITIONING PERFORMED ☐ YES ☐ NO Date:

(IF YES DESCRIBE HOW CONDITIONING WAS PERFORMED. INCLUDE MATERIAL PRE-HEATING, DILUTING, DRYING, ETC.)

6. APPLICATION PROCEDURE (LIST GENERAL PROCEDURE FOLLOWED. NOTE ALL DEVIATIONS FROM REQUIREMENTS)

Mix by hand. Brush Coating

7. CURE

8. CONTROL SAMPLE DATA (AS APPLICABLE)

REQUESTOR: NAME / SECT / ROOM / PHONE

TECHNICIAN: Helen NAME / ROOM / PHONE

Stamp NAME / ROOM / PHONE

10. REMARKS & LIMITATIONS:

PLASTIC LAB