STEREO IMPACT

PROBLEM REPORT
PR-1005
SEP LVPS Top FM1
2004-04-27

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SEP LVPS	**SubAssembly :** Top Board
Component/Part Number: SEP_Top_F001	**Serial Number:** FM1
Originator: Selda Heavner	**Organization:** U.C. Berkeley
Phone : 510-643-8640	**Email :** selda@ssl.berkeley.edu

Failure Occurred During (Check one √)

v Functional test | Qualification test | S/C Integration | Launch operations

Environment when failure occurred:

v Ambient | Vibration | Shock | Acoustic
Thermal | Vacuum | Thermal-Vacuum | EMI/EMC

Problem Description

During first power-on of the SEP LVPS Top Board did not produce output voltages 2.5V and 3.4V. Each voltage is generated from a separate LTC1877 regulator.

Analyses Performed to Determine Cause

The SYNC signal of LTC1877 should not receive any negative voltages. The Schottky Diode 1N5711-1 does not prevent negative voltages. When the SYNC signal pin goes negative the LTC1877 turns off. This is a design problem, not a layout issue.

Corrective Action/ Resolution

Rework | v Repair | Use As Is | Scrap

1. Remove D79
2. Remove R69
3. Remove C99
4. Install a 2N2222A transistor as shown in Figure 1.
5. Connect the collector (Pin3) of Qnew1 to the cathode pad of D79
6. Connect the emitter (Pin1) of Qnew1 to the anode pad of D79
7. Connect a 2.49KΩ (Rnew2) resistor to the base of Qnew1 and to C99 (RNC50H2491DS)
8. Connect a 4.99KΩ (Rnew1) resistor from C91A (5.1V side) to SYNC of U19 (Figure 2 and 3) (RNC50H4991DS)
9. Use shrink tubing where the leads are exposed.
10. During staking process stake, Qnew1, Rnew1, Rnew2 and the Rnew2 feed-through hole.
11. Update the schematics with the changes made to the design.

See attached photos of the post-repair and pre-coat, pre-stake photos. The transistor was deadbugged, shrink tubed and staked at the wires. A lash splice was used to make the repair. The schematics wer e updated and the fix was applied to FM2. Board level and then system level LVPS testing was successful.

Date Action Taken: 2004-4-23 **Retest Results**: Success

Corrective Action Required/Performed on other Units v Serial Number(s): FM2

Closure Approvals

Subsystem Lead: _____ Date:_____
IMPACT Project Manager: _____ Date _____
IMPACT QA: _____ Date:_____
NASA IMPACT Instrument Manager: _____ Date:_____

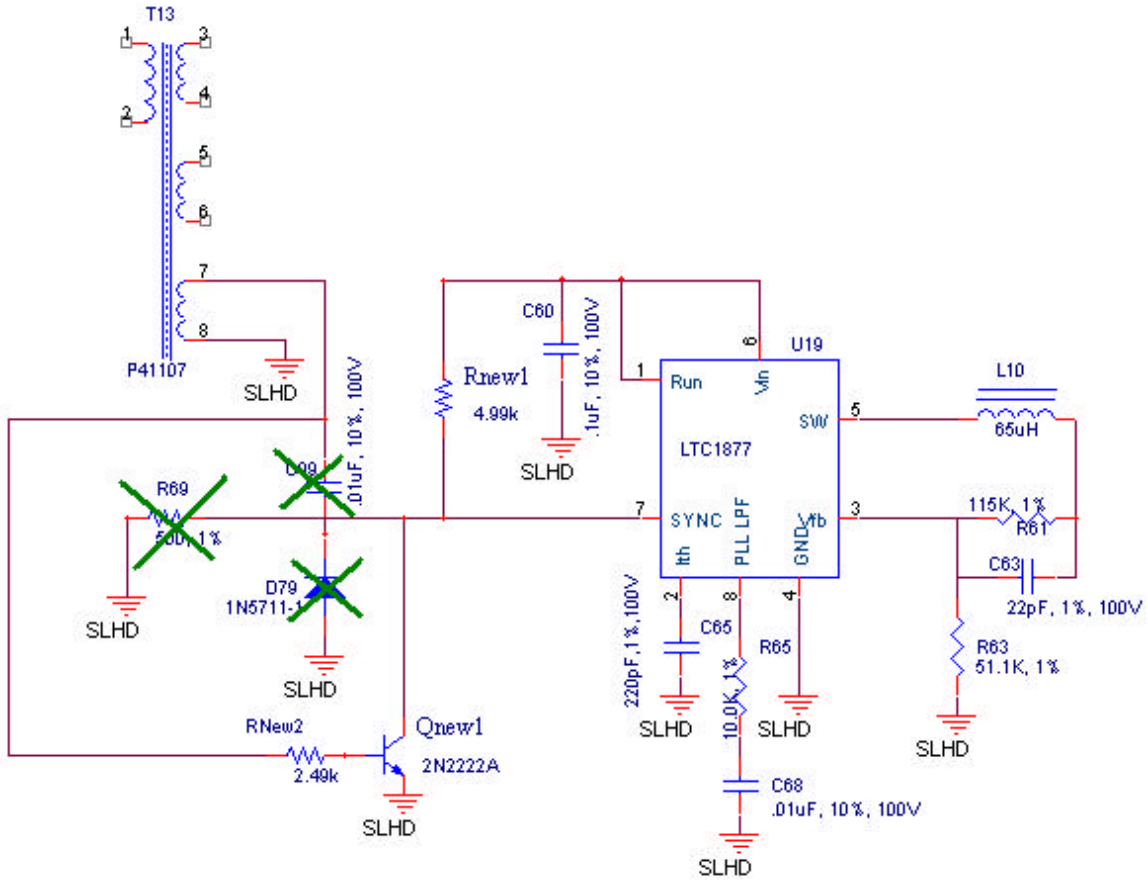


Figure 1: SEP LVPS Top board Schematic

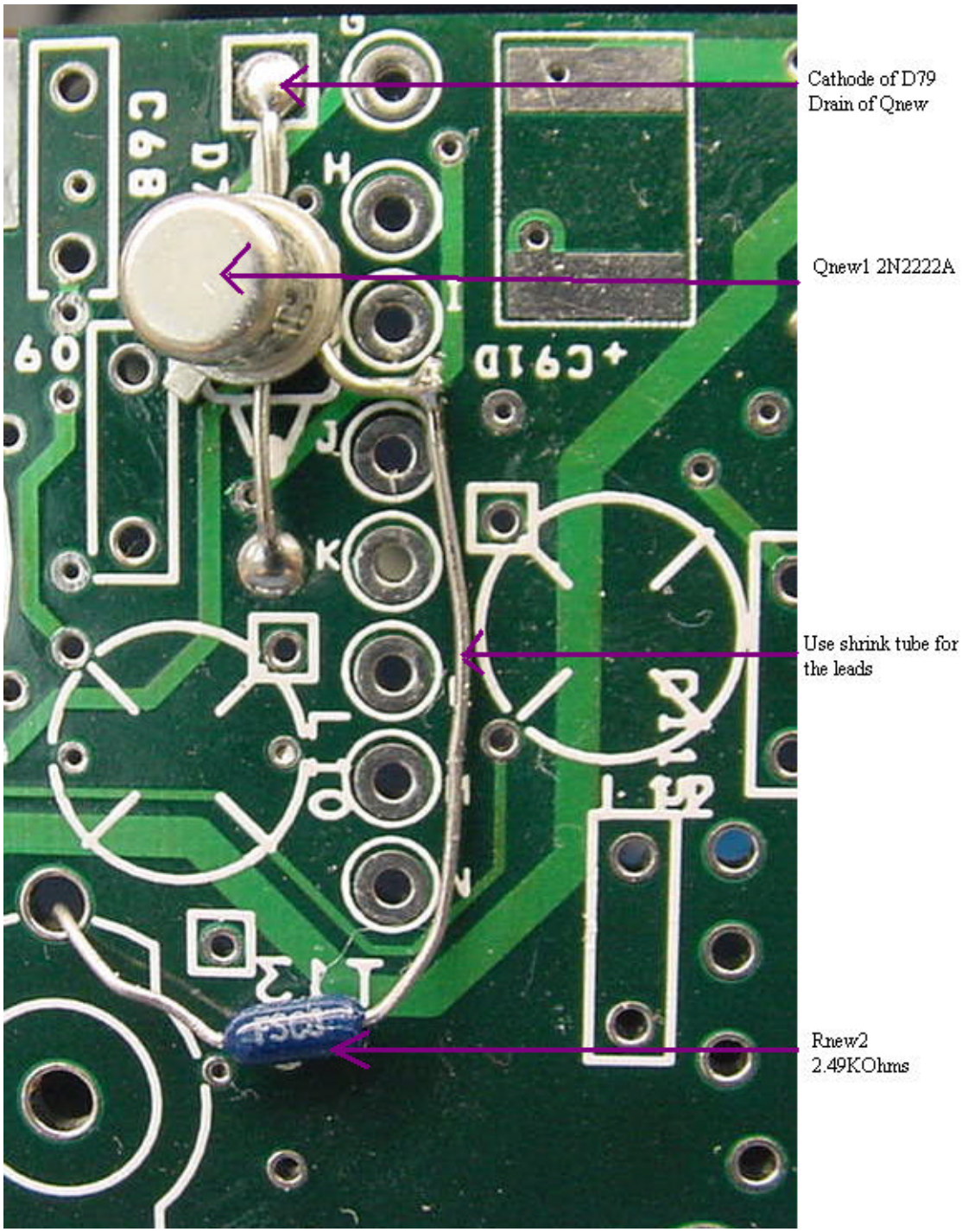


Figure 2: SEP LVPS Top Board Proposed Solution for PR-1005 (view from bottom)

Note: Soldering and wires shown in the figure are for information only. Proper wire and soldering technique will be used.

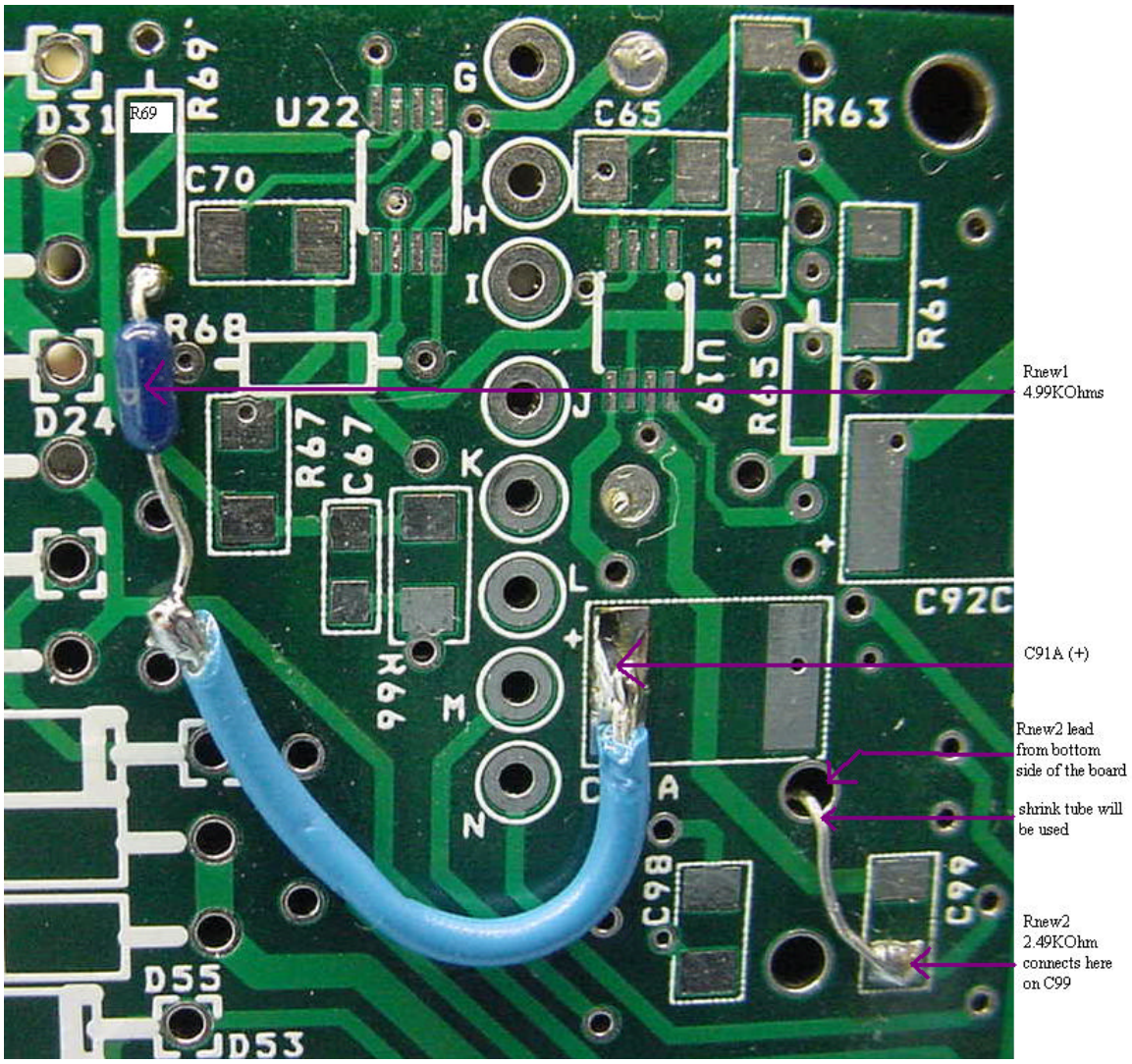
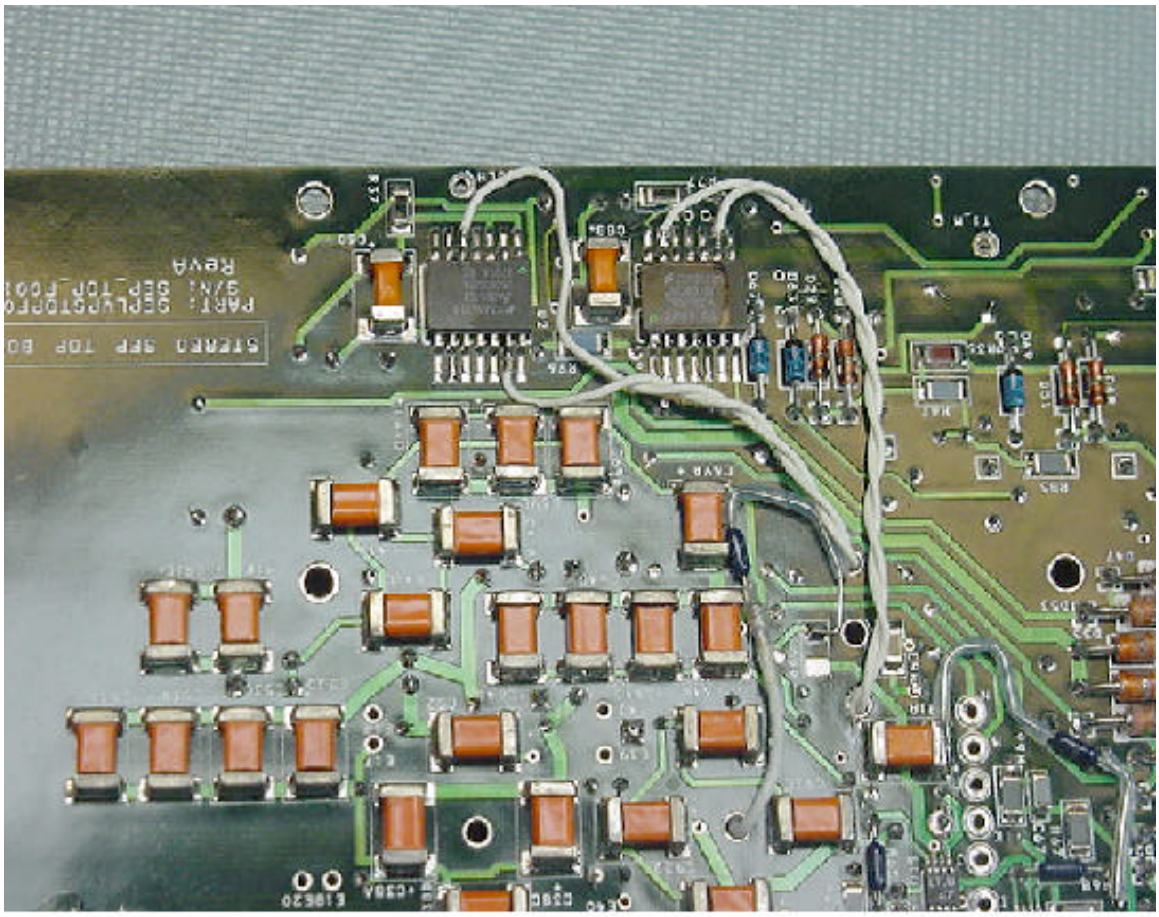


Figure 3: SEP LVPS Top Board Proposed Solution for PR-1005 (view from top)

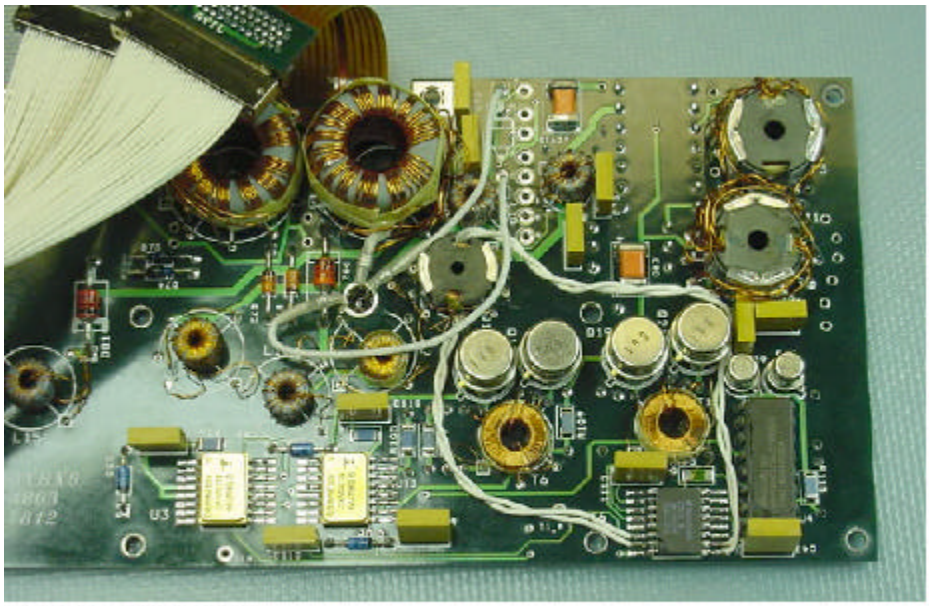
Note: Soldering and wires shown in the figure are for information only. Proper wire and soldering technique will be used.

SEP LVPS Board Top View – Post repair, pre-coat, pre-stake photos.



SEP TOP FROM TOP VIEW

SEP LVPS Top Board – Bottom View (post repair, pre-coat, pre-stake)



TOP BOARD FROM BOTTOM VIEW