C.3.5 SEP Common Electronics

C.3.5.1 Introduction

The SEP Common Electronics includes the various electronic systems shared by the SEP instrument suite. These systems include the SEP Data Processing Unit (SEP DPU), the Solid State Detector (SSD) Bias Power Supply, and the common SEP Ground Support Equipment (SEP GSE). The SIT HVPS and the front-end electronics of each of the SEP instruments are not included here since they are covered earlier in section C.3. The Low Voltage Power Supply is also not included, since it is covered in section C.1.

C.3.5.2 SEP Data Processing Unit

The SEP instrument suite will be served by a common Data Processing Unit (SEP DPU). This DPU will be similar in design to the DPUs used for the CRIS and SIS instruments on NASA's ACE mission. In the following sections, the tasks which the SEP DPU will perform for the SEP instruments are described, a functional description is given, and a development plan is laid out.

C.3.5.2.1 Requirements. The SEP DPU will fulfill the following requirements for the SEP instrument suite:

- Acquire event data from the HET, LET, and SIT instruments.
- Acquire rate/count data from the SEPT instrument.
- Acquire hardware rate scalar data from HET, LET, and SIT.
- Acquire analog housekeeping data.
- Perform routine instrument control functions as needed.
- Perform LET, HET, SEPT, and SIT Onboard Data Processing, per algorithms supplied by instrument science teams.
- Provide burst mode data from SEPT to the IDPU when a burst mode trigger is received.
- Select a subset of HET, LET, and SIT raw events for inclusion in telemetry to ground.
- Format processed data and selected raw events into CCSDS packets and feed them to IMPACT Instrument Data Processing Unit (IDPU).
- Control operating modes of SEP instruments.
- Decode and execute commands received via the IMPACT IDPU.

C.3.5.2.2 Functional Description. The heart of the SEP DPU will be a Harris RTX 2010 radiation-hard microprocessor, running at 8 MHz. The processor will be running the same version of the Forth real time operating system as was used for the CRIS and SIS instruments on ACE. The SEP DPU will operate and collect data from the four SEP instruments via similar serial interfaces. Packetized data, pre-formatted for telemetry, will be periodically sent to the IMPACT IDPU via a serial interface. Infrequent commands will be received from the IMPACT IDPU.

Since the volume of data generated by LET, HET and SIT will far exceed the allowed telemetry bit-rate, the most important function of the SEP DPU will be the categorization of events from these instruments into Z x E response matrices, which can then be telemetered periodically. In addition, the SEP DPU will use a priority scheme to select a small fraction of events for inclusion in the telemetered data stream. For SEPT, the very high electron rates will be counted in the SEPT front-end electronics, and no pulse-height events will be passed on to the SEP DPU. The SEP DPU will perform summing and compression of the SEPT rates before they are included in telemetry. Figure C.3.5-1 summarizes the event-processing functions of the SEP DPU hardware and software.

C.3.5.2.3 Development Plan

C.3.5.2.3.1 Trades in Progress. The hardware definition of the SEP DPU and associated interfaces and data transfer protocols are ongoing. Every effort is being made to provide ample margins for the key resources: RAM, EEPROM and processing cycles. The interface designs and protocols are being designed for relaxed response time requirements to ease the later software development tasks. The SEP DPU is being designed for minimum power dissipation by careful component selection. Improvements in power dissipation for static RAM have allowed us to increase the baseline DPU clock frequency from 4 to 8 MHz. The option to return to 4 MHz, with some power savings, will be held open until later in the development when CPU demands are better known.

C.3.5.2.3.2 New Technology Development and Descope Options. The SEP DPU requires no new technology. As mentioned above, the clock frequency may be reduced to save power if CPU resource demands allow.

C.3.5.2.3.6 Integration with Instruments and their Front-end Electronics. The final integration of the instruments and SEP DPU will occur at Caltech. However, SEP DPU simulators will be provided by Caltech to the instrument developers early in the program and will include fully functional interfaces, software to operate these interfaces, and complete documentation. Caltech personnel will accompany the delivery of the simulators to the instrument developers and aid in the initial integration of the simulators and instruments.

C.3.5.2.3.7 Interface with the IMPACT IDPU. This interface is described in detail in the UCB document "STEREO IMPACT Intra-Instrument Serial Interface" (D. Curtis).

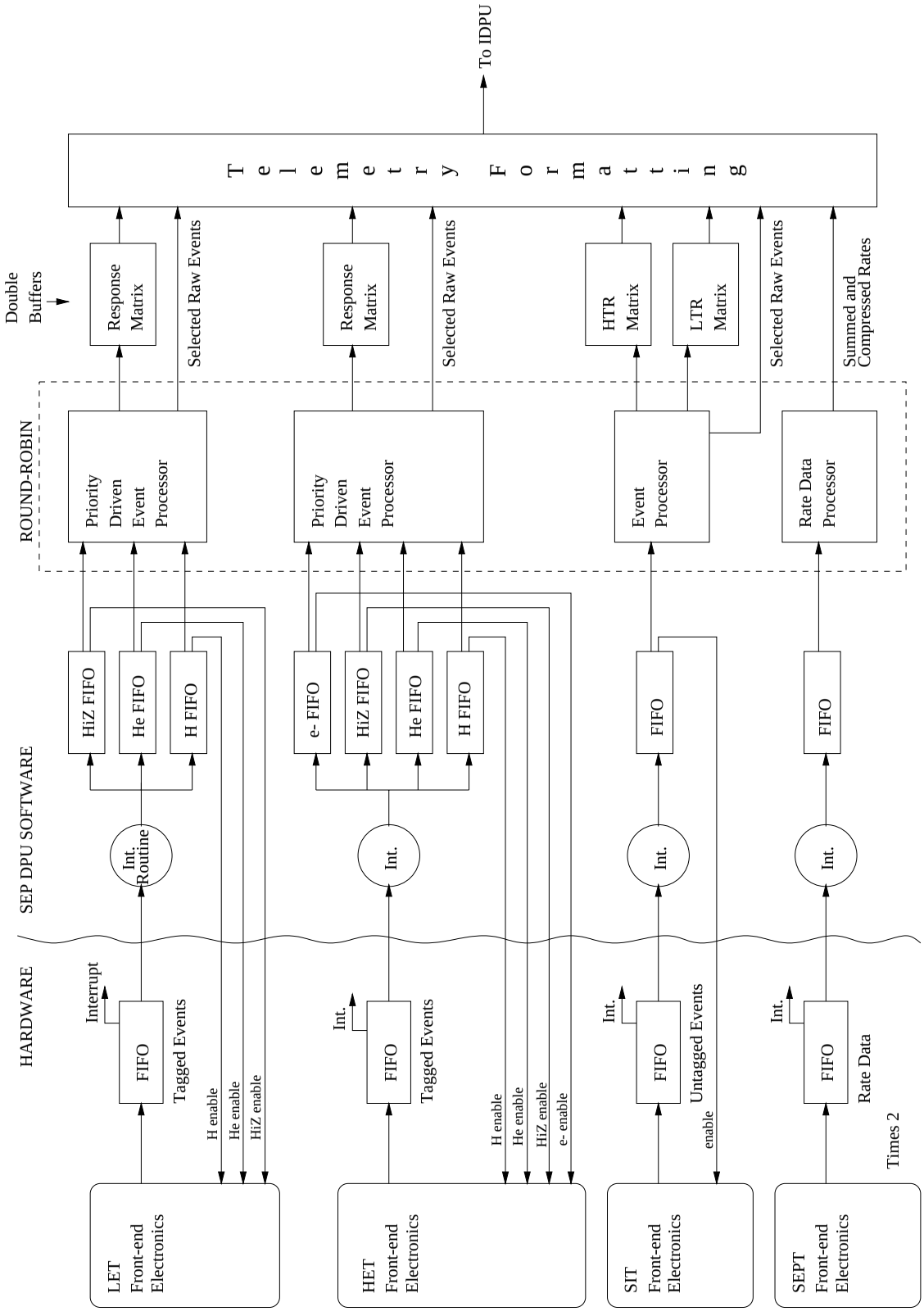

Figure C.3.5-1. SEP Event (and SEPT rate data) Processing

The SEP DPU will communicate with the IMPACT IDPU via a three-wire serial digital interface, providing CLK, CMD and TLM signals. A continuous 1 MHz clock signal (CLK) provided by the IDPU will synchronize command and data transfers. Data from the SEP instruments will be formatted into blocks of 16-bit words and passed to the IDPU on the TLM signal wire. Command packets for SEP will be passed on the CMD signal wire. These command packets will be passed on by the IDPU as received from the spacecraft. The CMD signal will also be used by the IDPU to send UT time codes and one-second spacecraft clock ticks to SEP for time-stamping of SEP telemetry packets. An IMPACT DPU simulator will be provided by UCB to Caltech early in the program for verifying the interface operation well before delivery of the SEP instrument/DPU suite to UCB.

C.3.5.2.3.8 Special Facilities Plan. No special facilities are required for development of the SEP DPU.

C.3.5.3 SEP SSD Bias Supply

The SSP SSD bias power supply will provide DC bias voltages to all the solid state detectors in the SEP instrument suite.

C.3.5.3.1 Requirements. The SSD Bias supply requirements are summarized in Table C.3.5-1.

SSD Name	Nominal Bias (V)	Bias Range Min (V)	Bias Range Max (V)	Wafer Quantity	Wafer Thickness (μm)	Instrument
L1	10	2	30	10	15	LET
L2	30	5	50	2	50	LET
L3	250	50	250	2	1000	LET
H1-6	250	50	250	9	1000	HET2
SSD	150	150	200	1	500	SIT
D1-8	-40	-30	-60	8	300	SEPT (center)
G1-8	-40	-30	-60	8	300	SEPT (guard)

Ripple	Spikes	Accuracy
mVpp	mVpp	V
0.2	1	+/- 1.0

Table C.3.5-1 SSD Bias Supply Requirements

Note: the SEPT detector bias shall have 16 short-circuit proof output lines for 8 detectors and their guard rings.

C.3.5.3.2 Functional Description. SEP solid state detectors operate in the reversed-bias diode mode and the bias supply will provide the DC voltage biases listed in Table C.3.5-1. Due to the mission's mass and power constraints, the bias supply will have six fixed output voltages rather than controllable voltages. The optimal voltage setting for each of the six outputs will be based on detector test results and implemented by replacing a few passive trim components. The individual outputs will be short-circuit protected but not switchable separately, again due to mass constraints.

Detector leakage current, as the primary load of the bias supply, is relatively small, but it is directly proportional to the temperature and detector health. The bias supply will have a safe power margin in order to accommodate temperature variations and detector degradation due to radiation over the expected mission life. Stand-by power consumption for each of the six outputs will be 10 mW/output, and total maximum power consumption (at high temperature, ~35 degC, and at the mission's end) will be 140 mW, assuming 75% efficiency. The bias supply will be packaged on two PCBs with components facing inward, with overall package dimensions of 5.3" x 3.3" x 1.3", total mass of 130 g (without shield).

C.3.5.3.3 Development Plan. Currently, the most promising sub-contractor for developing the bias supply is Space Instruments, Inc. with extensive experience in bias supply design and manufacturing. SI was the bias supply sub-contractor on the SAMPEX and ACE missions. SI will design, build and test a breadboard prototype for a proof of concept, then proceed to deliver engineering models and flight units including the documentation package to Caltech for SEP system integration and environmental testing. The bias supply resource figures stated in section C.3.5.3.2 were provided by SI. As was the case on the previous missions, SI will work closely with the Caltech and GSFC teams to meet the functional and packaging requirements of the bias supply.

C.3.5.4 SEP Ground Support Equipment (SEP GSE)

The SEP GSE will perform full functional tests of the SEP instruments and the SEP Common Electronics, as well as collect, analyze, and display the output data stream. The SEP GSE will accommodate the high data rates associated with integration/test operating modes, accelerator calibrations (if any) and burst-mode operation. The SEP GSE will have the capability to acquire data from the SEP DPU or DPU simulator directly, or via the IMPACT IDPU simulator, or via a network connection to the Berkeley IMPACT GSE. When connected directly to the SEP DPU or to the IMPACT IDPU simulator, the SEP GSE will have the capability to send commands to the SEP DPU.

C.3.5.5 Software Development Plan

Caltech and GSFC will be responsible for developing the flight software for the SEP DPU, while JPL personnel will be responsible for the SEP GSE software. These groups have had considerable experience developing real time processor-based

systems and GSEs for spaceflight use, most recently for the CRIS and SIS instruments on ACE.

Software development will be by a small team of Caltech, GSFC and JPL personnel, in close consultation with the SEP instrument teams and the IMPACT IDPU development team at UCB. Before flight code is written, a set of software requirements will be defined and documented to a level sufficient for a programmer to begin implementation. These requirements will be defined through consultations with the instrument teams, and will include algorithms defining the onboard processing of SEP instrument science data, and the display of those data on the GSE.

Caltech/JPL will be responsible for maintaining and testing the software, implementing a configuration control and backup plan, and responding to internal and external design reviews.

C.3.5.6 Management Processes

C.3.5.6.1 Roles and Responsibilities. Caltech/JPL and GSFC will be responsible for the design, assembly, software development, and testing of the SEP Common Electronics. E. Stone will direct the overall effort; R. Mewaldt, D. Reames, T. von Rosenvinge, and M. Wiedenbeck will provide science inputs to the design; A. Cummings will manage the effort.

W. Cook will be the chief engineer and have overall responsibility for the design. He will also code most of the flight software related to the interface with the SEP instruments. B. Kecman will serve as lead electrical engineer and be responsible for the assembly and testing effort of the electronics. GSFC and/or Caltech programmers will code the flight software related to the onboard data processing and data formatting. SEP investigators from each of the SEP instruments will provide science inputs and software requirements (algorithms) for the onboard data processing.

At JPL, M. Wiedenbeck will be responsible for the design of the SEP GSE, and R. Radocinski will code most of the GSE software.

C.3.5.6.2 Heritage..The SEP DPU and some of the onboard software will be derived from the CRIS and SIS processors successfully flown on ACE and previous similar projects. W. Cook and B. Kecman both worked on the CRIS and SIS flight processors, and both will also be working on the SEP Common Electronics. SEP GSE software development will draw on experience gained by M. Wiedenbeck and R. Radocinski in the development of the CRIS and SIS GSEs for ACE. The design of the SSD Bias Supply will be derived from the design of similar power supplies used on the ACE and SAMPEX missions.

C.3.5.6.3 Product Assurance and Safety Plans. Caltech, JPL, and GSFC will follow the Performance Assurance Implementation Plan for the STEREO IMPACT Instrument Suite.

C.3.5.6.4 Planning and Interface with the rest of the IMPACT Team. W.Cook will consult with D. Curtis on issues involving the electrical interface with the IMPACT IDPU. W. Cook, B. Kecman and A. Davis will consult with the SEP instrument teams on issues involving the electrical interface with the SEP instrument suite, the SSD Bias Supply, and the software requirements for onboard data processing. M. Wiedenbeck and R. Radocinski at JPL will consult with the SEP instrument teams on issues involving the monitoring of SEP instruments with the SEP GSE.

Regular IMPACT conference calls and meetings are scheduled to ensure the coordination between the groups.

C.3.5.7 Long Lead Items Plan

The following long lead items have been identified: *SRAM.* 4Mbit (512k x 8) 3.3V, monolithic Lockheed Martin die, 22 weeks delivery, rad-tolerant to 100krad. Similar Honeywell die is much more expensive, 20-24 weeks delivery. *EEPROM* 1Mbit (128k x 8) 5V, monolithic Hitachi die packaged in normal or shielded package, 16 or 20 weeks delivery, 30-50krad inherently rad-tolerant w/o shielding, by Austin Semiconductors, Inc. or Space Electronics, Inc. *FPGA* Actel RT54SX32 0.6 micron family, 3.3/5V, 14 weeks delivery, rad-tolerant to 80krad, lot tested; or Actel RT54SX32S 0.25 micron family, 3.3/5V, will be available in Q1 of 2001. *Microprocessor.* 16-bit, low-power, rad-hard, RTX2010, 5V, in stock at Caltech, heritage parts from ACE mission.

C.3.5.8 Breadboard, engineering model plans

The SEP electronics will consist of the following units:

- Analog/Post-regulator board
- SSD Bias Supply
- Low Voltage Power Supply
- Logic board
- Motherboard

The Analog/Post-reg. board and SSD Bias Supply will be developed by a reliable sub-contractor, Space Instruments, Inc., based on the heritage design used on SAMPEX and ACE missions. Because of that, only a portion of the SSD Bias Supply will be breadboarded for a proof of concept. Design of the Analog/Post-regulator board and SSD Bias Supply will be verified on EM PCBs which will be laid out with flight surface-mount parts and footprints in mind. The EM boards will be bench-tested in stand-alone fashion before being delivered to Caltech for further system integration and test. Eventually, we will have two EM units of each type, to interchange with flight boards during testing and integration.

The Low Voltage Power Supply will be developed by UC Berkeley based on a common design for several IMPACT suites. An EM unit will be built and delivered to Caltech for SEP system-level

integration and testing. Eventually, two such EM units will be needed. Dummy loads will simulate those sub-systems that are not present, and when EM LVPS unit is not there we will have means of connecting lab power supplies to the card-cage.

Logic board development is already under way at Caltech due to the fact that the SEP CPU simulator is being designed and multiple copies will soon be made for distribution to the SIT, SEPT and IDPU teams. One EM board will be built for a proof of concept, with EM parts closely matching the flight packages, but eventually two EM Logic boards will be built. A very useful feature in EM development is the fact that Actel EM parts don't have to be soldered onto EM boards. There is a ZIF socket that has the same footprint as the Actel PQFP part, and the socket is soldered to the EM board. We are in the process of making a common footprint and lead-forming tool for the flight CQFP parts that would fit the footprint of the EM part and the ZIF socket.

The Motherboard will initially be wire-wrapped in the back of a card-cage which will have grooves for the units described above that comprise the SEP Electronics. The units will have edge connectors to plug orthogonally into the motherboard's heat-activated ZIF connectors. Similarly, other SEP sub-systems plug into the motherboard with flexy-strips that end with an edge-connector tab. This concept eases the testing and integration schedule by giving more flexibility and quicker response over other types of connectors. No EM Motherboard will be built, but rather flight units will be designed when all interfaces have been tested on the breadboard version.

C.3.5.9 ITAR concerns

Caltech is responsible for developing the SEP DPU, which must supply the SEP instruments with low-voltage power and bias voltages for the solid-state detectors. In addition, the SEP DPU will command the instruments and receive digital and analog data, which must be formatted into the telemetered data stream. The SEPT instrument is being provided by the University of Kiel and ESTEC. Currently we are unable to have any meaningful technical discussions with their engineers until we get TAAs in place. We have begun to write the TAAs, but it may be many months before approvals are in place and all the requisite signatures are obtained. In the meantime, valuable schedule time is being lost. We are also expending considerable resources in defining these TAAs, for which we did not budget in our proposal, as the ITAR issue only came to our attention after we were selected for this mission.

We are assuming that GSFC will handle all our hardware exchanges for SEP and thus we are seeking licenses only for the exchange of technical data.