

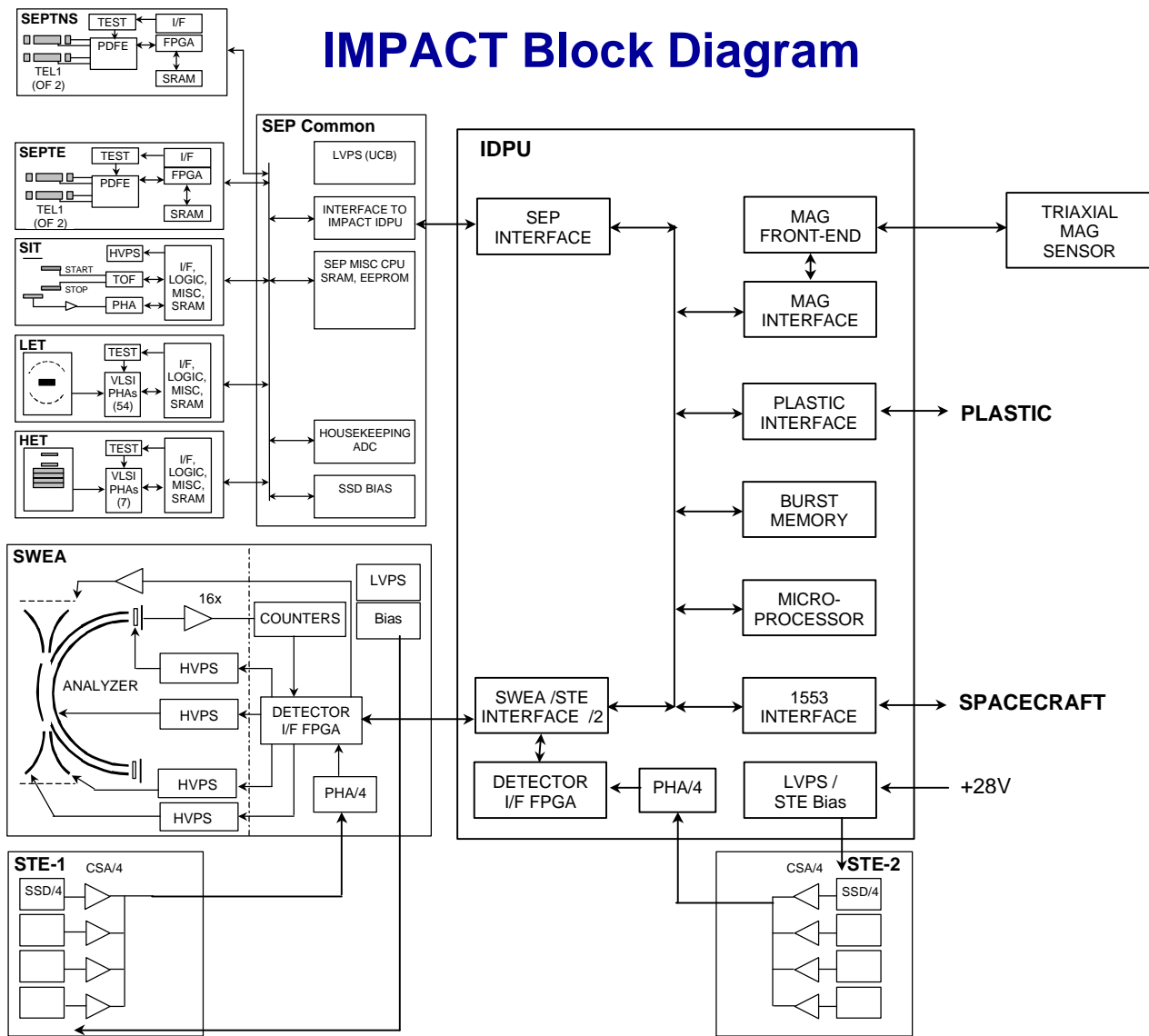
STEREO IMPACT

**IDPU Peer Review
2001-August-1, U.C.Berkeley**

STEREO IMPACT

IDPU Peer Review
2001-August-1

IMPACT Block Diagram



IDPU Requirements

- **A single-point interface between the IMPACT and PLASTIC instruments and the spacecraft C&DH system (1553 bus)**
- **Provide instrument control, data collection, compression, and formatting for the IMPACT and PLASTIC instruments**
 - **Note SEP has its own processor, so the IDPU acts mostly as a bent pipe for commands and telemetry to SEP**
- **Provide a home for miscellaneous instrument electronics, such as the MAG front end and the second STE front end**
- **Provide a common design, simple serial interface to the instruments tailored to meet the instrument needs**
 - **Instrument mode commands**
 - **Instrument data collection**
 - **Common sample and spacecraft timing distribution**
- **Provide a 2Mbyte Burst Memory to record short intervals of high time resolution data**

IDPU Interfaces

- **Spacecraft 1553 Interface**
 - Command, Telemetry, Status, Timing
 - SWAVES Burst Trigger Exchange
 - RT to RT once a second in each direction
- **Spacecraft 28V power interface**
 - powers IDPU, MAG, Sunward STE
- **Serial Instrument Interfaces**
 - SEP, PLASTIC, SWEA/STE
 - MAG and Sunward STE interfaces to internal cards
- **MAG Sensor Interface**
 - To MAG Front End Card in IDPU
- **Sunward STE Interface**
 - To STE Front End card in IDPU

IDPU Resources

IDPU:	Mass, kg	Power, W	Telemetry, bps
Mag Card	0.30	0.38	
DIB Card (STE)	0.30	0.20	
DPU Card	0.30	0.80	
S/C Interface (on DPU card)		1.70	
IDPU LVPS	0.20	1.71	
Mag Heater Control	0.07		
BOX	0.96		
IDPU Total:	2.12	4.89	748

IDPU:	Packet Header	50
bps	Packet Collect Time	50
	Housekeeping	32
	Playback Beacon	32
	Burst Playback	584
	Total	748

IDPU Responsibilities

- **System Design – Dave Curtis**
- **MAG Analog – GSFC / Mario Acuna**
- **MAG Heater – GSFC / Mario Acuna**
- **LVPS – Peter Berg**
- **Data Controller Board, FPGAs – Elf / Dorothy Gordon**
- **STE Detector Interface Board – Steve McBride**
- **Mechanical Design – Heath Bersch**
- **Flight Software – Dave Curtis**
- **EGSE:**
 - **IDPU Simulator Hardware – Elf / Dorothy Gordon**
 - **IDPU Simulator Top Level Software – Mike Hashii**
 - **IDPU Simulator SWEA, STE, MAG Software – Mike Hashii**
 - **IDPU Simulator PLASTIC Software – UNH**
 - **IDPU Simulator SEP Software - Caltech**
 - **Command & Display GSE – Mike Hashii**
 - **SWEA, STE, MAG Science Displays – Mike Hashii**
 - **SEP Science Displays – Caltech**
 - **PLASTIC Science Displays - UNH**

Controlling Documents

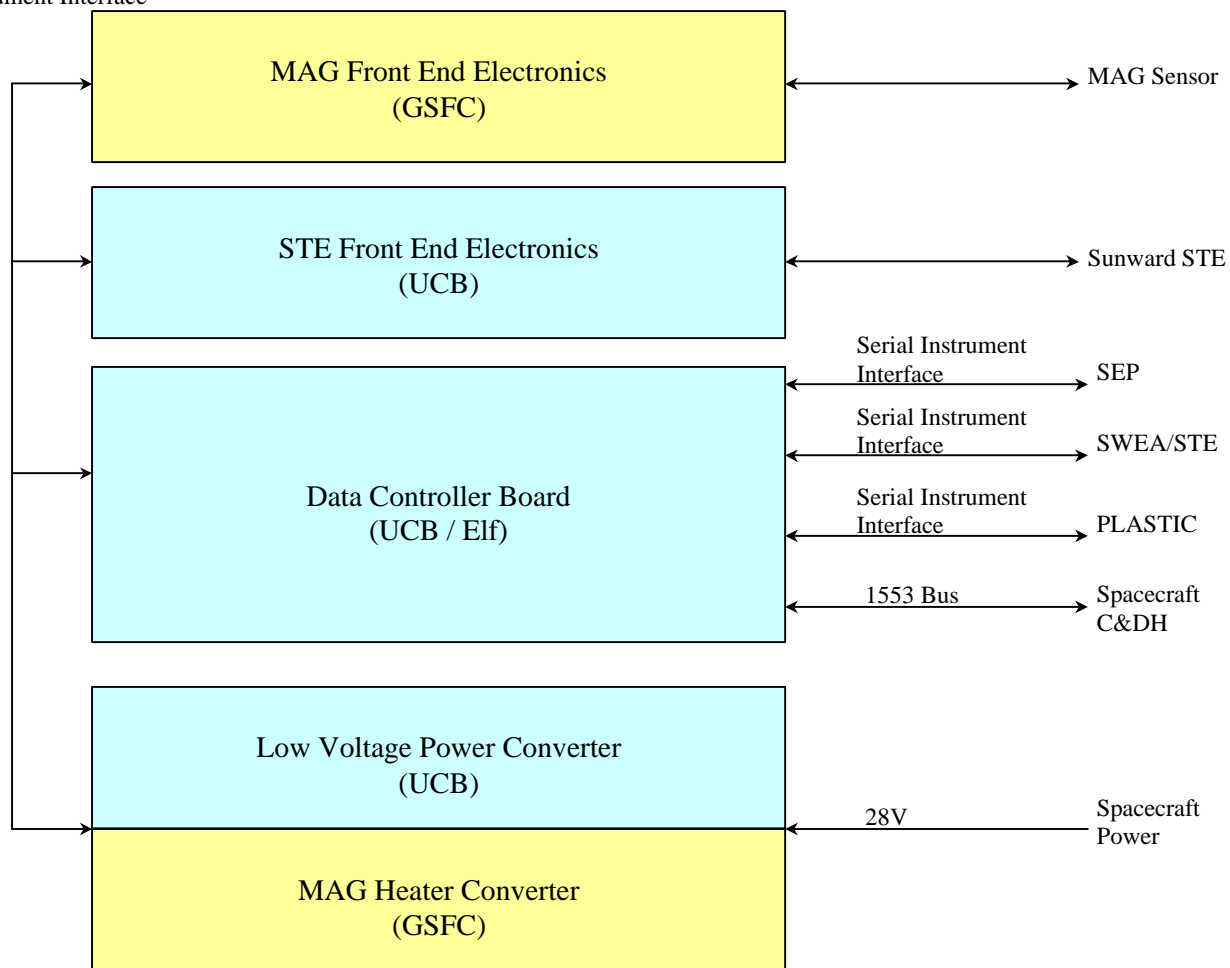
- **IMPACT Performance Requirements Document covers Science Requirements on the IMPACT Suite**
- **IMPACT / Spacecraft ICD covers the spacecraft interface**
- **IMPACT Serial Interface document (ICD) covers the data interface between Instruments and the IDPU (including PLASTIC)**
- **IMPACT PAIP covers the performance assurance requirements**
- **STEREO EMC and Contamination Control plans**
- **IDPU Specification Document describes the IDPU (Data Controller Board) Hardware**
- **IDPU Software Requirements Document describes the Flight Software Requirements**
- **IDPU Simulator Specification covers the IDPU Simulator GSE Hardware**

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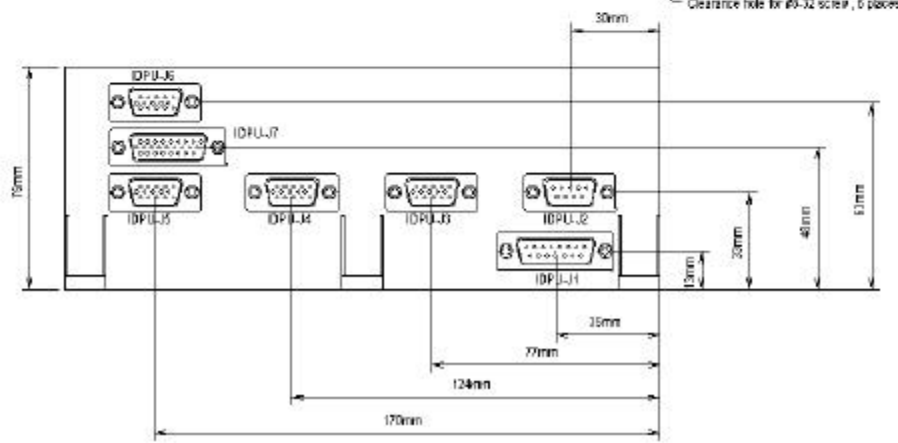
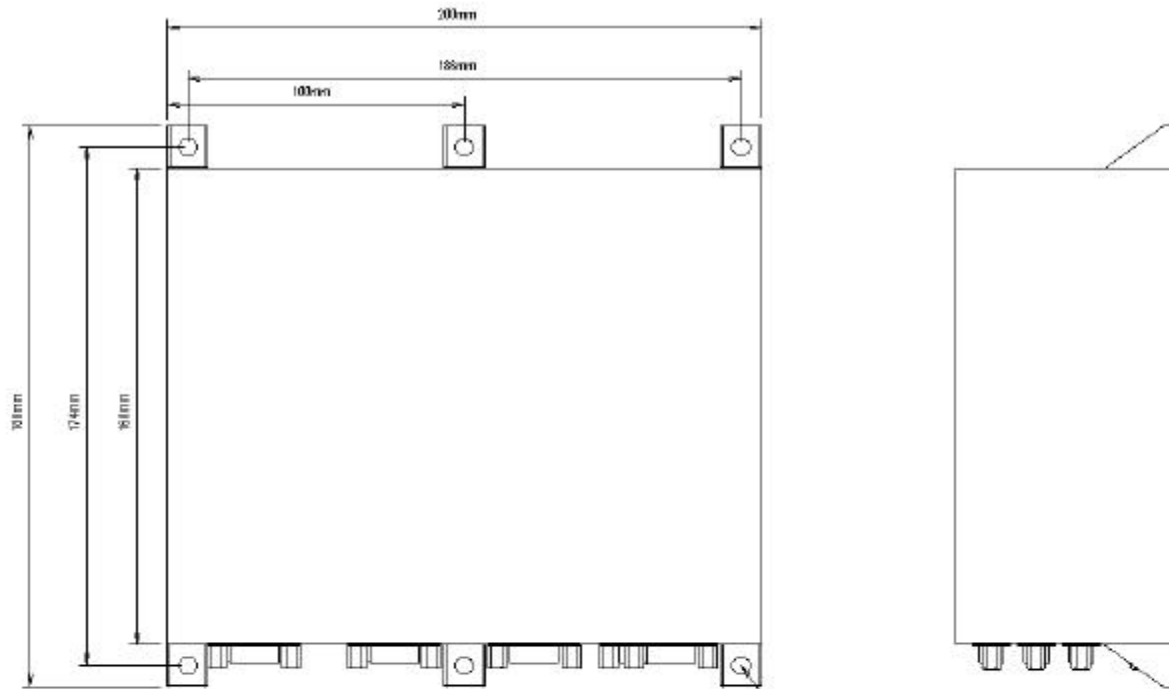
"Stackable Connector" Interconnect:
+/-12V, +/-5, +5V, +2.5V
MAG Serial Instrument Interface
MAG Heater Control
STE Serial Instrument Interface

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IDPU Block Diagram
D. Curtis Rev B 2001-7-17



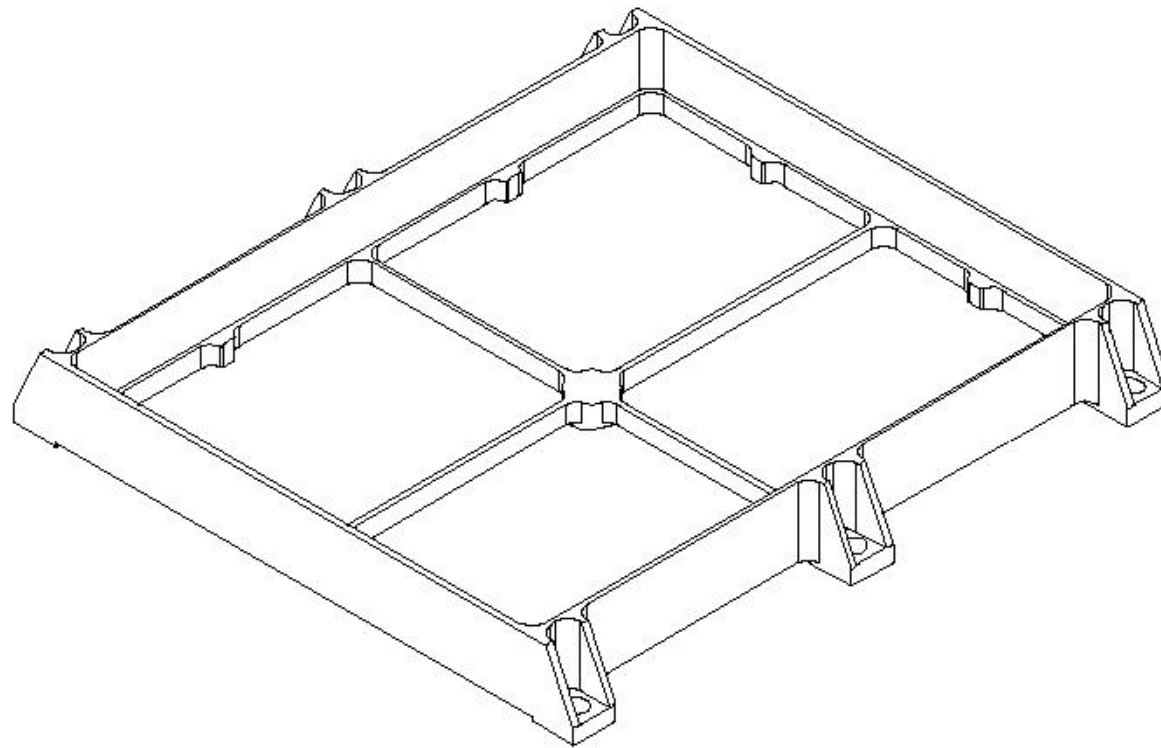
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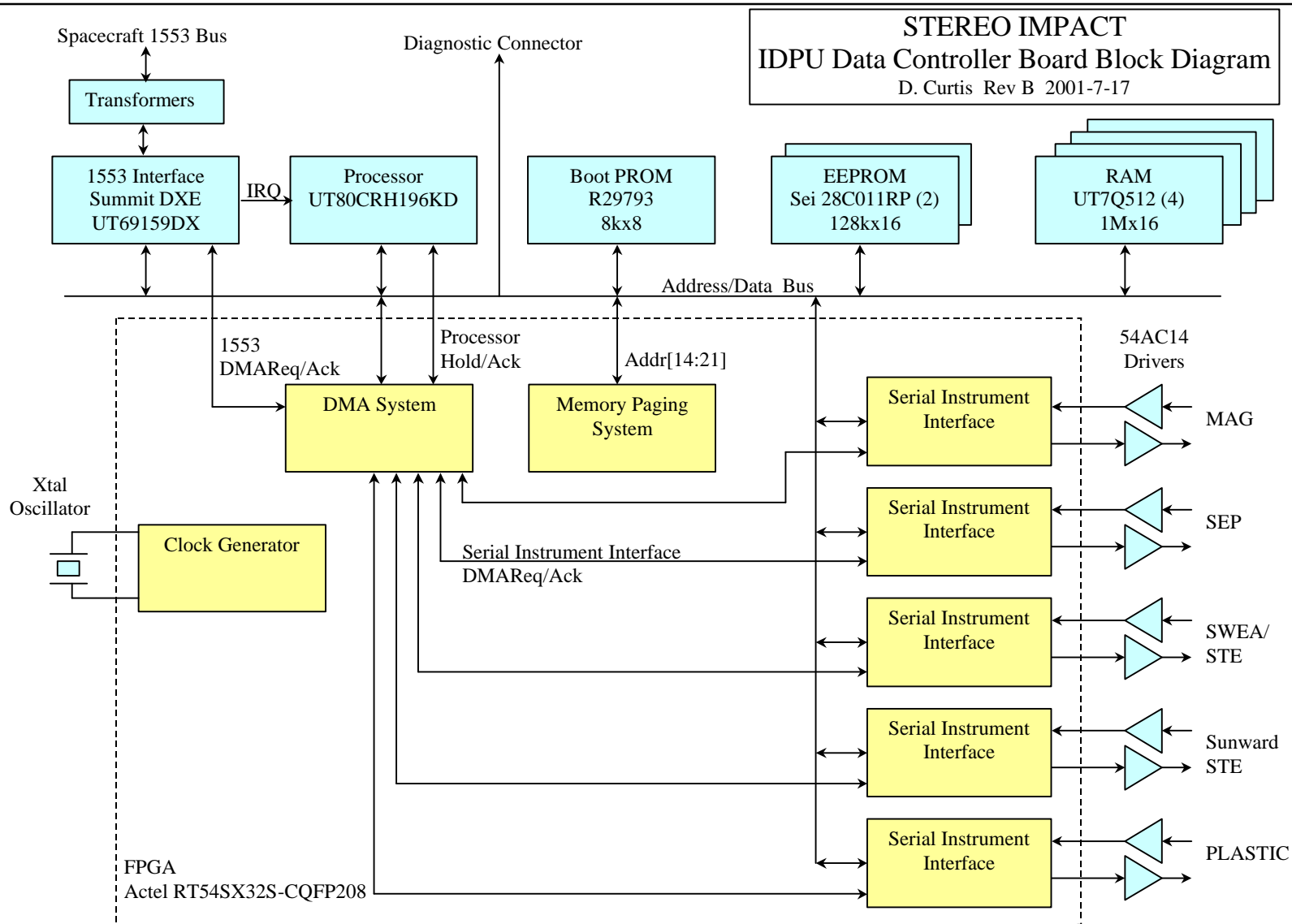
STEREO IMPACT IDPU
2001-7-17 ICD Drawing
Dave Curtis Rev A

IDPU Card Tray

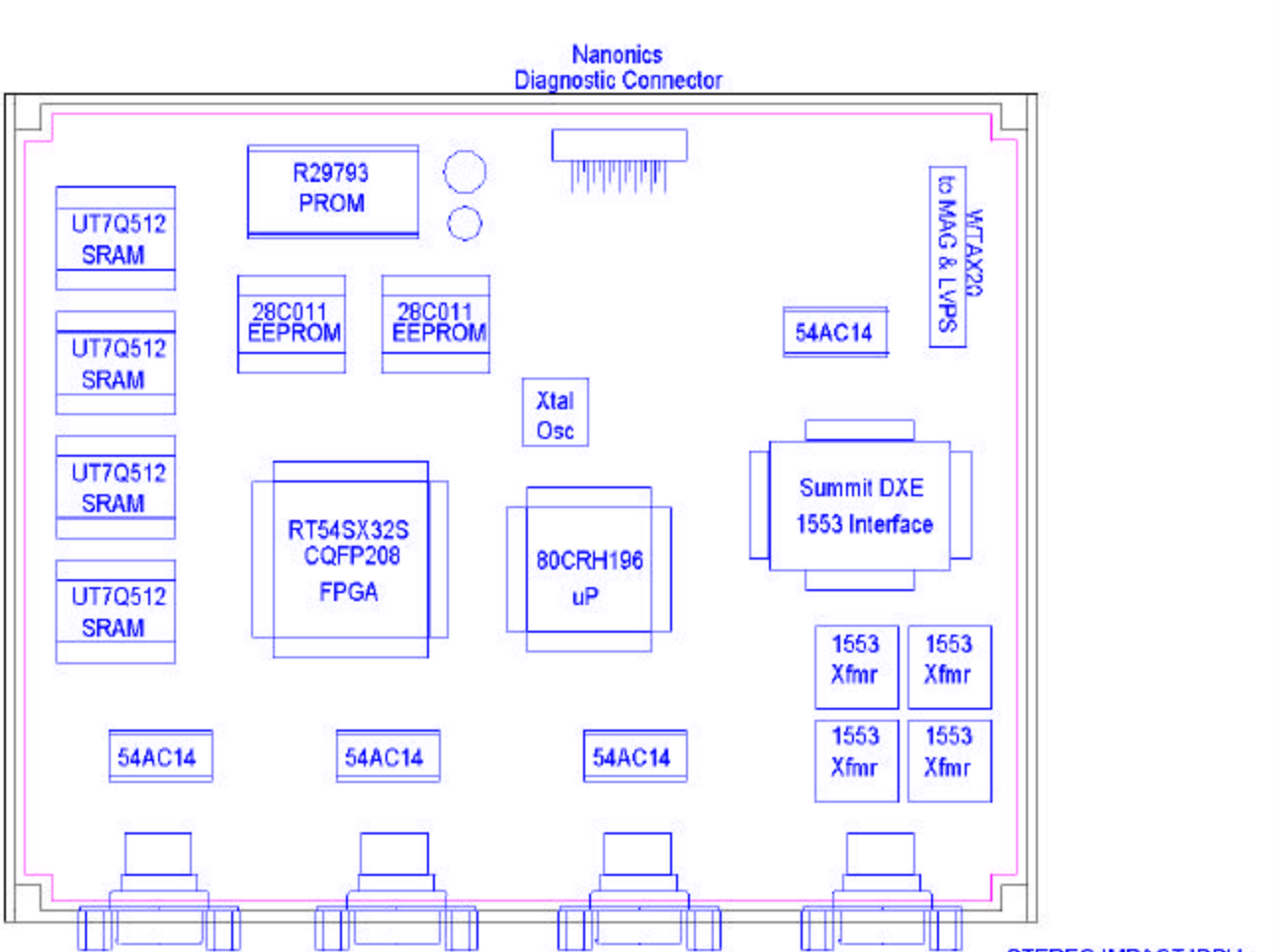


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Data Controller Board Layout



STEREO IMPACT IDPU
Processor Card
Dave Curtis 2001-5-3

Processor

- **UT80CRH196KD available high-rel, rad-hard from UTMC**
- **16-bit micro controller based on Intel design**
- **Can clock up to 20MHz; limited by low-power RAM access speed to 12MHz. Adequate throughput with generous margins (2x) at 8MHz.**
- **Low power processor with high speed ALU for computational tasks (SWEA and PLASTIC moment computations)**
- **64Kbyte addressing requires a paged memory system**
- **Low Power standby mode allows extra processor margin to be designed in without wasting power (put processor to sleep when not being used)**
- **Built in watchdog timer**
- **Built in serial interface for diagnostics**
- **Processor Bus Arbitration scheme for Direct Memory Access scheme to get data in and out quickly with little processor overhead**

Memory

- **Boot PROM contains startup code and ability to reload EEPROM and RAM from ground command**
 - 8 kbytes more than adequate
 - RAD Hard Bipolar PROM with power switch (off when not used)
- **EEPROM contains normal operational code and look-up tables**
 - 128Kx16 is huge over-kill; Estimate < 16kbytes of flight code.
 - Sei rad tolerant package, low SEU rate, no SEL
 - In-flight reprogrammable via Boot PROM
- **2Mbytes of static rad-hard RAM (UTMC 512K x 8), mostly for Burst memory plus some telemetry buffering**

1553 Interface

- **UTMC Summit part**
 - RAD Hard, High Rel, Highly Integrated
- **Connected to processor memory via DMA**
 - Control tables
 - Data buffers
 - Low processor overhead

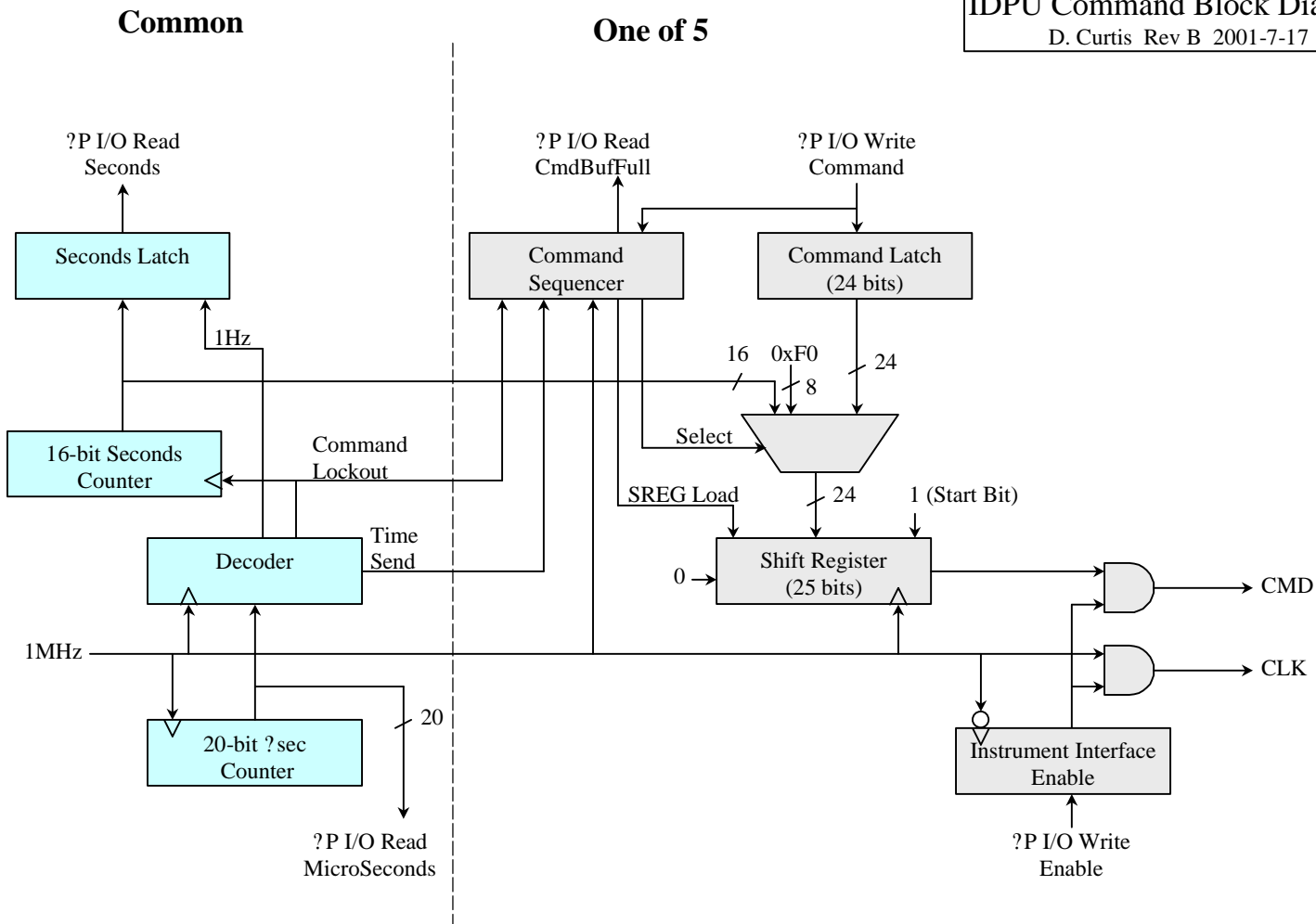
Data Controller Board FPGA

- **Processor Interface Logic implemented in an FPGA**
- **Actel RT54SX32S baselined**
 - **Common FPGA selected for IMPACT team**
 - **Rad tollerant (100krads)**
 - **High Rel available**
 - **2880 logic modules**
- **Actel specification to be developed by SSL (Curtis)**
- **Actel design to be developed/tested by Elf**
 - **Same arrangement & personnel used on HESSI**
- **Attention will be given to good Actel design practices**

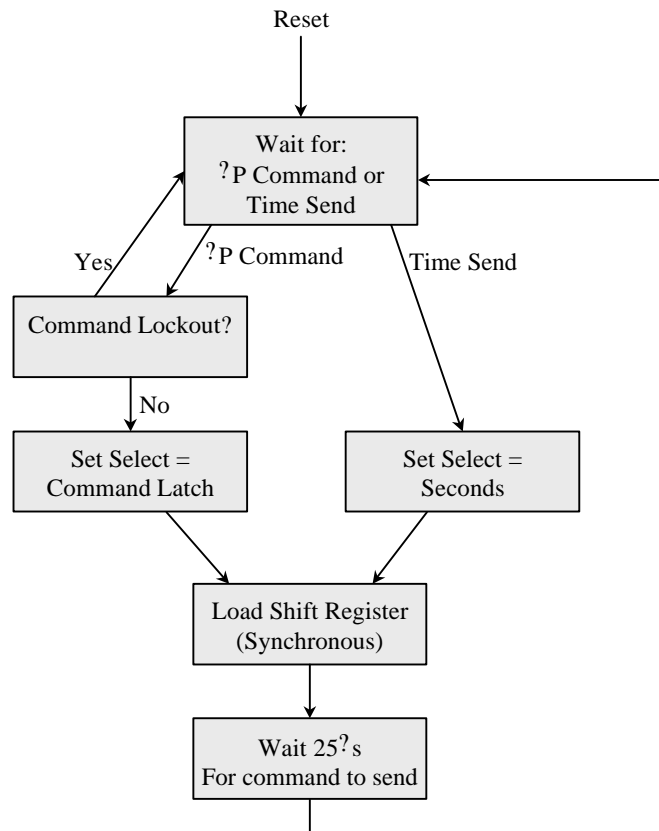
Processor Interface Logic

- **Instrument Serial Interface Implementation**
 - DMA telemetry into processor memory to off-load processor
- **Spacecraft interface glue logic (another DMA channel)**
- **Synchronous clock generation based on a 24MHz crystal**
 - 1553 interface (24MHz)
 - Processor clock (8MHz)
 - Serial interface clock (1MHz)
 - Sampling clock (divided down from 1MHz by instruments)
 - Processor Timing Interrupt (64Hz)
- **Memory Paging**
 - Processor 64kbyte addressing broken into four 16kbyte blocks
 - Each block can be paged into one of 128 RAM pages, or 16 EEPROM pages
 - Boot PROM comes in in boot page on reset

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Serial Instrument Interface
IDPU Command Block Diagram
D. Curtis Rev B 2001-7-17



STEREO IMPACT
Serial Instrument Interface
IDPU Command Sequencer
D. Curtis Rev A 2001-5-4

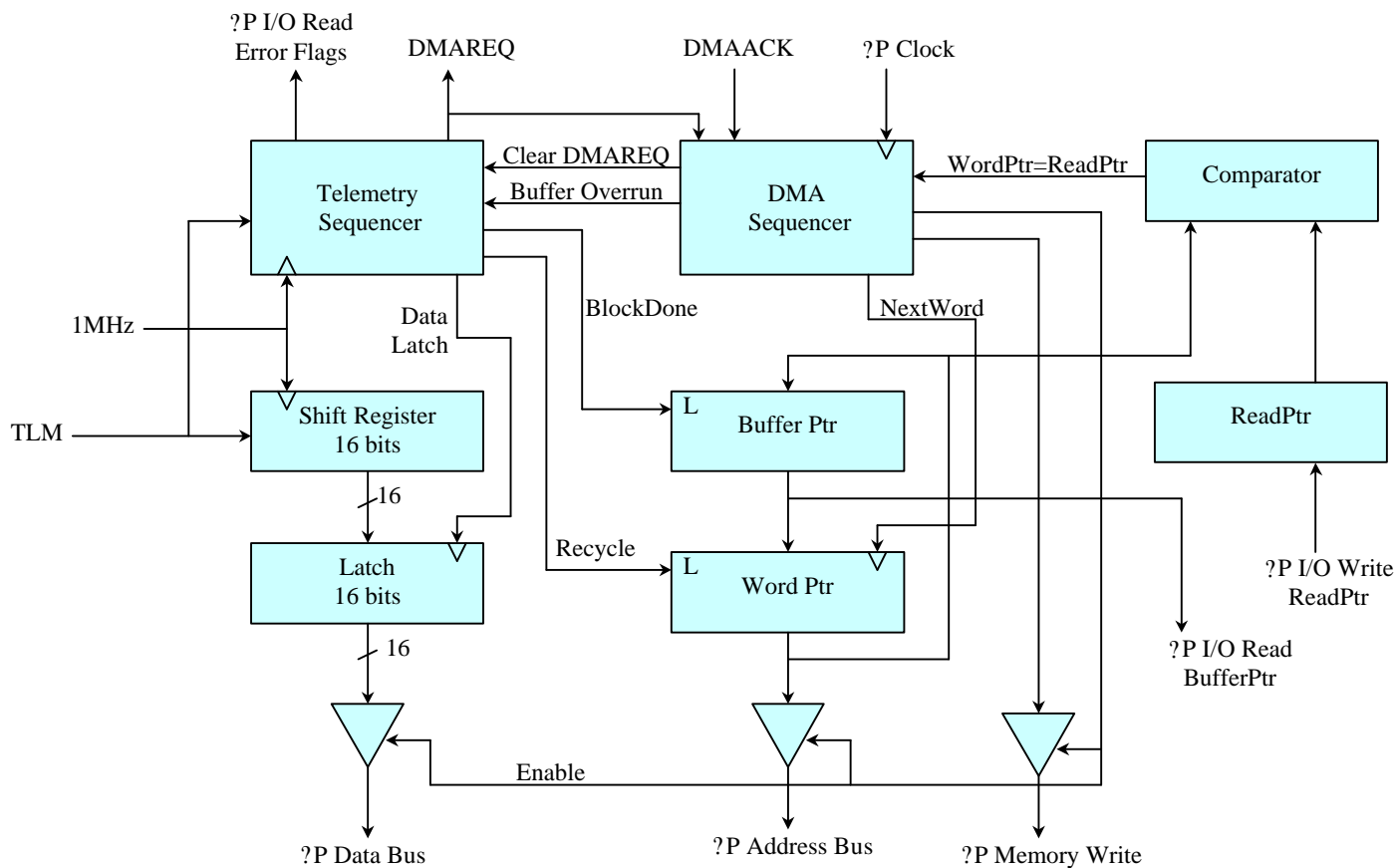


Timing:

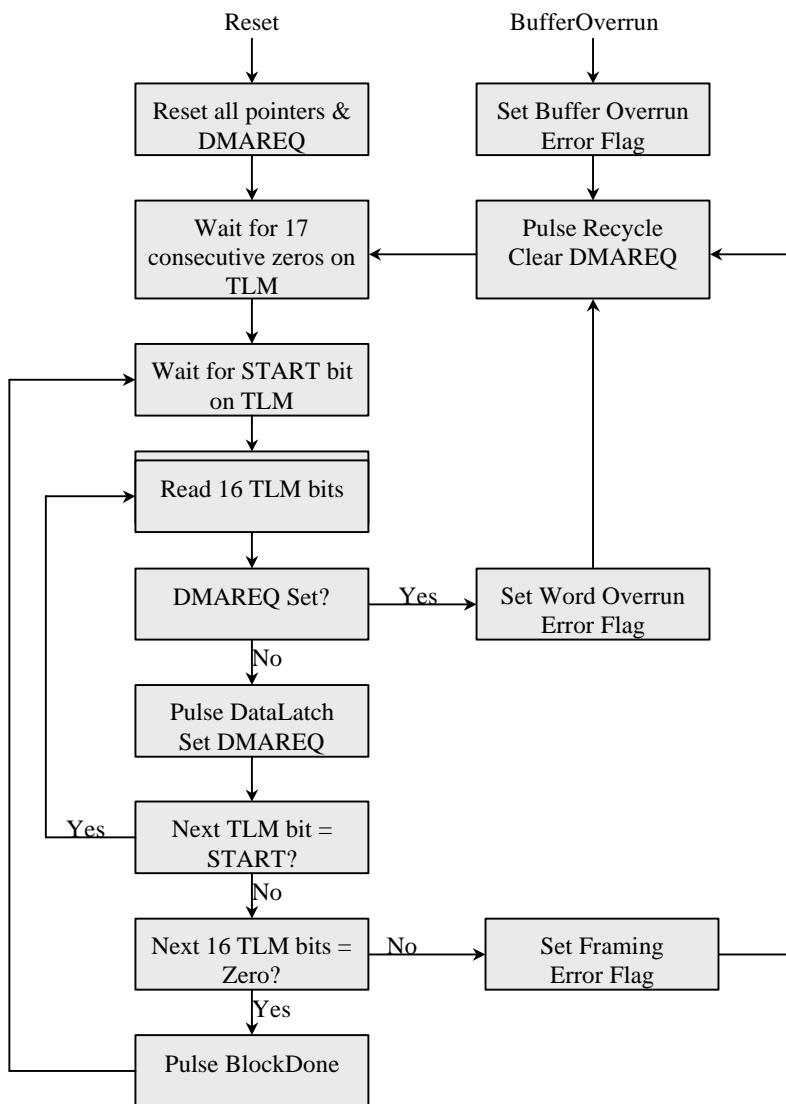
- ✘ Decoder generates 1Hz tic on rising edge of 1MHz clock when microsecond counter returns to zero
- ✘ Decoder Generates Command Lockout signal starting 50 microseconds before the 1Hz tic, and lasting until the 1Hz tic. This is used to lock out and processor generated commands in the interval when the time command must be sent
- ✘ Decoder Generates the Time Send signal 24 microseconds prior to the 1Hz tic. The state machine timing must be arranged to ensure that the rising edge of the 1MHz clock following the last time command data bit corresponds to the rising edge of the 1Hz tic (per the IMPACT Serial Interface Specification)

One of 5

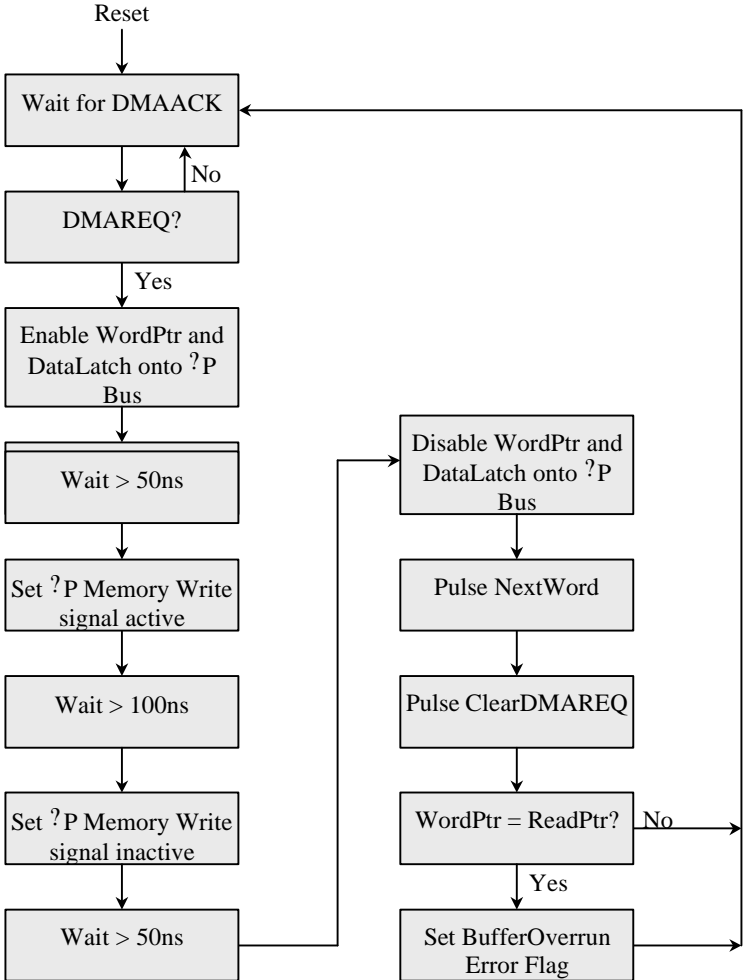
STEREO IMPACT
Serial Instrument Interface
IDPU Telemetry Block Diagram
D. Curtis Rev A 2001-7-17



STEREO IMPACT
Serial Instrument Interface
IDPU Telemetry Sequencer
D. Curtis Rev A 2001-5-7



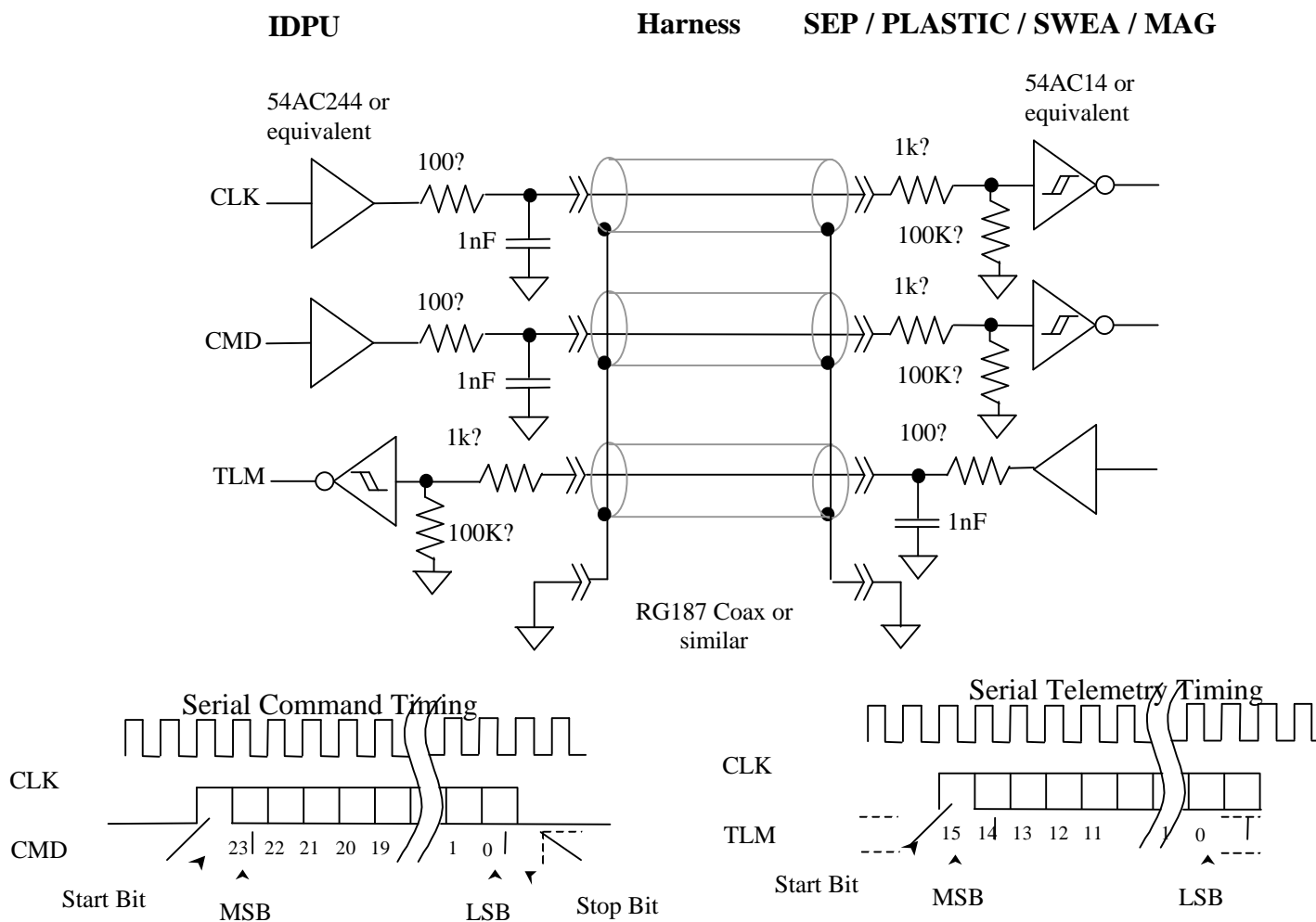
STEREO IMPACT
Serial Instrument Interface
IDPU DMA Sequencer
D. Curtis Rev A 2001-5-7



Serial Instrument Interface

- **Interface between IDPU and MAG, SWEA/STE, SEP, PLASTIC, and Sunward STE**
- **As defined by IMPACT Serial Interface document**
- **Three-wire serial digital single-ended interface**
 - **Continuous 1MHz Clock**
 - **Serial Data Out (Command)**
 - **Serial Data In (Telemetry)**
- **R-C rise time limiters to reduce EMC**
 - **OK by Manning (SWAVES)**
- **Coax or shielded wire harness**
 - **Breadboard shows good waveforms and timing with an 8m harness**
- **No handshaking; system designed to handle maximum throughput at both ends**
- **No gating; start/stop bit synchronization like RS232**
- **24 bit Commands in data out (8 bit ID, 16 bit data)**
- **Blocks of 16-bit Telemetry in**
 - **Blocks include an identifying header (5 bit ID, 10 bit block length)**
- **Synchronous 1-second time tic command**

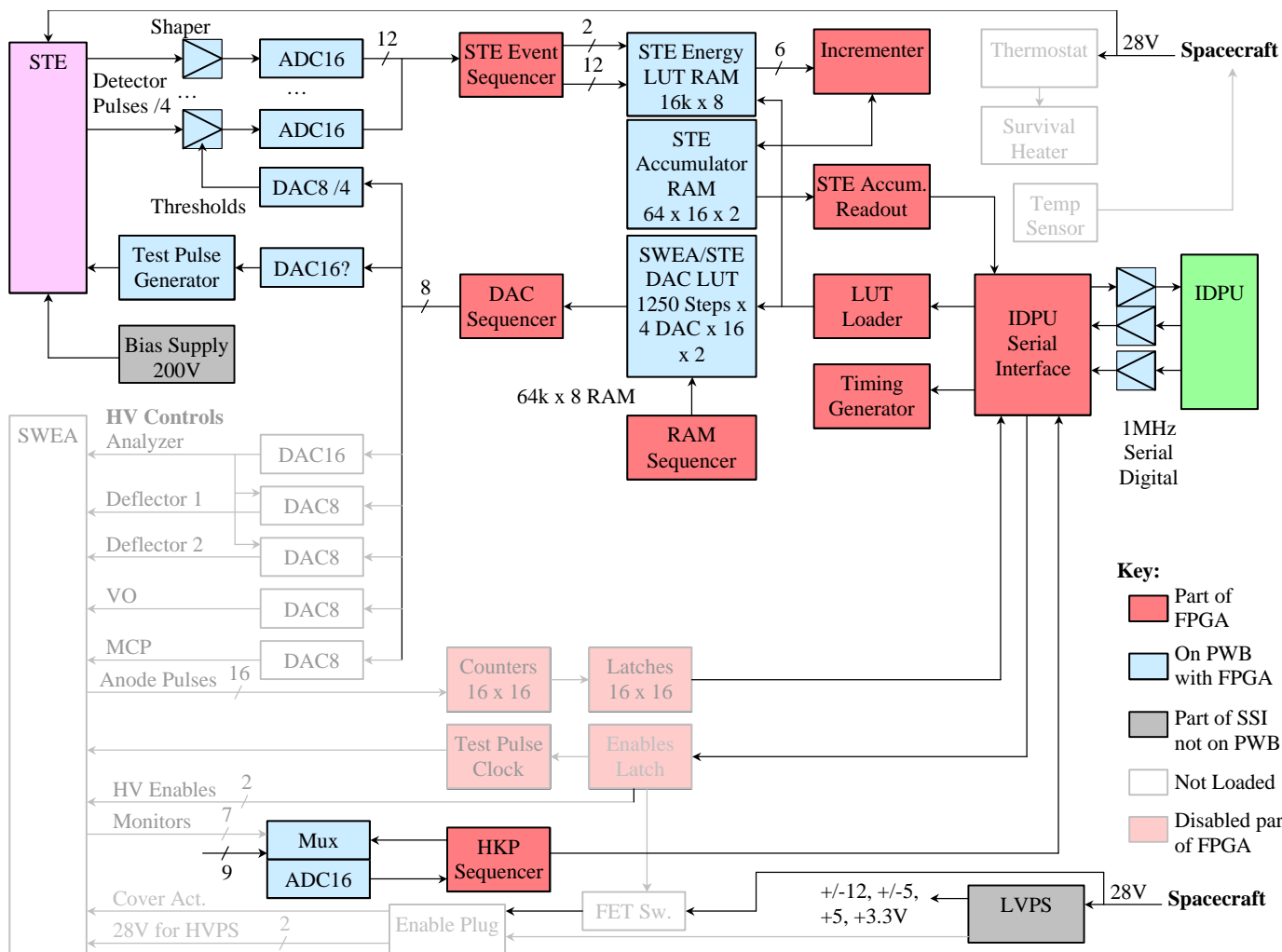
Serial Instrument Interface



Sunward STE Detector Interface

- **4 analog chains**
 - Charge Sensitive Amplifier inside STE
 - Shaper
 - Discriminator (programmable threshold)
 - ADC (200x dynamic range, 5% DNL -> 14-16 bit ADC)
- **Pulse height analyzer**
 - Programmable Energy binning to 16 log-spaced energy channels
 - 64-channel double-buffered accumulator (16E x 4 Det.)
 - 30KHz/detector throughput
- **Test pulse generator to test electronics**
 - Ramped-amplitude tail-pulse generator
 - Capacitively coupled into preamp inputs
 - When pulser active, only allow events near pulse times
- **Temperature housekeeping monitor**
- **Cover Actuator power switch**
- **Identical to SWEA/STE Interface (in SWEA), with SWEA circuits not loaded**

Sunward STE Detector Interface Board



IDPU Flight Software

IDPU Software Requirements

- **First draft of Software Requirements Document 6/01**
- **First draft of PLASTIC software requirements from UNH 6/01**
- **Top level requirements:**
 - **Support Spacecraft 1553 Interface per the Instrument ICD**
 - **Support Instrument Interfaces per the hardware and software specification**
 - **Collect, compress, and format telemetry data into CCSDS packets**
 - **Pass on mode-setting commands from the ground to instruments**
 - **Limited automation:**
 - **Set SWEA offset voltage to track spacecraft bias voltage**
 - **PLASTIC solar wind tracking and entrance system selection**
 - **MAG ranging**
 - **Instrument safing (response to HV anomaly, and spacecraft thruster/power down notifications)**
 - **Support a Burst memory system to collect high time resolution data for short intervals based on a burst trigger criteria**
 - **Share burst trigger data with SWAVES via RT to RT 1553 transfers**

IDPU Software Architecture

- **Use a simple custom polling loop operating system**
 - Tasks requiring fast turn-around are associated with the timer or other interrupt
 - Slower tasks run out of a polled loop in foreground
 - No preemptive scheduling or dynamic memory allocation required
 - Similar to schemes used on many previous instruments
- **Tasks are modular and as independent as possible**
 - Especially PLASTIC, to allow independent operation by UNH
- **Hardware designed to relieve software of most time-sensitive tasks**
 - Instrument sequencers allow instruments to cycle independently
 - DMA system collects data into IDPU memory automatically
- **Code will utilize software watchdogs on each task, together with a hardware watchdog, to monitor operation**
- **Software will regularly re-load all instrument registers to protect against SEU**
- **On reset the system will boot from the boot PROM, which will then verify the contents of the EEPROM, and transition to EEPROM code. A new EEPROM or RAM code image can be loaded by the boot PROM from ground commands**

MAG Software Requirements

- **Average MAG data to 4 samples/second, format into CCSDS packets**
- **Format 32 sample/second data into CCSDS packets for Burst memory**
- **Average MAG data to 1 minute and pass to Beacon telemetry formatter**
- **Perform ranging functions to select one of two gains based on previous measurements (only expected to be used on the ground)**

SEP Software Requirements

- **Pass on all SEP command packets (by ApID) and Spacecraft Time via Serial Instrument Interface**
- **Pass on all Telemetry Packets received via Serial Instrument Interface to Telemetry packet queue**
- **Pass SEP Housekeeping data received via the Serial Instrument Interface to Housekeeping packet formatter**
- **Pass SEP Beacon data received via the Serial Instrument Interface to Beacon packet formatter**

STE Software Requirements

- **Initialize and periodically reload STE Energy to Accumulator look-up table via Serial Instrument Interface from IDPU EEPROM**
- **Initialize and periodically reload STE threshold DAC values via Serial Instrument Interface from IDPU EEPROM**
- **Log-compress counters and format into CCSDS packets to pass to the Burst system**
- **Time Average and Log Compress counters and format into CCSDS packets for real-time telemetry**
- **Time and Space Average and Log Compress counters and pass to Beacon telemetry formatter**

SWEA Software Requirements

- **Initialize and periodically reload SWEA voltage waveform look-up table via Serial Instrument Interface from IDPU EEPROM**
- **Initialize and periodically reload SWEA control registers via Serial Instrument Interface from IDPU EEPROM**
- **Accumulate raw counter measurements into a three-dimensional distribution measurement**
- **Compute Moments, Pitch Angle Distributions and Full 3D distributions with desired time and space resolution and format into CCSDS packets for the Burst, Real Time, and Beacon telemetry streams**
- **Adjust SWEA bias voltage based on measured distribution function to offset spacecraft charging effects**

PLASTIC Software Requirements

- **Instrument Control Tasks:**
 - Decoding and routing instrument mode and table load commands
 - Controlling the energy at which apertures are switched based on measured count rates
 - Controlling “Solar Wind Tracking Mode” when Bursts are triggered to get high time resolution data
 - HV safing in response to an Arc
- **Data Tasks: Collect, compress, and format**
 - Housekeeping data
 - Monitor Rate data
 - Matrix data (from the classification board)
 - Proton and Alpha Moments
 - Reduced Proton and Alpha Distributions
 - Heavy Ion Distributions
 - Raw Event Data
 - Event Prioritization
 - Beacon Mode data

Software Development Plan

- **IDPU Flight Software to be developed at UCB by a single programmer**
- **Code to be developed in modular, structured assembly code**
- **Software to be developed and tested on the ETU IDPU, with ETU Instruments or simulators**
- **Software to be tested at the module level, then at the IDPU level in an acceptance test, and finally at the system level in interface and suite tests**
- **Software to be developed in builds of progressing complexity:**
 - **First Build to test processor hardware**
 - **Second build provides at least minimal functionality required to verify suite hardware (without automation and more complex telemetry products)**
 - **Third build should be for Flight**
- **Prior to installation in the flight hardware, code is maintained with minimal formality, using a log book which contains the development history, testing, problems, etc.**
- **Following installation in flight hardware, software is under the same control as the hardware (configuration control, problem reports, etc.)**

Software Development Tools

- **Use Commercial Phyton PC-based 80C196 development tools**
 - Assembler/Linker
 - Simulator (for early module testing)
- **ROM Emulator (for fast testing)**
- **Logic analyzer (for those subtle timing problems)**
- **ETU Data Controller Board**
 - Note that IDPU Simulator GSE is based on the same architecture as IDPU DCB (commercial 80C196KD with similar memory and FPGA); can be used for early software development and test
- **EGSE:**
 - **APL Spacecraft Emulator**
 - UCB-developed Command and Telemetry GSE
 - UCB-developed Science Display GSE (MAG,SWEA,STE)
 - SEP, PLASTIC Science Display GSE
 - UCB-developed Instrument Simulator
 - Instrument ETUs
 - UNH-provided PLASTIC simulator

Ground Support Equipment

IDPU Simulator GSE

- **Developed at UCB (with Elf)**
- **Provides ability to test instruments in the absence of the IDPU and verify the instrument/IDPU interface**
- **Consists of a black box (IDPU Simulator GSE, ISG) plus a PC**
- **ISG includes most of the functionality of the Data Controller Board, minus the 1553 interface**
 - **Includes a commercial 80C196 processor, FPGA with an early version of the flight DCB FPGA**
 - **Interfaces with PC via the printer port**
 - **Designed to IDPU Simulator Specification Document by Elf (who also designs the DCB)**
 - **Can be used as a test bed for IDPU software**
 - **Has an added Instrument Simulator feature which works the serial instrument interface in the reverse direction for IDPU testing**
- **PC software shall be developed at UCB**
 - **Based on LabWindows CVI development system**
 - **HESSI GSE heritage; STOL-like scripted command system**
 - **Science display modules written at the instrument home institution**

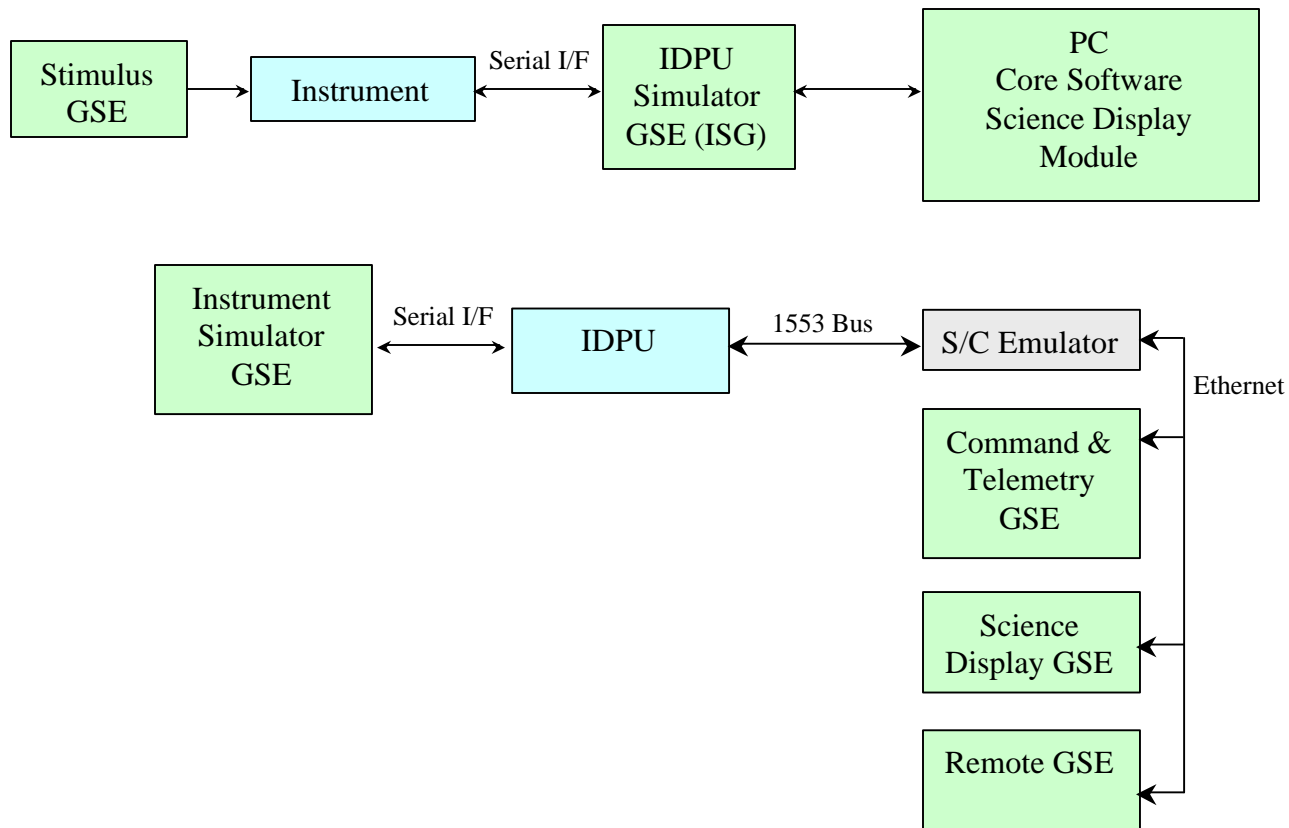
Command & Telemetry GSE

- **Works with Spacecraft Emulator at suite I&T level**
- **Works with MOC at Spacecraft I&T level**
- **Runs commands and command scripts**
 - **STOL-like language**
- **Remote commanding & display via secure internet connection**
- **Displays housekeeping and instrument status information with limit-checking / alarms**
- **PLASTIC command scripts may be run on the IMPACT C&T GSE, or on a separate C&T GSE running the same software**

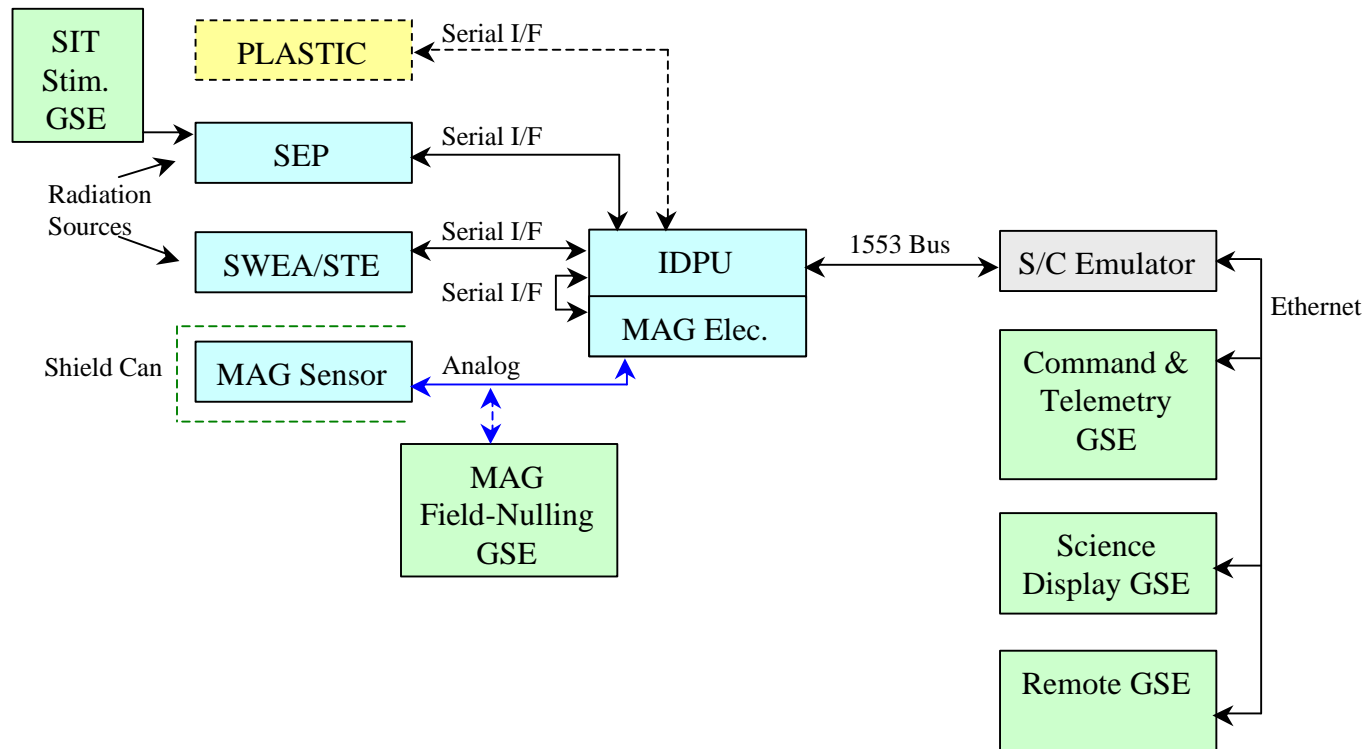
Science Display GSE

- **Decodes and Displays science data from instruments**
- **Provides adequate information to determine the health and functionality of the instrument in the I&T, Commissioning, and mission environment**
- **Runs on a second workstation (PC) in order to provide more display space, separate science and engineering functions, and improve the reliability of the C&T system**
- **Science Display GSEs will get data from the MOC or Spacecraft Emulator**
- **Science displays shall be developed by the instrument teams:**
 - **MAG, SWEA, STE – UCB / Hashii**
 - **SEP – Caltech**
 - **PLASTIC – UNH**

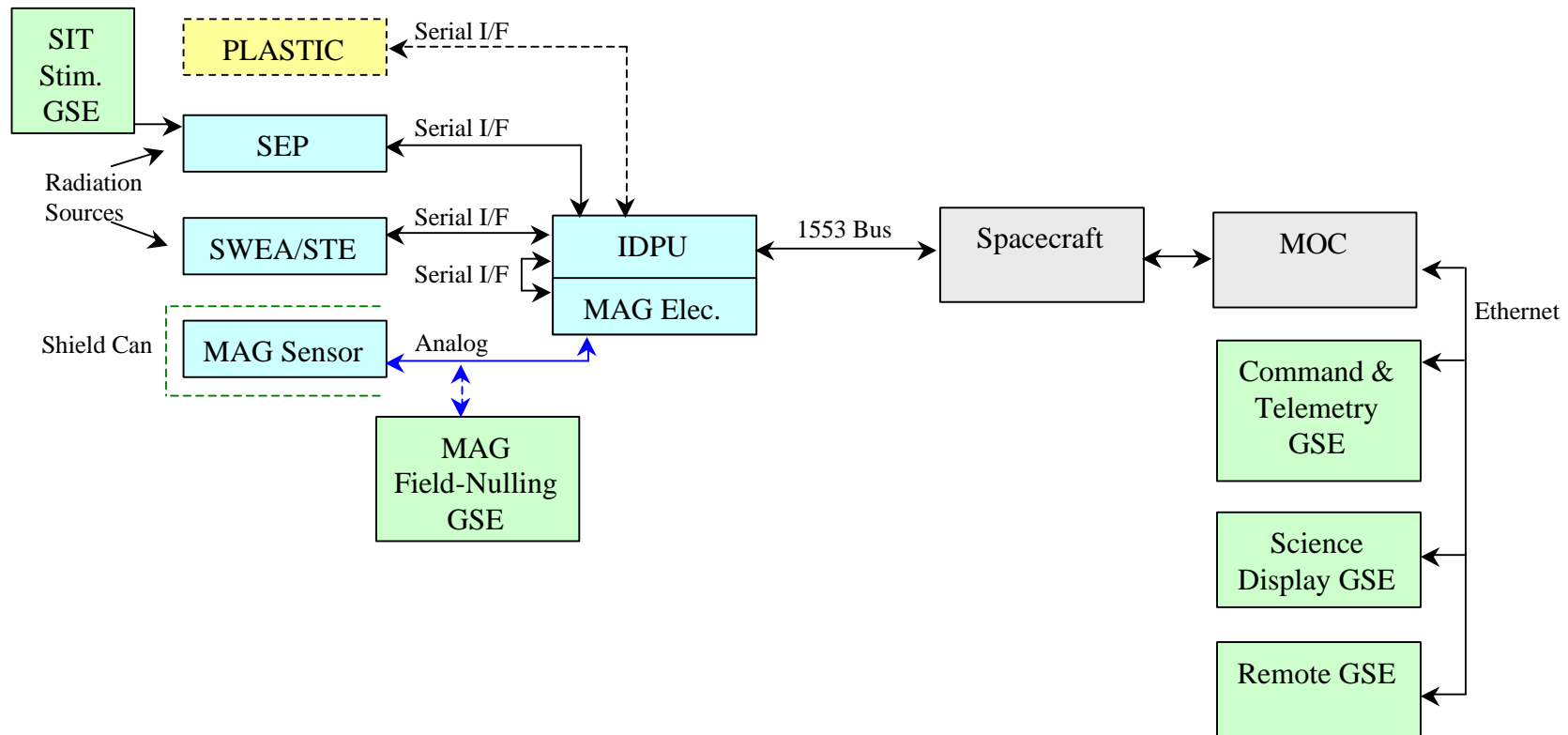
Instrument Bench Checkout Configuration



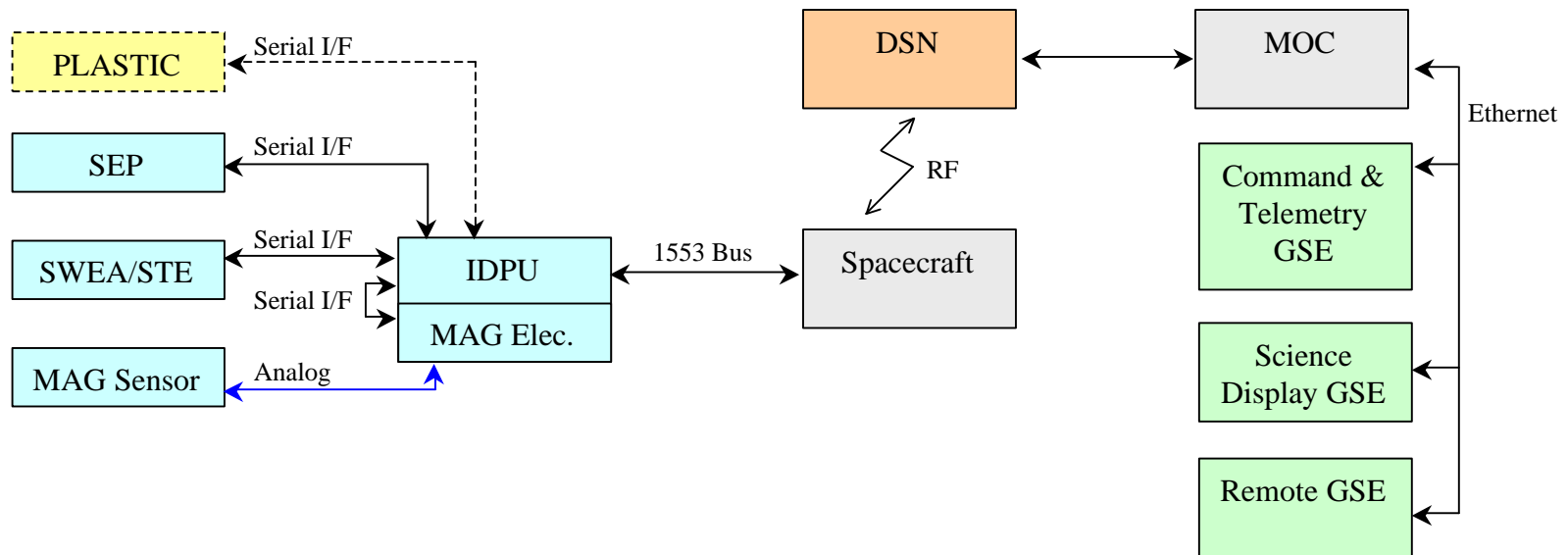
IMPACT Suite Integration GSE Configuration



IMPACT Spacecraft Integration GSE Configuration



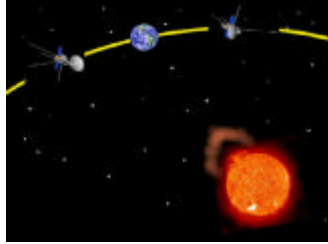
IMPACT Mission Operations GSE Configuration



GSE Software Development

- **The IMPACT IDPU Simulator, Command & Telemetry, and Science GSE are PC-based systems running LabWindows-CVI based software**
- **The software is based on a long series of GSE developed at Berkeley, most recently for Lunar Prospector and HESSI.**
- **The software is modularized so that much of the existing code will be usable**
- **The software already has most of the features required (user interface, command scripting, database-driven command encoding and telemetry decoding, TCP/IP data interface, data decommutation and limit-checking, some science displays)**
- **The programmer who developed the most recent version of the GSE (HESSI) is base-lined to develop the IMPACT version.**

Low Voltage Power Converters



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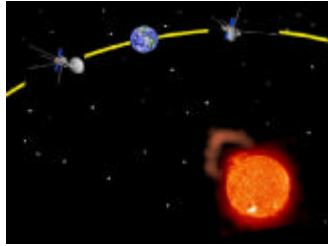


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LVPS OVERVIEW

- INPUT IS SPACECRAFT 28 VOLTS (22-35 VOLTS NOMINAL)
- COMPLIES WITH 7381-9030 GUIDELINES
- DEDICATED SUPPLIES PER SUBSYSTEM
- TOPOLOGIES CHOSEN TO PROMOTE EFFICIENCY
- ALL SUPPLIES SYNCHRONIZED TO CRYSTAL CONTROLLED 100KHZ MULTIPLES
- SUPPLIES ARE SOFT STARTED TO MINIMIZE TURN-ON STRESSES – INPUT CURRENT CONTROLLED
- TRANSFORMERS FARADAY SHIELDED TO REDUCE ELECTROSTATIC NOISE



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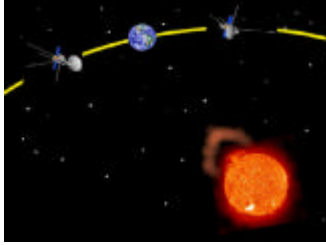


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LVPS OVERVIEW_{CONT}

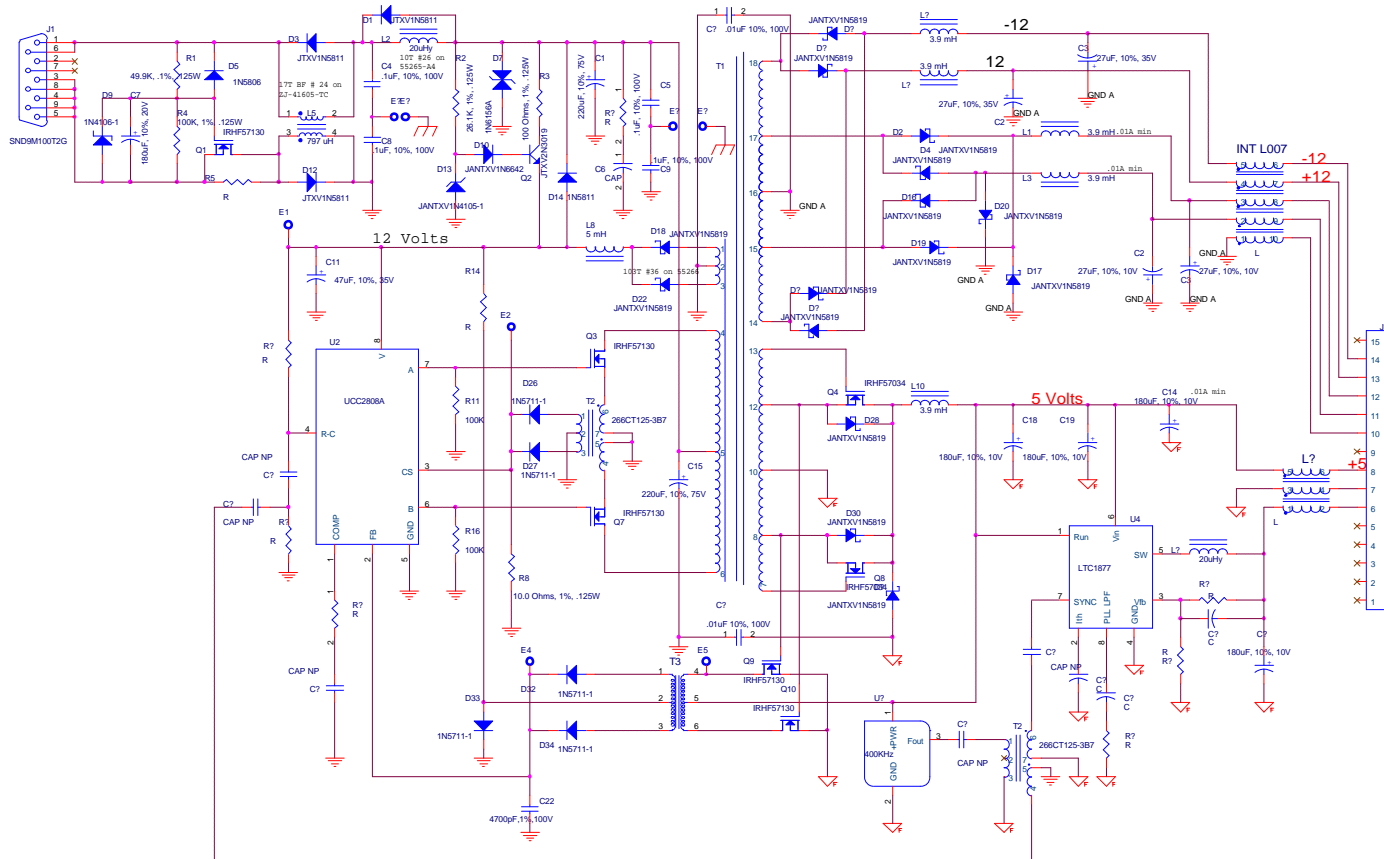
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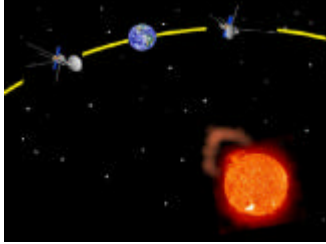
- INPUT TO SUPPLIES EMPLOYS BOTH COMMON MODE AND DIFFERENTIAL MODE FILTERS TO IMPROVE NOISE SUPPRESSION
- OUTPUTS EMPLOY COMMON MODE FILTERS TO IMPROVE NOISE SUPPRESSION
- INPUT IS SPACECRAFT 28 VOLTS (22-35 VOLTS NOMINAL)
- GENERATION 5 FETS USED FOR MAXIMUM EFFICIENCY
- USE SCREENED COTS INTEGRATED CIRCUITS



IDPU LVPS

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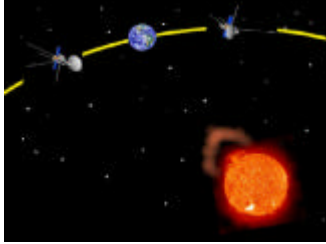


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SIT HVPS

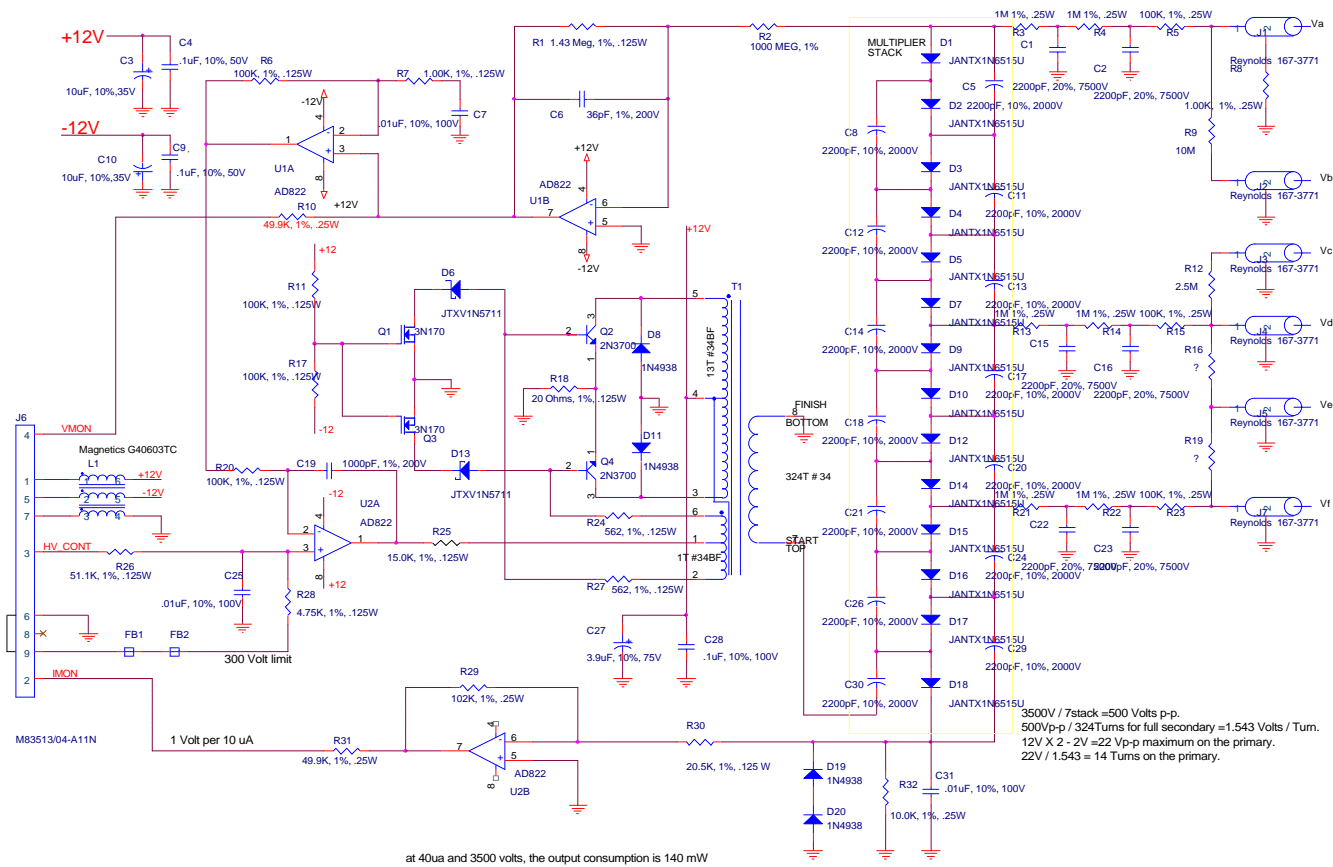
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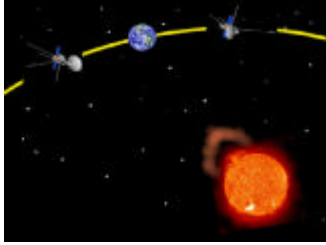
- SUPPLY IS SINE WAVE FOR LOWEST NOISE
- SIX OUTPUT TAPS, MAXIMUM VOLTAGE IS 3500 V
- RUNS AT ~ 65 KHZ
- INPUT IS ? 12 VOLTS FROM SEP SUPPLY
- OPERATES AT SEA LEVEL AND DEEP SPACE
- EFFICIENCY ~ 60 %



SIT HVPS

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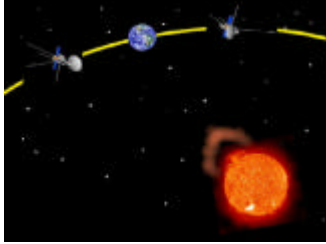


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IDPU LVPS VOLTAGES

- ? 12 Volts Analog
- ? 5 Volts Analog
- +5V Digital
- +2.5 Volts
- EFFICIENCY ~70%
- OUTPUT POWER = 3 WATTS



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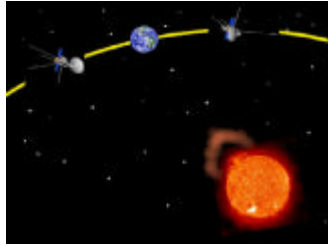


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STEREO
IMPACT

PLASTIC LVPS VOLTAGES

- ? 12 Volts Analog
- ? 5 Volts Analog / Digital
- +2.5 Volts
- EFFICIENCY ~ 75%
- OUTPUT POWER = 7.11 WATTS



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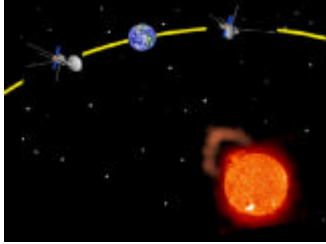


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SWEA LVPS VOLTAGES

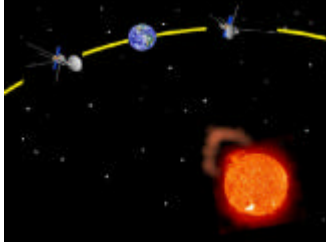
STEREO
IMPACT

- ? 12 Volts Analog
- ? 5 Volts Analog
- - 200 Volts Bias
- +5 Volts Digital
- +2.5 Volts
- EFFICIENCY ~60%
- OUTPUT POWER = 1.03 WATTS



SEP LVPS VOLTAGES

- ? 12 Volts Analog
- +5 Volts Analog
- +7.5 Volts Analog
- +3.3 Volts Digital
- +5 Volts Digital
- +2.5 Volts Digital
- -5.2 Volts Digital
- 3500V HVPS located in SIT
- EFFICIENCY ~ 60%
- **OUTPUT POWER = 3.6 WATTS**



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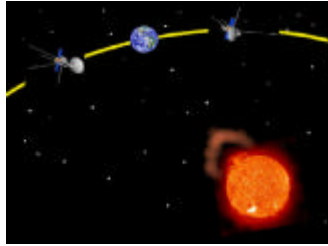


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PARTS CANDIDATES

STEREO
IMPACT

- TC25C25 - LOW QUIESCENT CURRENT VOLTAGE MODE PWM *DIP*
- UCC2808 - LOW QUISECENT CURRENT CURRENT MODE PWM *SM*
- ALD2302A - LOW QUISECENT CURRENT COMPARATOR *DIP*
- LTC1877 – HIGH EFFICIENCY STEP DOWN CONVERTER *SM*
- LM2672 - HIGH EFFICIENCY STEP DOWN CONVERTER *SM*
- STATEK LOW CONSUMPTION CRYSTAL OSCILLATORS



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COTS SCREENING

STEREO
IMPACT

- PARTS SCREENED FOR RADIATION HARDNESS TO 10K TD
- PARTS SCREENED TO 883 LEVELS GENERALLY
- PARTS SCREENED FOR RADIATION INDUCED LATCH UP