Plan

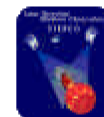
1-Technical issues (L.D.)

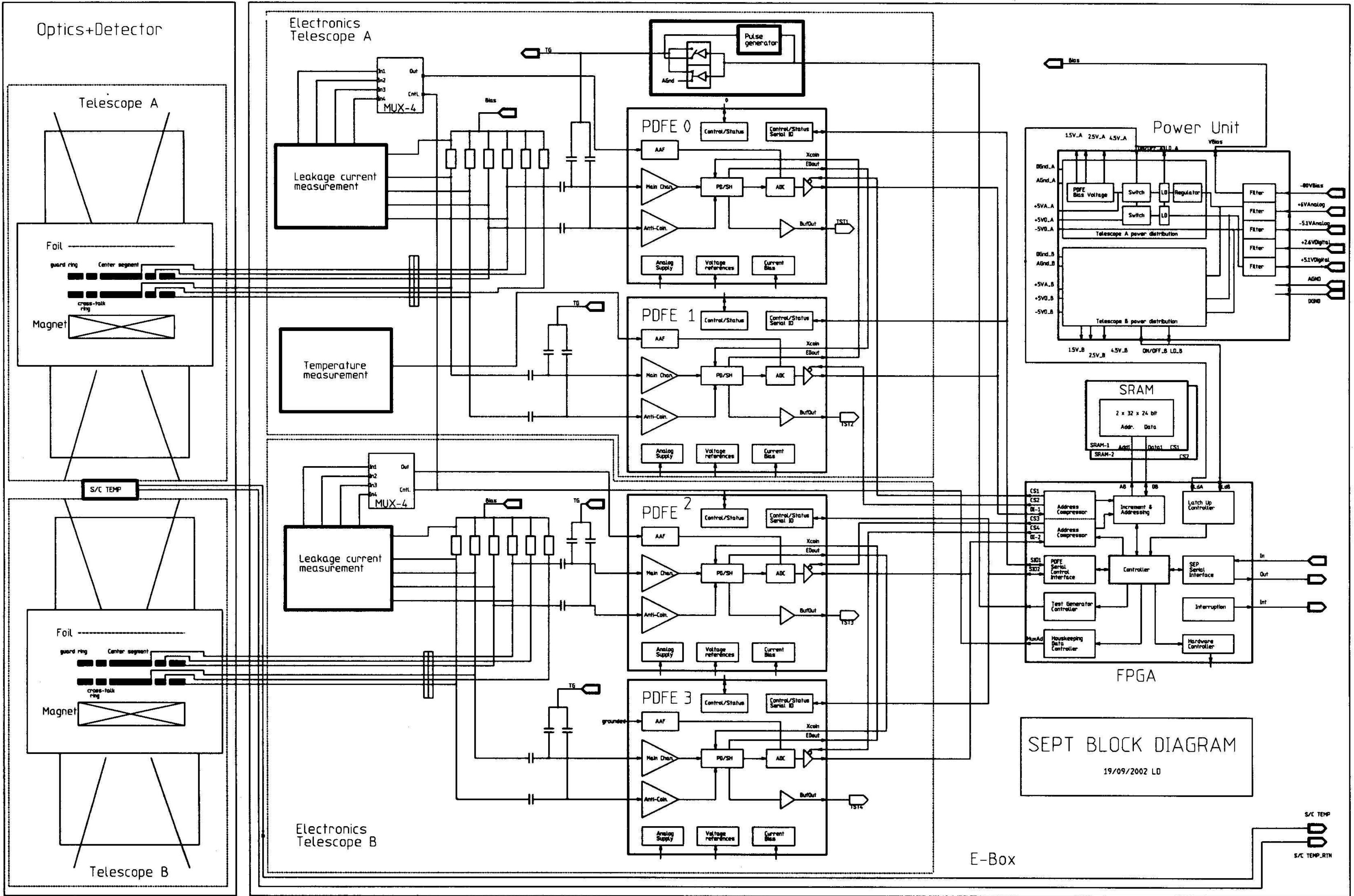
2- Schedule status (L. D.)

3- PAIP (B. J.)

4- CDR (L.D.)

List of attendants: D. Curtis (Berkeley), P. Turin (Berkeley), H. Culver (GSFC), M. Delont (GSFC)
M. Jones (GSFC), T. Sanderson (ESTEC), D. Martin (ESTEC), B. Johlander (ESTEC), L. Duvet (ESTEC)



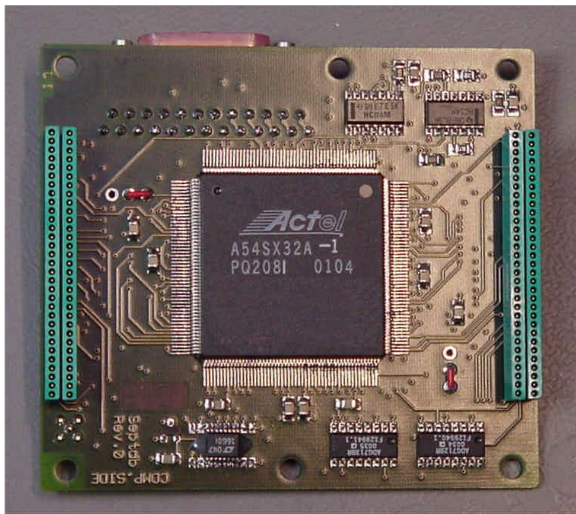


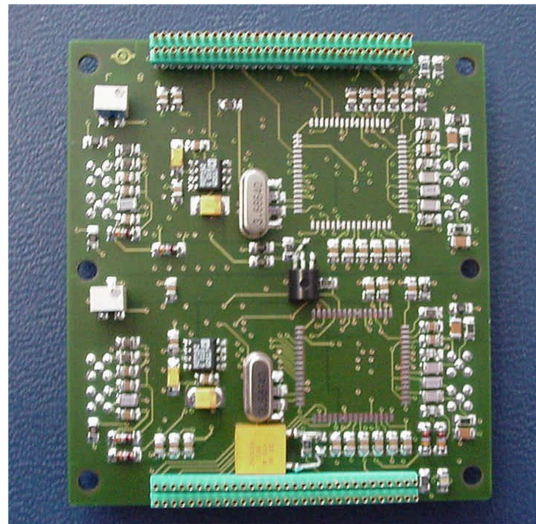
Optics+Detector
Telescope A
Foil
guard ring
Center segment
cross-talk ring
Magnet
S/C TEMP
Telescope B
Electronics Telescope A
MUX-4
Leakage current measurement
Temperature measurement
Pulse generator
PDFE 0
PDFE 1
PDFE 2
PDFE 3
Control/Status
Control/Status Serial IO
AAF
Main Chan.
Anti-Coin.
PD/SH
ADC
BufOut
Analog Supply
Voltage references
Current Bias
Electronics Telescope B
Power Unit
Telescope A power distribution
Telescope B power distribution
Filter
Switch
Regulator
SRAM
2 x 32 x 24 bit
FPGA
Address Compressor
Increment & Addressing
Latch Up Controller
PDFE Serial Control Interface
Controller
SEP Serial Interface
Test Generator Controller
Interruption
Housekeeping Data Controller
Hardware Controller
SEPT BLOCK DIAGRAM
19/09/2002 LD
E-Box

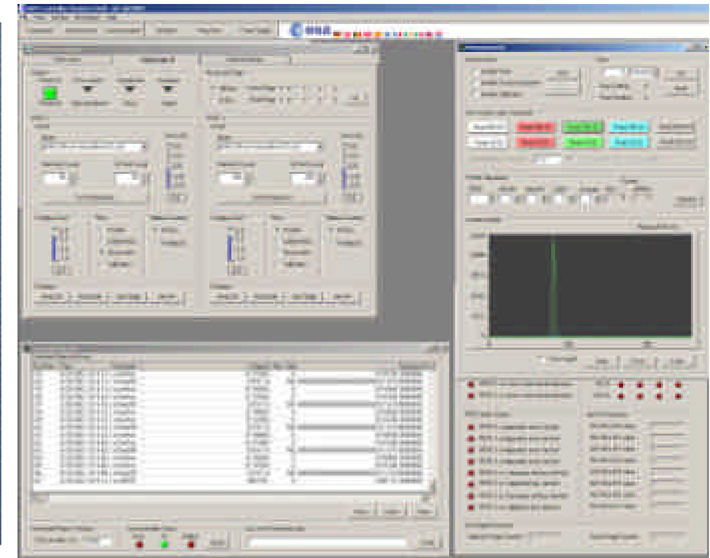
1- Technical issues

1.1 Breadboard tests

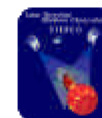
Analog and digital breadboards have been debugged (external contract, KTH)
Fully operational with GSE (interfaced with 1st release of the FPGA) at ESTEC since June 2002







Functional and performance tests have been performed to validate the design.



1- Technical issues

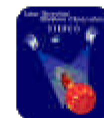
Functional tests

-FPGA control & interfacing
-PDFE operational modes and event filtering (together with FPGA)
-Power supply switching
-…

Performance tests

-Consumption: updated power break down
-Noise level: typically σ~1100 erms (=0.5 LSB, or 9.4 keV FWHM)
For 1 PDFE running alone on the breadboard, noise increase with other PDFE active (randomly stimulated)

- Tests are still being performed to identify potential noise sources.

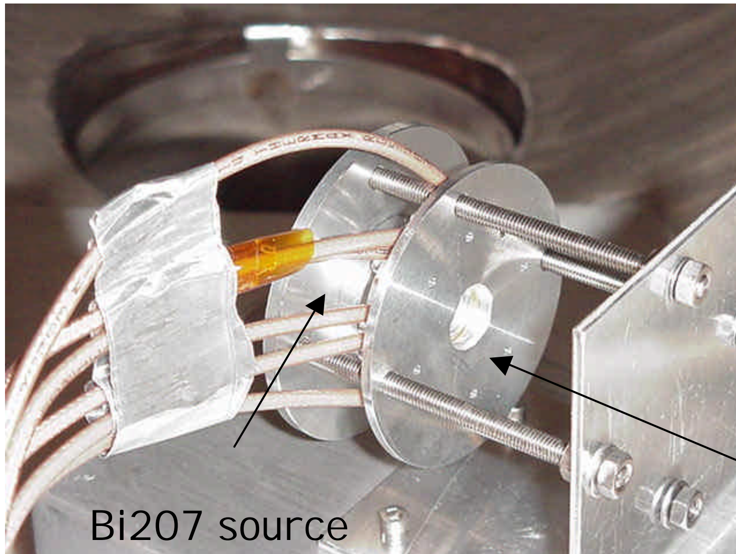


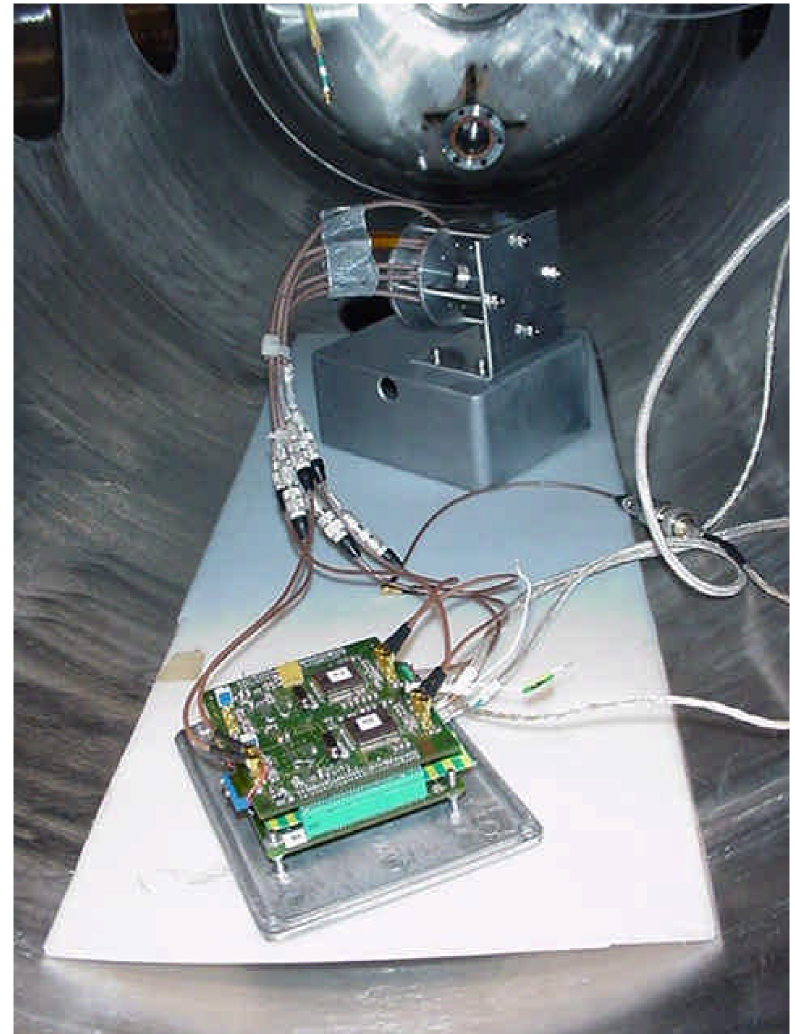
1- Technical issues

1.2 Integration tests

Integration tests carried out at ESTEC
(26th – 29th August)
Electronics (Breadboard)
+ prototypr detector (Kiel)

First integration





Stack of two detectors (1 telescope)

1- Technical issues

1.2 Integration tests

PIPS prototype 45102, Detector 2, 50V, Bi-207

AU K 56.7
K 481.7
L 553.8
M 565.8
K 975.7
L 1047.8
M 1059.8
SP2
GR2
SP1R
CRT2
[counts/sec]
[keV]

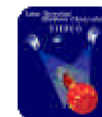
counts
bin

(1 hour accumulation)

(1 bin =8 keV)

Detector noise alone FWHM ~ 7 keV
With lab. Electron. FWHM ~ 7 keV
With Breadboard FWHM ~ 20 keV
Electronic noise FWHM ~ 18.7 keV

esa



1- Technical issues

1.2 Integration tests

At this stage:

- Fully operational instrument

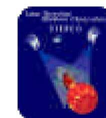
➢ No major changes for the EM model (Test pulse generator, Supply switching/regulation/filtering, HK)

-Noise level is not optimum yet. Progress are possible since:

- 3.8 times noise level of one PDFE alone on dedicated test board, the noise is likely to be external to PDFE..
- the breadboard layout was not optimized for noise reduction (4 layers). Great care will be taken for the next layout (EM).
- No input filtering on the breadboard

➢Additional tests (pulser/detector) are foreseen to fully characterize the influence of the different parts and signals on these high density boards (EM may not be yet the optimum).

Goal FWHM ~12 keV (~10 keV electronic noise)



1- Technical issues

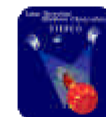
1.3 Others

Closed issues

-Grounding scheme agreed with Kiel
-Connectors/cable identified (SSMC bulkhead, MMCX PCBconnector)
-Connector pinout J2 (MDM 31) agreed with B. K. (redundancy on all signals)
-Temperature (op. heater) will be provided through the HK flow (1s resolution), TEMP S/C (non op heater) signal directly routed to detector housing.
-Serial link communication parameters (No H/S, baud rate)

Open issues:

-Power line specifications has to be updated (-5.1VA, +5.6VA, 5.3 VD, 2.6VD)
- noise level?
- -5.1VA may not be used.



2. Schedule Status

2. 1 EM progress

Delivery to Kiel 2nd week of January.

Design

- Design closed last week: schematics updated. New layout should be ready within 3 weeks.
- New block diagram issued
- Mass and power breakdown updated (power not released yet)
- Power lines specifications updated (not released yet)

FPGA

- Second version of FPGA (18 MHz clock, single counter) is currently being tested by KTH.

- FPGA EM design agreed (minor changes wrt to last release)

PDFE

-PDFE new contract is currently being prepared. Delivery scheduled for end of March 2003. EM will use present version (fully compatible)

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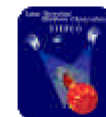

2. Schedule Status

2. 2 Part procurements

80 % (FPGA FM received, SRAM not yet)
Still quotations to be made (connectors...)

2. 3 Radiation testing

- Design has been optimized to lower the number of parts to be tested.

-Final selection made/procurement ~60% of selected parts

-Test PCB/adaptors not received yet

- Co 60 tests facilities booked for second week of october (delay wrt schedule)

- The aim is to have Californium tests (at least) done for CDR (so before 20 October). Additional heavy ions tests schedule still TBC.

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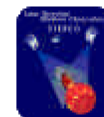
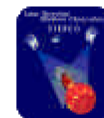


4. CDR

4.1 Deliverable Documents for CDR:

- Critical Design review package
- Final Product Assurance implementation Plan
- Final Failure Modes and Effects Analysis
- Final Environment test Plan
- Final Requirements Validation Plan
- Final physical block diagram
- Final grounding diagram
- Final parts identification list
- Final Hazardous Material list
- Final Material and processes list
- Final Instrument Flight/ground software development and management plan
- preliminary experiment users Manual



4. CDR

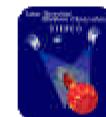
4.2 Delivered

- PA plan version 2 released end of July
- Part/Material lists released 1 week ago
- SEPT operation control and data processing requirements: released on 23/09/02 to A. Davis

4.3Soon to be delivered

-Level 1 data format will be delivered next week.
-Others?

CDR preparation meeting 25th, 26th september in Kiel



SEPT Electronics: Parts

90 % delivered

Developer Selected Part	Flight Part Number	Description	MFR
RT54SX32A-PQ208	RT54SX32S-CQ208B	FPGA, 208CQFP	Actel
HX6256/NQRC	5962R9584501QXC	SRAM, 32Kx8, 25ns, 28-Flat pack	Honeywell
54AC14	5962-8760901DA	FP-14, Schmitt trigger	National
54AC04	5962-8762401DA	FP-14, Hex inverter	National
CR60A HC49/U	TBD	Crystal, 18 MHz, HC49/U package	Croven/Crystek
MAX892	MAX892LEUA	Current limited switch	Maxim
AD590	AD590MF/883B	Temperature transducer	Analog Devices
1N6642	JANTXV1N6642-1	Diode, Switching, MIL-PRF-19500/578	Microsemi
100nF 0805	C0805C104K5RAC		KEMET
22pF 0805	CDR31BP220BJWS		KEMET
1nF 0805	CDR31BX102BKWS		KEMET
1uF	CWR11JH105KD		KEMET
10uF	CWR11HH106KD	Tantalum chip, 15 V, 10 uF, surge current tested	KEMET
33 uH	MS75085-1	Inductor, leaded, IM-2 size, 130 mA, 33 uH	VISHAY
22k	M55342K06B22E0R	22k, size 0705	SOTA
100R	M55342K06B100DR	100R, size 0705	SOTA
100k	M55342K06B100ER	100k, size 0705	SOTA
1M	M55342K06B1F00R	1M, size 0705	SOTA
MTB	ESA/SCC 340103101C31PFR116	Connector, Microminiature Strip, 0.050 centers, 31P	ITT-Cannon
MDM31S	M83513/04-E11N	Connector, Micro-D, Receptacle, Electroless Nickel, 31 Socket, pigtail	Glenair

PDFE ASIC	TBD	Particle Detector Front End ASIC	Alcatel
ADP3300	ADP3300ART-5	Voltage Regulator, 5V	Analog Devices
MAX892	MAX892LEUA	Current limited switch	Maxim
LMC6062	LMC6062AIM	Dual Op-Amp, Single Supply	National
ADG704	ADG704BRM	Multiplexer, 4-1 channels, SOIC-10	Analog Devices
CR60A HC49/U		Crystal, 4MHz	Croven/Crystek
1N5291	JANTXV1N5291	Diode, Current Limited, 0.5 mA	CDI
1pF	CDR31BP1R0BBWS	Ceramic capacitor, MIL-PRF-55681	KEMET
15pF	CDR31BP150BJWS		KEMET
1nF	CDR31BX102BKWS		KEMET
2n2	CDR31BX222BKWS		KEMET
3n3, 200V	C0805C332K2RAC	Capacitor, High Voltage SMD	KEMET
100nF	C0805C104K5RAC		KEMET
1nF, 200V	C0805C102K2RAC	Capacitor, High Voltage SMD	KEMET
0.47uF	CWR11KH474KD	Tantalum chip, 0.47 uF	KEMET
1uF	CWR11JH105KD	Tantalum chip, 1 uF	KEMET
100	M55342K06B100DR	100, size 0705	SOTA
2k0	M55342K06B2E00R	2k0, size 0705	SOTA
10k	M55342K06B10E0R	10k, size 0705	SOTA
22k	M55342K06B22E0R	22k, size 0705	SOTA

24k9	M55342K06B24E9R	24K9, size 0705	SOTA
69k8	M55342K06B69E8R	69K8, size 0705	SOTA
100k	M55342K06B100ER	100K, size 0705	SOTA
105k	M55342K06B105ER	105k, size 0705	SOTA
121k	M55342K06B121ER	121K, size 0705	SOTA
330k	M55342K06B330ER	330k, size 0705	SOTA
1M	M55342K06B1F00R	1M, size 0705	SOTA
5M11	CHP0705K5114GBE	5.11M, size 0705	VISHAY/Sfernice
10M	CHP0705K1005GBE	10M, size 0705	VISHAY/Sfernice
190M	HV1206CF1906J100S2	Resistor, 190 M, 1500 V, size 1206	Vishay
SSMC	7003-1572-002	SSMC straight bulkhead mounted cable jack	Applied Engineering products
MMCX plug	16 MMCX-50-1-1	MMCX right angle plug	Suhner
MMCX PCB jack	82 MMCX-50-0-1	MMCX straight PCB jack	Suhner
coax cable	RG178	RG178 coaxial cable	Axon
MTB	ESA/SCC 340103101C31SFR116	Connector, Microminiature Strip, 0.050 centers, 31S	ITT-Cannon
M 17/93 RG 178	MIL-C-17/93 RG 178	Coaxial cable	Axon Germany
7105-1521-002	MIL-PRF-39012	SSMC connector	AEP Connector
DE9P-OL2-K87	MIL-PRF-24308	D Subminiature	Cannon ITT Industries
P5-403-10S		Pinpuller	Tini AEROSPACE, Inc.
S 17624 PDYT1A		Thermistor	Minco Products, Inc.
Klixon 4-BT-2	MIL-S-24236/13	Thermostat	Texas Insruments
MDM9S		Connector, Micro-D, Receptacle, 9 socket, pigtail	Glenair
TBD	TBD	Heater (operational, survival)	TBD

PDFE Manufacturing and screening

- WP 1: Design update: oscillator cell
- WP 2: Manufacturing: two wafers, 800 dies, current rev. and updated mixed
- WP 3: Test S/W and H/W development (in parallel with WP 2)
- WP 4: Packaging and screening
- WP 5: LAT

Rad testing

- TID and SEL test PDFE, mux, switch, regulator and OP amp

Potential problem parts:

- PDFE (single source)
- MUX (multi source)
- Switch (multi source)
- Current limiter (single source?)
- OP-amp (multi source)
- +5V Regulator (multi source)
- Crystal (multi source)
- SMD HV resistor
- Ceramic caps ??

PDFE Flight lot screening

100% production test
Internal visual (MIL-STD-2010, condition A), including bond strength & die shear
Serialise
Electrical test (min, max, RT, read and record)
Select (based on distributions)
Temperature cycling (MIL-STD-1010, condition C)
Electrical test (min, max, RT, read and record)
PIND (MIL-STD-2020)
Burn-in (MIL-STD-1015, condition D)
Final electrical measurement (min, max, RT, read and record, delta calculation)
Hermetic seal (MIL-STD-1014, condition A)
External visual (MIL-STD-2009)
Solderability (3 samples from rejects)

LAT
DPA (3 pcs) including bond strength and die sheer
Life test, 1000 h, 10 pcs, Electrical test at 0, 500 and 100 hours

Parameters for electrical test:

Digital part
1. functional test (TBD fault coverage)
2. VO, VI, IDD, IOZ, IIL (digital part)
3. TP (?), TR (digital part)

Charge amp
1. TR
2. noise?
3. VOS
4. TP ED-OUT
5. S/H out: linearity
6. shape bias vs S/H out
7. rmbias vs S/H out

Analog input amp
1. VOS
2. A
3. IIO
4. linearity
5. PSRR

ADC
1. VOS
2. linearity (differential, integral)

LOW VOLTAGE EFFECTS

Customers sometimes question the possible effects of low voltage operation of ceramic chip capacitors. Some are concerned with whether metal migration might occur, and, and its possible impact on performance.

The most common concern is the possible migration of silver between two opposed capacitor electrodes. In the presence of a DC electric field and moisture , pure silver has a tendency to migrate toward the negative potential. If the ceramic chip capacitor were to have a crack or a void between opposed interior electrodes, this could lead to silver migration through the void or crack, and could cause electrical conduction between the 2 opposed electrodes within the capacitor.

Silver migration would tend to occur faster in a humid environment as the DC voltage increased. Thus, higher voltages would cause more rapid silver migration. However, higher voltages also provide more "clearing" energy, which tends to dissipate the migration path. On the other hand, low voltages and high source impedances tend to limit the "clearing" energy, and thus allow the migration path to worsen. As a result, the low voltages could result in unacceptable levels of insulation resistance in the chips. Indeed, the US Military imposed a test to check for this phenomenon in MIL-C-123 and MIL-C-55681. In that test, the chips are mounted on circuit boards, and are subjected to 240 hours of low voltage (1.2 ± 0.25 volts DC) applied through a current limiting high resistance of (100 KOhms) in an 85°C 85% relative humidity moisture-laden environment.

However, KEMET surface mount ceramic chips have not been associated with this "low voltage" failure mode. We have routinely tested our chips against the military specifications without problems, and we attribute our good performance to:

...The "low voltage" failure mode requires internal cracks and voids to provide a path for development of migration. KEMET chips demonstrate extremely low levels of internal cracks and voids, thus making them resistant to failure.

...KEMET ceramic chips are thermally robust, so that the customer is less likely to cause internal cracking during mounting on his circuit boards.

...KEMET ceramic chips include palladium with the silver in their electrodes. The palladium exerts a strong inhibiting effect on silver mobility, and thus decreases the possibilities of silver migration.

One remaining area needs to be considered - that is surface conduction in low voltage applications, particularly in the presence of high humidity. When the circuit board is intended for use in a high humidity environment, then the customer needs to thoroughly clean and protect the circuit boards after assembly. This helps to prevent formation of a conductive path on either the circuit board or on the outer surface of the capacitor. Contaminants such as flux could combine with moisture, and result in ionic surface conduction. Additionally, the ionics can help to form electrolytic cells which can also cause separation and migration of external metal components of the solder and the capacitor end metallizations. In extreme cases, even the lead from the solder can be induced to migrate. Other metals from the solder, the circuit board pads, and the end terminations of the capacitors could also migrate in extremely severe conditions. While surface conduction is not a failure of the capacitor itself, it does represent a condition which would be unacceptable to the customer. Thus, in the case of high humidity low voltage circuits, KEMET recommends thorough circuit board cleaning, with care being taken to clean under surface mount components. For extremely high humidity applications, protection against moisture should be taken, either in the form of a case or a protective overcoat.

Thanks to Dr. L. Mann in Technology for his review and insights for this material.

Dick Thompson

rjt\lowvolt.sam