LET Threshold Settings

4.8.01

Detector	Area cm2	Thick (micron)	Detect. Cap. (pf)	Est. (1) Noise (MeV)	Minimum Thresh (MeV) (=5xn)	Nominal Hi-gain Thresh (MeV)	Min. Setting (MeV)	Hi-gain Full (2) Scale (MeV)	Delta (3) Adjust. (MeV)	Max. Hi-gain Thresh (MeV)	Min. Lo-gain Thresh (MeV)	Delta (3) Adjust. (MeV)	Max. Hi-gain Thresh (MeV)	Nom (4) Hi-Rate Thresh (MeV)	Lo-gain Full (2) Scale (MeV)
L1i	0.4	15	304	0.035	0.18	0.3	0.25	125	0.025	3.45	2.00	0.20	28	3	1000
L1o	1.6	15	1214	0.133	0.67	0.7	0.25	125	0.025	3.45	2.00	0.20	28	3	1000
L2	0.64	50	146	0.018	0.09003	0.3	0.30	150	0.05	6.7	2.40	0.40	54	4	1200
L3i	2.8	1000	32	0.006	0.029	1	0.80	400	0.1	13.6	6.40	0.80	109	1	3200
L3o	13.2	1000	150	0.018	0.092	1	0.80	400	0.1	13.6	6.40	0.80	109	20	3200

HET Threshold Settings

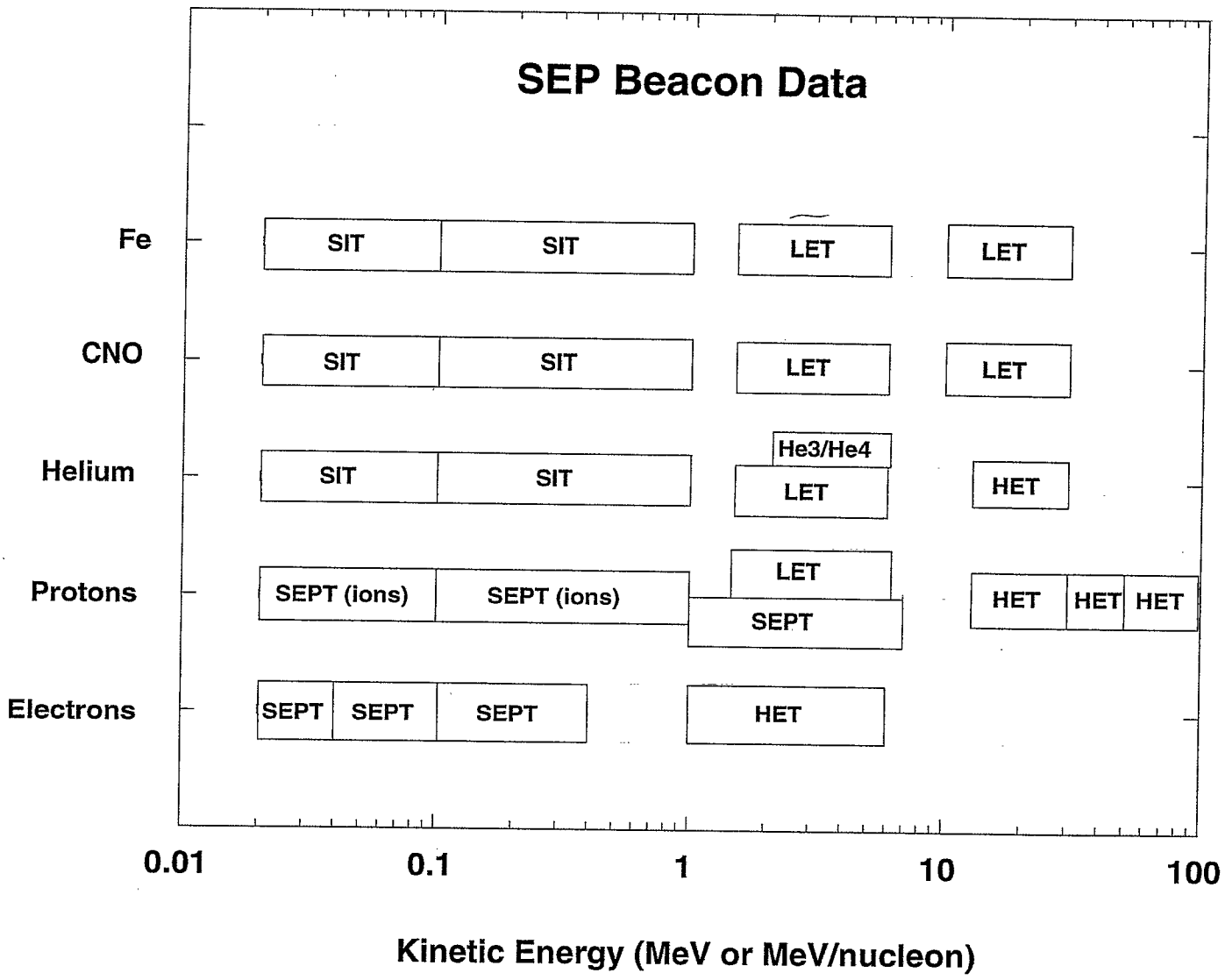
Detector	Area cm2	Thick (micron)	Detect. Cap. (pf)	Est. (1) Noise (MeV)	Minimum Thresh (MeV) (=5 x n)	Nominal Hi-gain Thresh (MeV)	Min. Setting (MeV)	Hi-gain Full (2) Scale (MeV)	Delta (3) Adjust. (MeV)	Max. Hi-gain Thresh (MeV)	Min. Lo-gain Thresh (MeV)	Delta (3) Adjust. (MeV)	Max. Hi-gain Thresh (MeV)	Nom (4) Hi-Rate Thresh (MeV)	Lo-gain Full (2) Scale (MeV)
H1i	0.5	1000	6	0.003	0.014	0.2	0.18	100	0.02	2.74	1.44	0.16	22	0.20	720
H1o	2.64	1000	30	0.006	0.028	0.2	0.18	100	0.02	2.74	1.44	0.16	22	16	720
H2	3.14	1000	36	0.006	0.031	0.2	0.18	100	0.02	2.74	1.44	0.16	22	0.20	720
H3,H4,H5	12	2000	273	0.032	0.159	0.45	0.45	225	0.02	3.01	3.60	0.16	24	0.50	1800
H6	12	1000	137	0.017	0.085	0.2	0.18	100	0.02	2.74	1.44	0.16	22	0.20	720

Notes:
(1) Estimated noise = (Detector capacitance + 21 pf) x 0.108 keV
(2) Dynamic range = 500 for both low and high gain; nominal high/low gain factor = 8
(3) Nominal thresholds can be adjusted (by command) to accommodate range of thicknesses and noise
(4) For L1, L2, L3o, and H1o the low-gain thresholds may be used during high-rate periods

SEP Beacon Data

12.12.00

SEP Sensor	Species	(MeV or MeV/nuc) E1	E2	Geometry Factor (cm2sr)	Number of Directions Summed Over	Time Resolution (sec)	Min. Observable 1-minute Flux (/cm2sr.sec.MeV)	bps
SIT	He	0.02	0.1	0.3	1	60	6.9E-01	0.27
		0.1	1	0.3	1	60	6.2E-02	0.27
	CNO	0.02	0.1	0.3	1	60	6.9E-01	0.27
		0.1	1	0.3	1	60	6.2E-02	0.27
	Fe	0.02	0.1	0.3	1	60	6.9E-01	0.27
		0.1	1	0.3	1	60	6.2E-02	0.27
SEPT	Electrons	0.02	0.04	0.8	4	60	1.0E+00	0.27
		0.04	0.1	0.8	4	60	3.5E-01	0.27
		0.1	0.4	0.8	4	60	6.9E-02	0.27
	Ions	0.02	0.12	0.96	4	60	1.7E-01	0.27
		0.12	1	0.96	4	60	2.0E-02	0.27
		1	7	0.96	4	60	2.9E-03	0.27
LET	Protons	1.5	6	0.9	10	60	4.1E-03	0.27
	Helium	1.5	6	4.5	10	60	8.2E-04	0.27
	3He/4He	2	6	2	10	60	2.1E-03	0.27
	CNO	1.5	6	4.5	10	60	8.2E-04	0.27
	CNO	10	30	4.5	10	60	1.9E-04	0.27
	Fe	1.5	6	4.5	10	60	8.2E-04	0.27
	Fe	10	30	4.5	10	60	1.9E-04	0.27
HET	Electrons	1	4	0.5	1	60	1.1E-02	0.27
	Protons	13	30	0.7	1	60	1.4E-03	0.27
		30	50	0.7	1	60	1.2E-03	0.27
		50	100	0.7	1	60	4.8E-04	0.27
	He	13	30	0.7	1	60	1.4E-03	0.27
								6.67


SEP Beacon Data
Fe
CNO
Helium
Protons
Electrons
SIT
SIT
LET
LET
SIT
SIT
LET
LET
SIT
SIT
He3/He4
LET
HET
LET
SEPT (ions)
SEPT (ions)
SEPT
HET
HET
HET
SEPT
SEPT
SEPT
HET
0.01
0.1
1
10
100
Kinetic Energy (MeV or MeV/nucleon)

Warning of the Onset of Large Solar Particle Events

- As we move into an era when the space station will be continuously occupied, it becomes more important to have warnings (nowcasts) of the onset of large solar particle events.

- The particle flux seen at Earth depends critically on how well it is connected to the shock. The degree of connection can vary quickly as the shock moves outward.

- Although it may be impossible to track the Stereo spacecraft continuously, their location at longitudes well separated from Earth can be an important advantage.

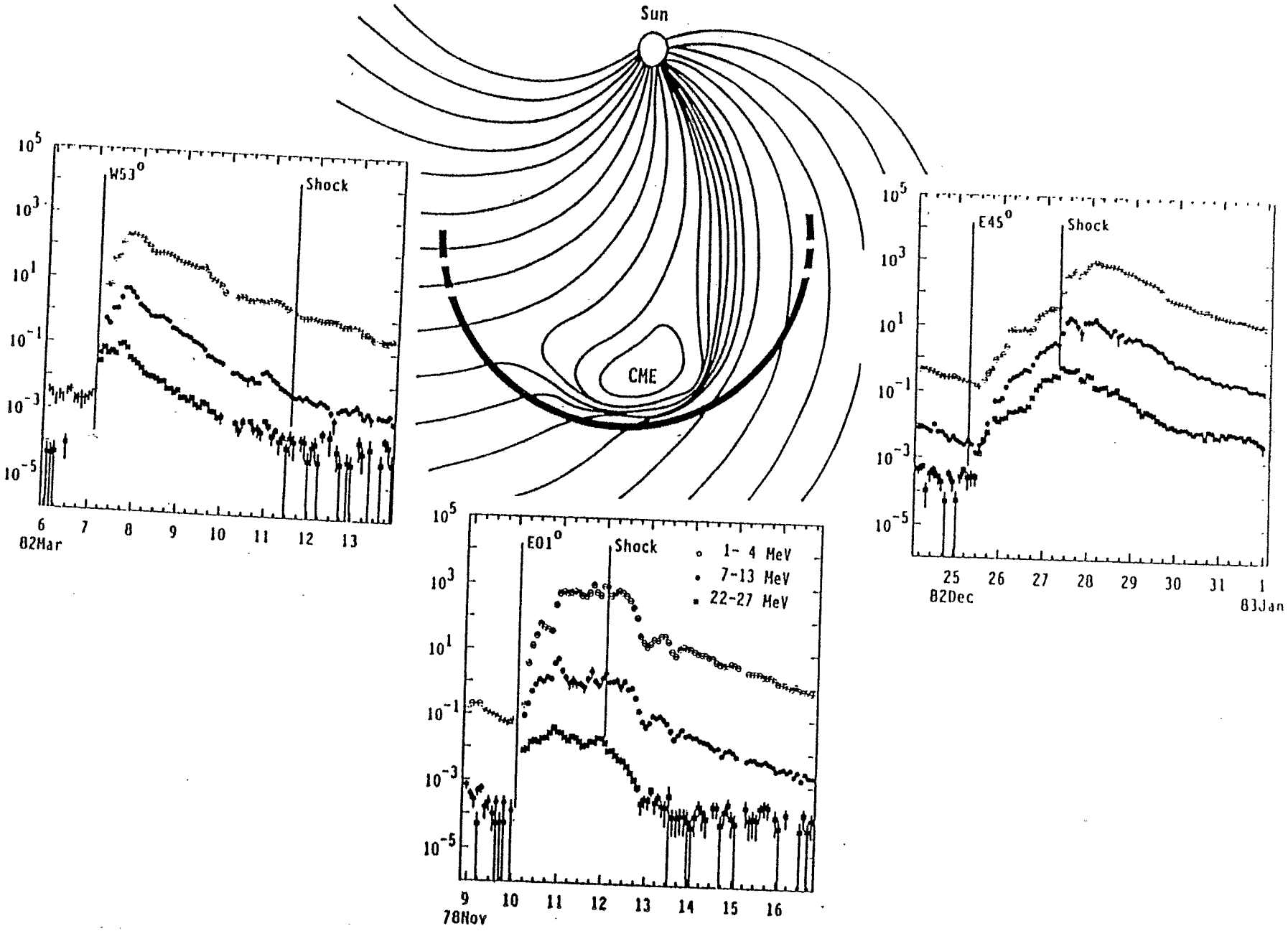
- In cases where the Earth is magnetically connected to the shock at the time of its formation, little warning is possible, and an L1 monitor is adequate.

- A spacecraft located 60 to 90 deg east of Earth will in many cases be magnetically connected to the shock well before the Earth is, and a warning of hours to days is possible.

- Multiple spacecraft connected to the shock typically all see similar fluxes. This means that any location that is connected can be used to forecast the fluxes that other locations will see, once connected.

- Whenever particle fluxes at one of the Stereo spacecraft exceed established threshold levels a warning should be sent.

- Depending on the situation (e.g., astronauts on EVA), this warning might result in emergency tracking.


Sun
CME
W53°
Shock
E01°
Shock
1- 4 MeV
7-13 MeV
22-27 MeV
E45°
Shock
82Mar
78Nov
82Dec
83Jan

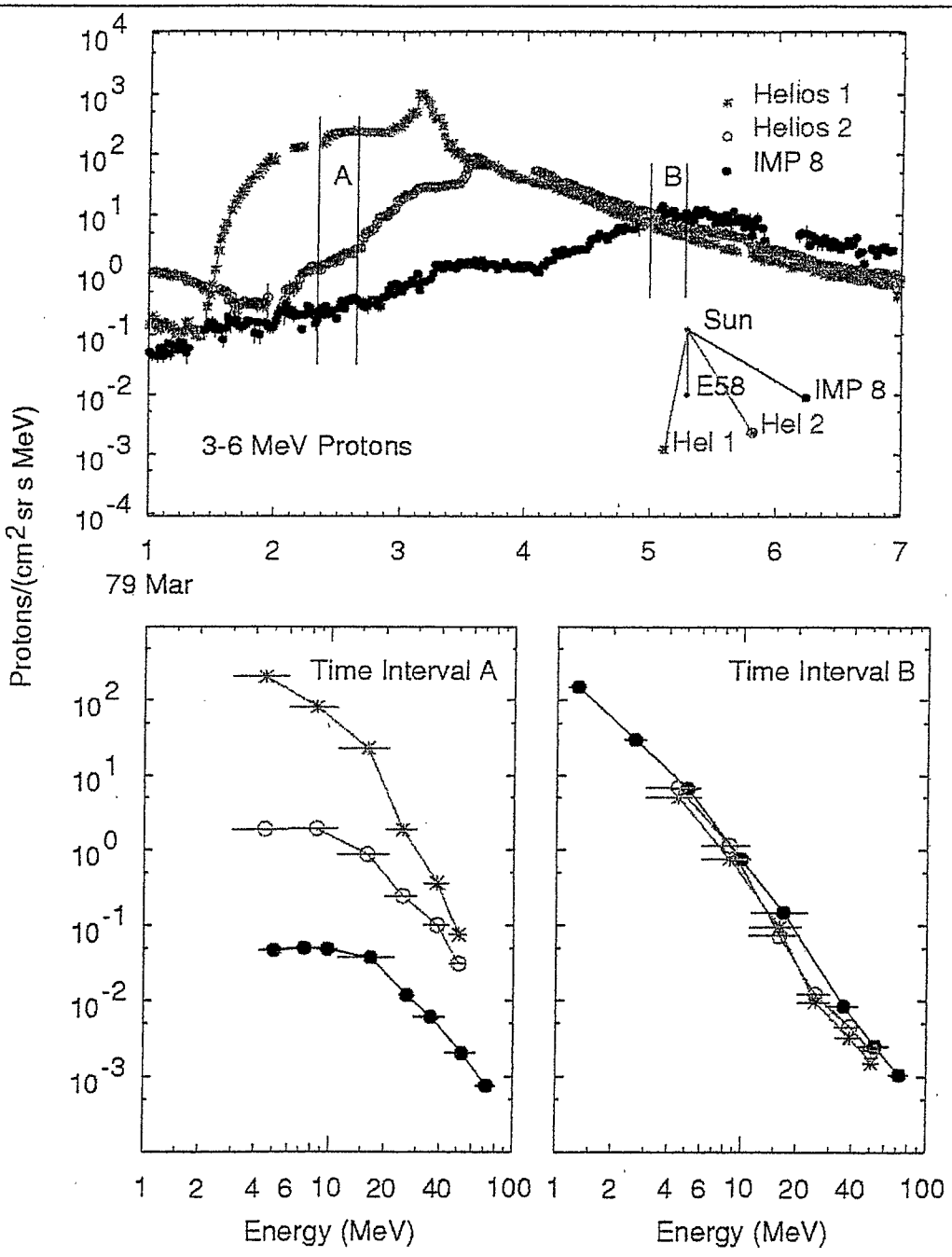


Fig. B.8 Multi-spacecraft observations of a small SEP event from longitudes shown on the inset. Energy spectra at the 3 locations are shown at times A and B. (Reames, Kahler, and Ng 1997).

LET L1 Silicon Detector Development Status

M. Wiedenbeck JPL

Background

- Thin Si detectors (< 20 μm) with areas of a few cm^2 have been flown (most notably on Wind/LEMT).
- Thin Si detectors flown to date have been made using surface barrier technology. This technology is sensitive to surface contamination problems and has largely been supplanted by ion-implantation technology which leads to much more robust detectors.
- Si detectors thin enough for STEREO/LET have not been commonly made. For example, the thinnest ion-implanted detectors previously made by Micron Semiconductor were 30 μm thick.

Thin Si Detector Development Project

- JPL / Caltech is presently involved in a technology study related to the development of thin, large-area Si detectors.
- Because of STEREO needs for L1 detectors, some work was started in late 1999 to understand and improve capabilities for making thin detectors of the 2 cm^2 area needed for LET
- Two approaches have been tried:

  A: conventional fabrication from Si wafers (3 inch diameter) lapped and polished to the desired detector thickness

  B: etching of a thicker Si wafers down to the desired thickness over the smaller area needed for the detector

Progress to Date at Micron Semiconductor

- A number of improvements in detector fixturing and processing techniques were developed by Micron Semiconductor to allow successful fabrication of thin detectors.
- Micron has already delivered thin detectors (thickness range: 13 to 24 μm) made with the two techniques. A total of 14 such detectors (4 of type A, 10 of type B) are presently being characterized at Caltech / JPL.
- Even with Micron's process improvements, the yield of detectors produced using method A has been very low.
- The yield of detectors produced using method B has been significantly better. However, most such detectors tested thus far have poor thickness uniformity.

Silicon Thinning by JPL / MDL

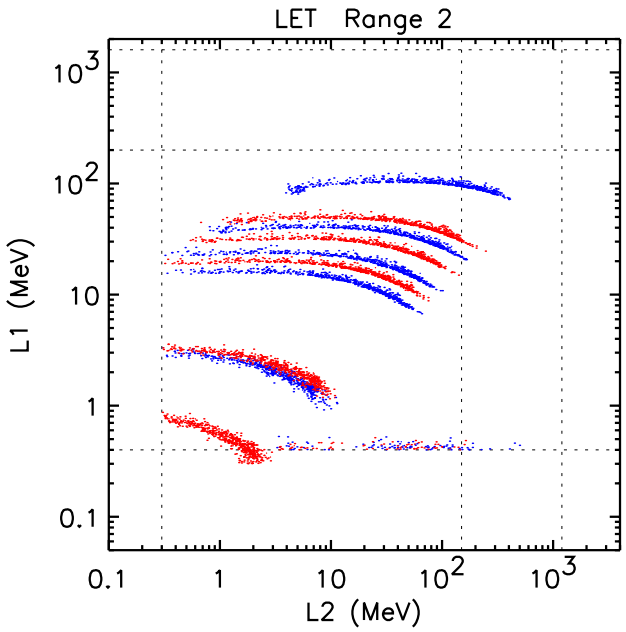
- As part of the Thin Silicon technology project, the JPL Micro-Devices Laboratory (MDL) has been working on alternative etching techniques to produce more uniform Si membranes.
- Tests of a first MDL sample at Caltech / JPL indicate that it has much better thickness uniformity than Micron-etched samples.
- Silicon thinning process being used at JPL relies on KOH as the etchant.
- There are issues with processing the KOH-thinned silicon to make detectors:
    - KOH-etched silicon has a rough ("orange peel") surface on small scales. This might interfere with uniform ion implantation.
    - Residual potassium could migrate around during high temperature (1100°C) oxidation step, ruin oxides, and contaminate the oven.

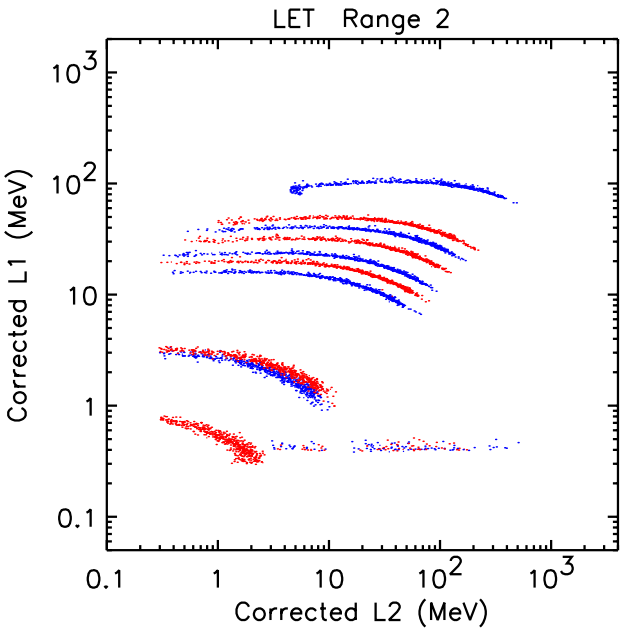
Plan for Fabrication from JPL-thinned Silicon

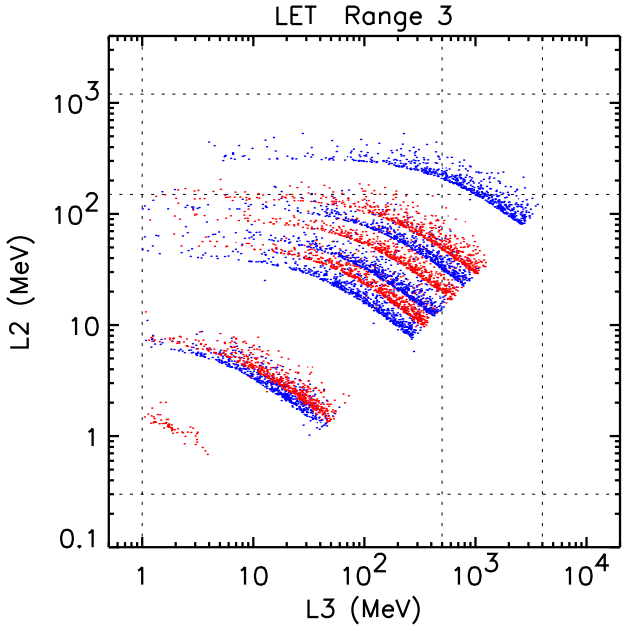
- A process for surface-smoothing has been found, involving a brief finishing etch in a gas of XeF_2 + He.
- Micron Semiconductor and JPL / MDL have agreed on a process flow which should avoid problems with potassium contamination:
    1. Micron supplies Si wafers to be thinned
    2. JPL grows nitride masking layer on back surface
    3. Micron does front-side (junction surface) processing of detector—high temperature oxidation occurs before KOH etching
    4. JPL thins desired regions from back side using KOH
    5. Micron does back-side processing and assembly of detector
- JPL / MDL has a new technique for achieving the desired absolute thickness:
    1. pre-etch small test areas of thick wafer to depth corresponding to desired thickness (by timing the etch)
    2. etch the entire wafer until test sections just etch through to other surface—silicon remaining in other areas should equal the depth of the pre-etch

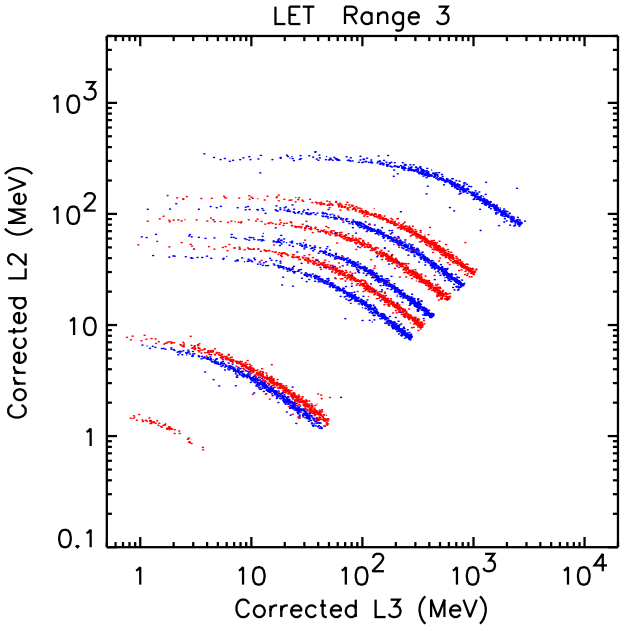
Backup Plans

- Use detectors thinned by Micron:
  - best examples have marginally-acceptable thickness nonuniformity
  - may require producing a large number of samples, measuring thickness nonuniformity, and selecting the best ones
- Use detectors made from silicon wafers lapped and etched thin
  - low yield could significantly increase costs and introduce schedule risk
  - don't have enough examples to know whether the thickness nonuniformity measured thus far is typical
- Use surface barrier detectors
  - have not yet determined ability and willingness of potential manufacturers to supply such detectors
  - manufacturing may also have poor yields
  - use would raise concerns about LET high-temperature limit and vapor contamination of sensitive surfaces
  - some spares are available from Wind/LEMT but: not enough; poorest from set produced for Wind; would require modification of LET mechanical design









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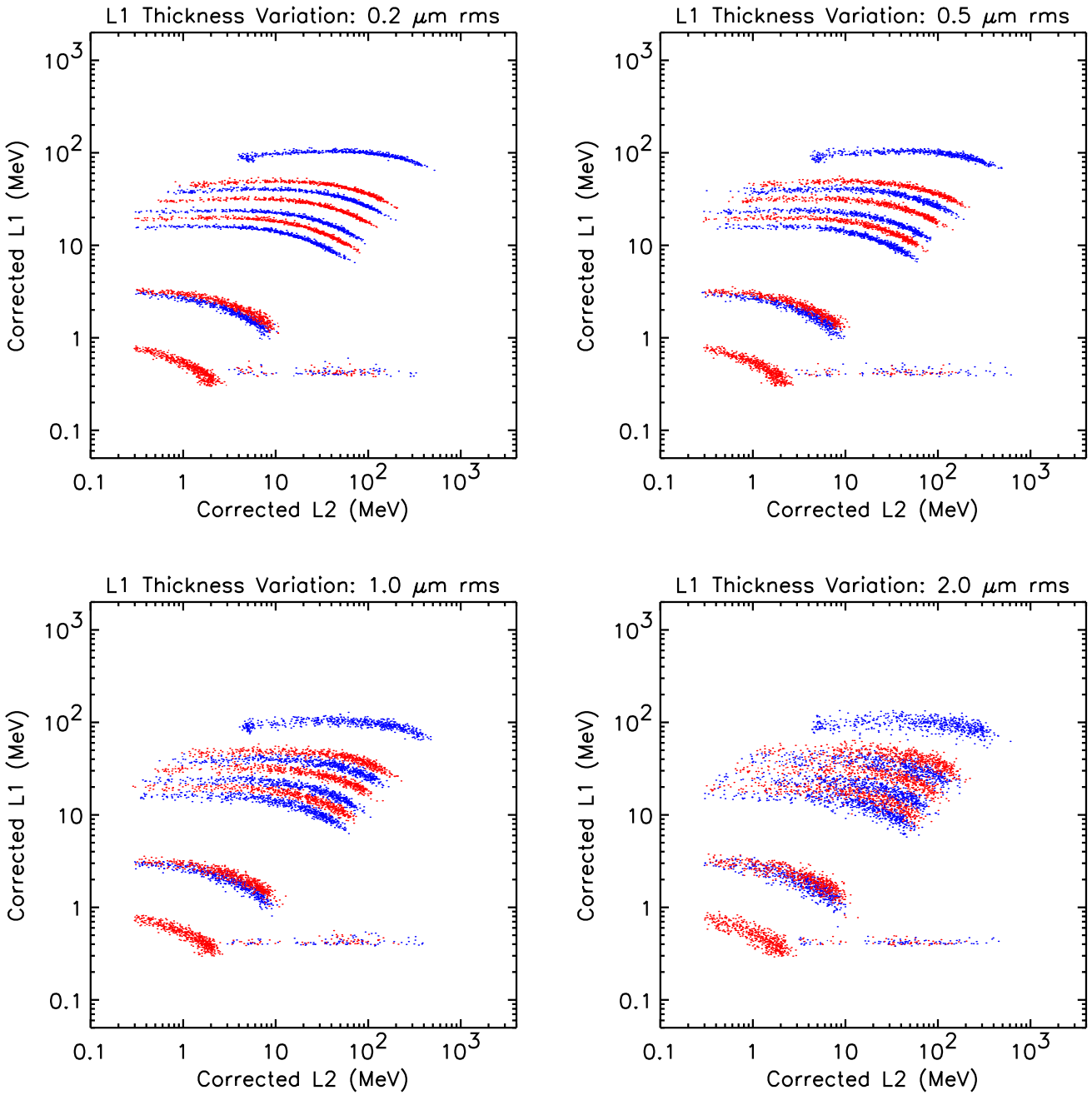
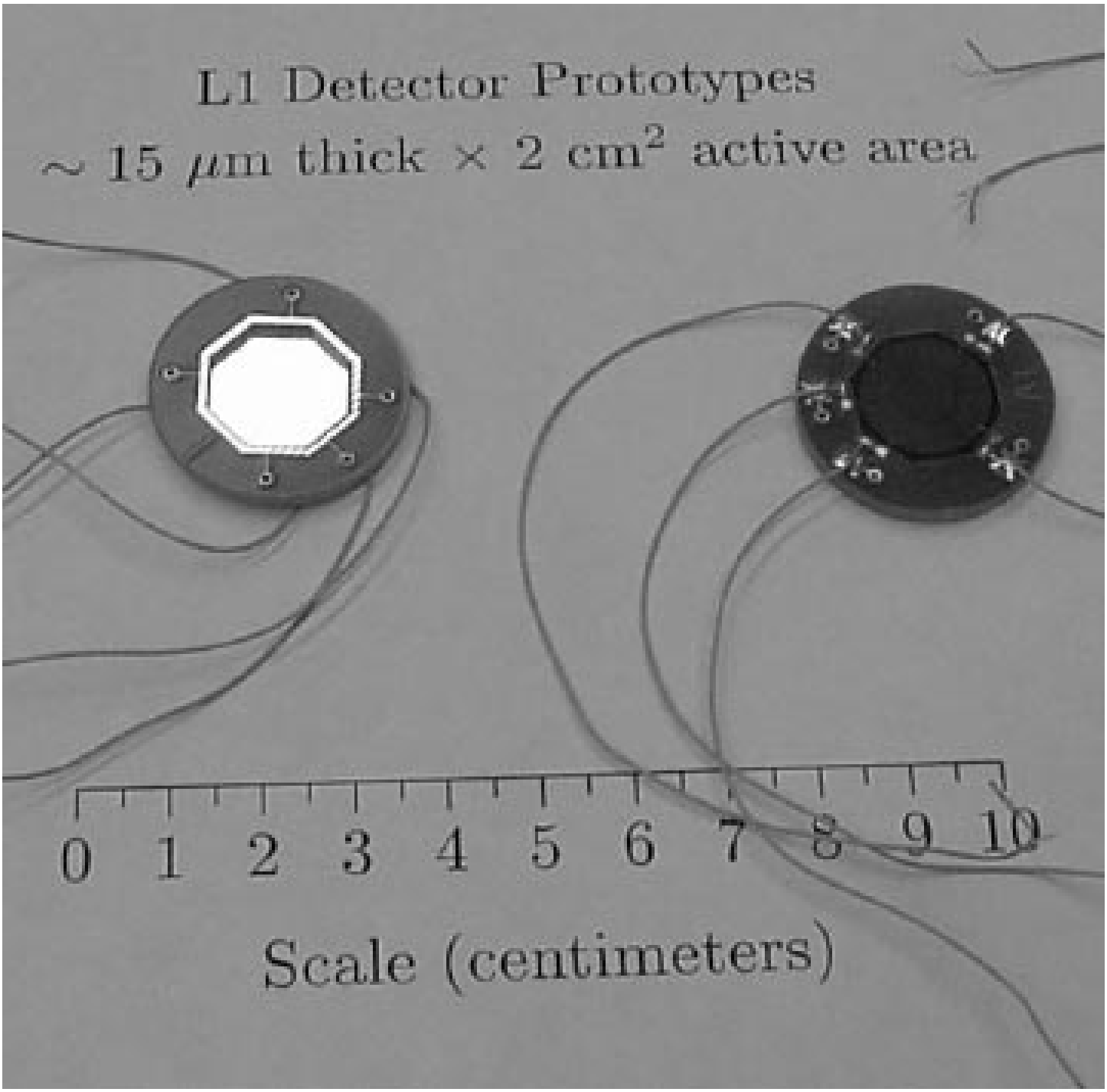
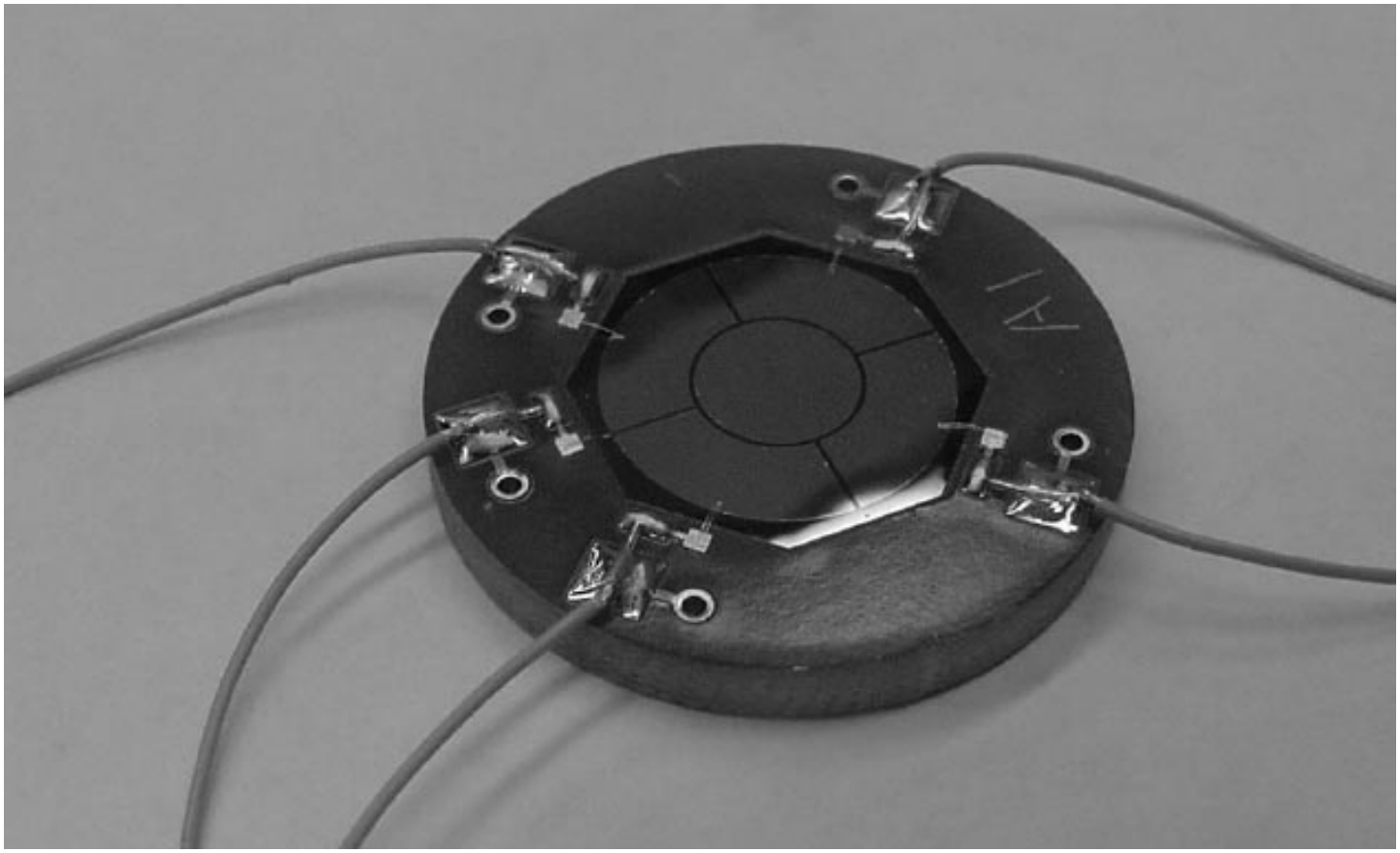
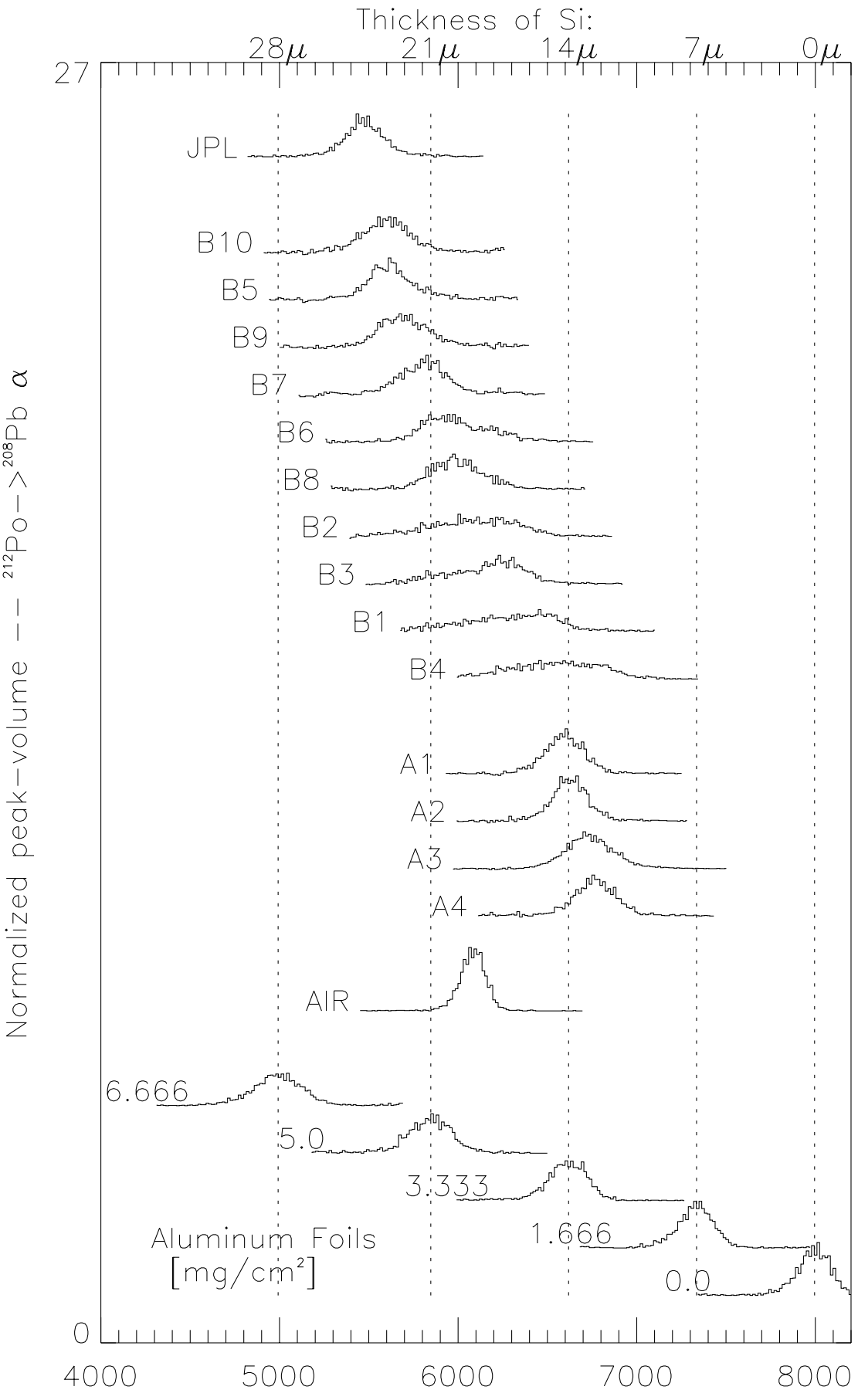
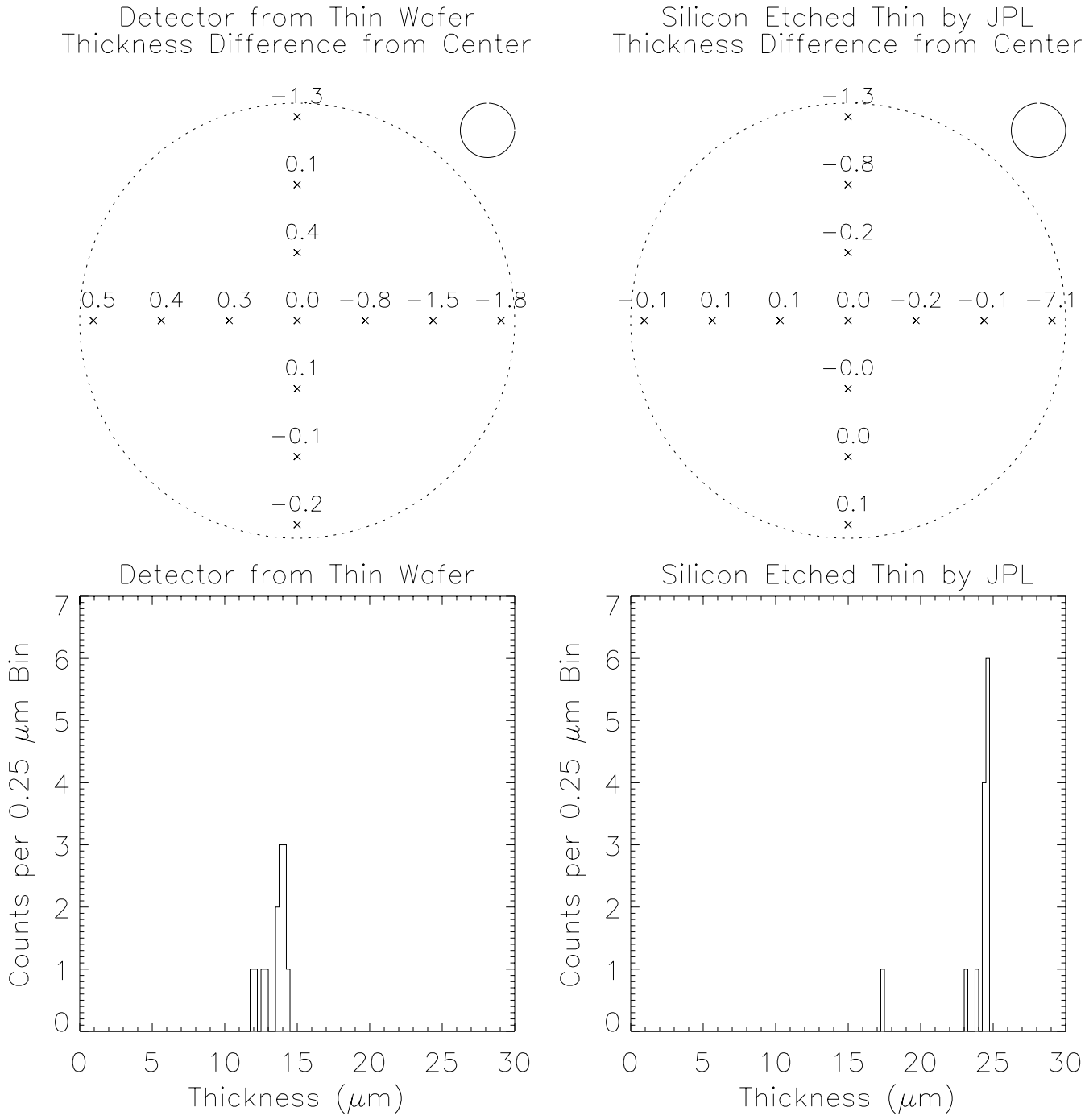

L1 Thickness Variation: 0.2 μm rms
L1 Thickness Variation: 0.5 μm rms
L1 Thickness Variation: 1.0 μm rms
L1 Thickness Variation: 2.0 μm rms
Corrected L1 (MeV)
Corrected L2 (MeV)
0.1
1
10
10^2
10^3


L1 Detector Prototypes
$\sim 15\ \mu$m thick $\times$ 2 cm^2 active area
0 1 2 3 4 5 6 7 8 9 10
Scale (centimeters)


A1


Thickness of Si:
28μ
21μ
14μ
7μ
0μ
27
0
JPL
B10
B5
B9
B7
B6
B8
B2
B3
B1
B4
A1
A2
A3
A4
AIR
6.666
5.0
3.333
1.666
0.0
Aluminum Foils
[mg/cm²]
Normalized peak-volume --- $^{212}Po \rightarrow ^{208}Pb$ α
4000
5000
6000
7000
8000



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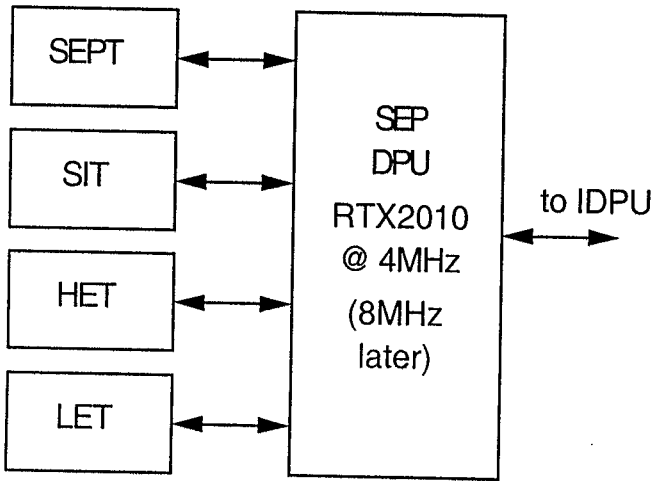
MISC Story: Part I, the Problem.

1) During Phase A realized that we were squeezed everywhere: power, mass, schedule, budget, ...

2) Key risk element: frontend VLSI development.

3) Needed to SIMPLIFY the overall design (and VLSI design especially), and improve the distribution of effort at the various collaborating institutions.

MISC Story: Part 2, the Original Concept (and its Disadvantages).



1) Single processor requires event selection within LET and HET -- complicates both VLSI design and logic design.

2) Since accumulation of counts is done in the processor, SIT, HET and LET interfaces are "high bandwidth".

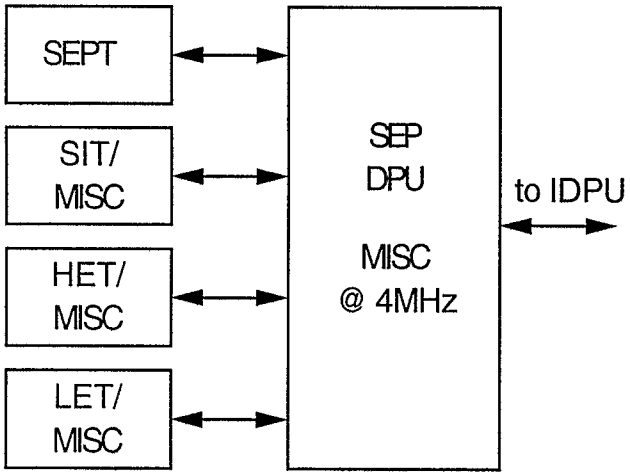
3) SIT, HET, and LET are not easily tested separately.

4) Interactions between SIT, HET and LET processing difficult to test.

5) Distribution of effort is overly concentrated at institution responsible for SEP DPU.

6) Project and team members concerned about ability of single RTX2010 to meet requirements

MISC Story: Part 3, the new Concept (and its Advantages).



1) Processing power is distributed to SIT, HET, and LET.

2) Total processing capability is increased without substantial increase in weight or power.

3) Front-end logic and VLSI are simplified.

4) SIT, HET, and LET are easily tested separately.

5) Interfaces are all "low bandwidth".

6) Allows more even distribution of institutional effort -- a plan that works.

MISC Story: Part 4, What is a MISC?

1) "Minimal Instruction Set Computer"

2) Scalable architecture designed by Chuck Moore, inventor of FORTH and designer of the RTX2010.

3) Development began in early 1990's with goal of enhanced performance and simplicity.

4) Dual-stack architecture, with 5 bit "operandless" instructions and multiple instructions per memory word.

5) Simple "cacheless" method to achieve high instruction execution rate per unit memory bandwidth.

6) Several designs (p8, p24, etc.) implemented by Dr. C. H. Ting in FPGAs, using both schematic and VHDL descriptions.

MISC Story: Part 5, Where are We?

1) "p24" MISC (with UART) has been implemented in Actel 54sx72a.

2) Fully functional development board uses p24 MISC, 128kx24 SRAM and 128kx24 EEPROM. Boots from EEPROM or serial link. 5 units fabricated and working.

3) "p24" hardware definition, FORTH operating system, and PC based cross-development system, including PC-based MISC simulator, provided via sub-contract with Dr. C. H. Ting.

4) Basic p24 MISC enhanced for our needs: 5 bit --> 6 bit instruction to obtain fast i/o and "Gbus" analogous to RTX2010; prioritized interrupts (7).

5) FORTH system augmented with resident assembler, optimizing compiler, fast multi-tasker, and interrupt driven serial i/o.

6) Suite of test programs provided by Dr. Ting used to aid validation of hardware and FORTH system.

7) Prototype LET event processing algorithm has been tested both on p24 MISC and RTX2010 systems for performance comparison.

STEREO PHA ASIC

1) Complete front-end signal pulse processing for Silicon detectors in LET, HET and SIT.

2) Contains 10 complete dual-gain PHAs, each with:
   A) Preamplifier, configurable to various detector capacitances and signal amplitude ranges.
   B) Two complete shaping amplifier-linear gate-Wilkinson ADC chains, with combined dynamic range of 4000 (F.S./threshold).
   C) Programmable thresholds
   D) Bias switching to enable or disable power.
   E) Scalar (20 bits) for counting trigger rate.

3) Pulse processing chain architecture due to H. Marshall, with 25 years of development/use in numerous space applications.

4) Evolution from ASIC developed for Advanced Composition Explorer:
   A) Bipolar ---> CMOS
   B) Critical passives off-chip ---> Most critical passives on-chip
   C) No digital on-chip ---> Complete digital support on-chip
   D) Dynamic range: 2000 ---> 4000
   E) Max ADC conversion time 256 usec ---> 32 usec
   F) Shaping time constants: 2 usec ---> 1 usec.
   F) Power consumption (per chain) 40 mW ---> 5 mW.

STEREO PHA ASIC Development

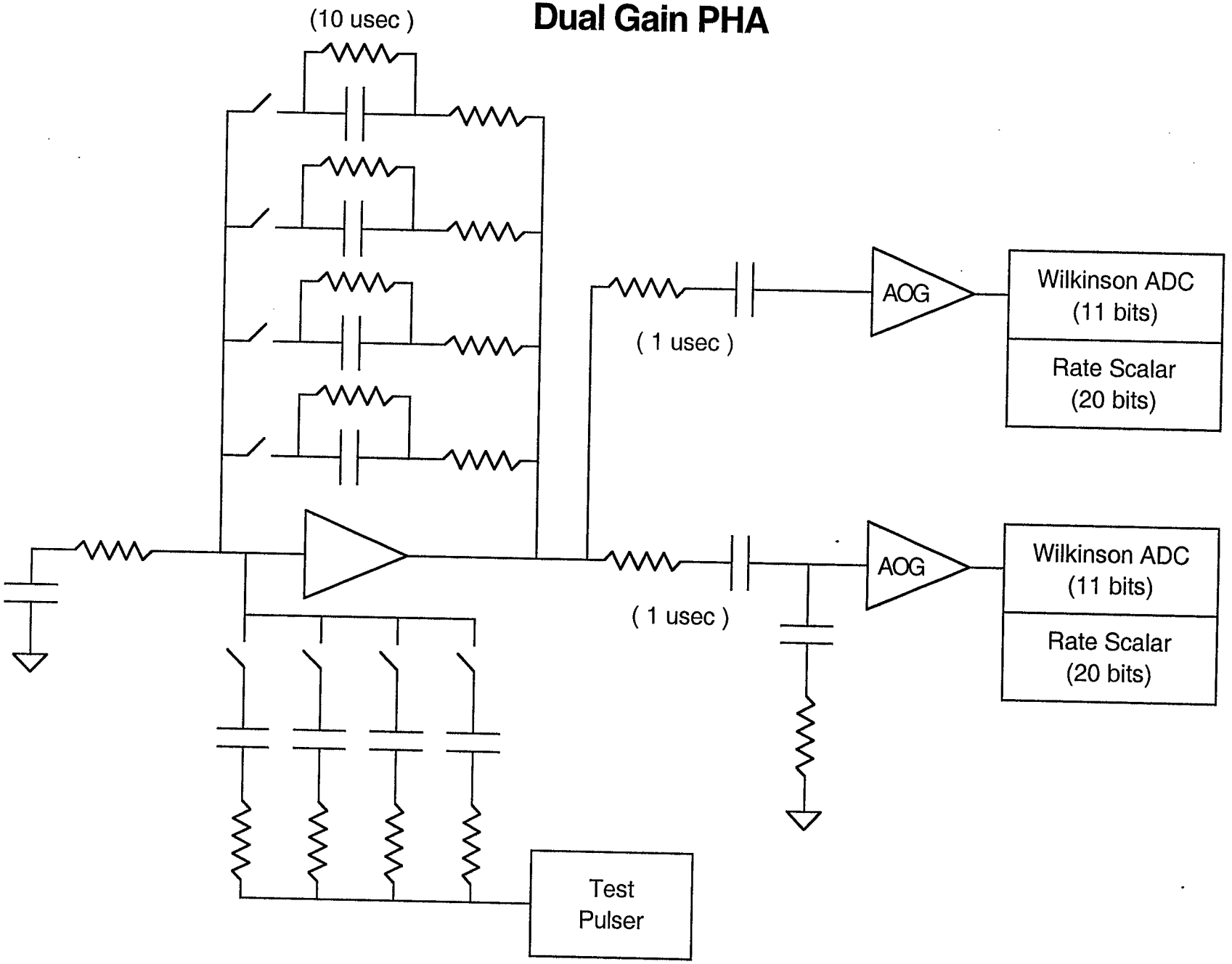
1) Experience with AMI 0.5 uM "C5N" fab gained through MOSIS:
   - A) Prototype of critical pulse chain elements (2 runs)
   - B) Prototype of pixel detector readout for gamma-ray telescope.
   - C) First-time success on all analog functions ---> accurate SPICE modeling achieved.
   - D) Noise performance verified, SPICE noise parameters measured.
   - E) Process characterized down to 85K in collaboration with MOSIS.

2) Design simplifications:
   - A) "Digital discriminators" removed.
   - B) Low-gain pulse-shaping made identical to high-gain ---> prototyping run eliminated.
   - C) "Fast Reset" for Wilkinson PHAs not added.

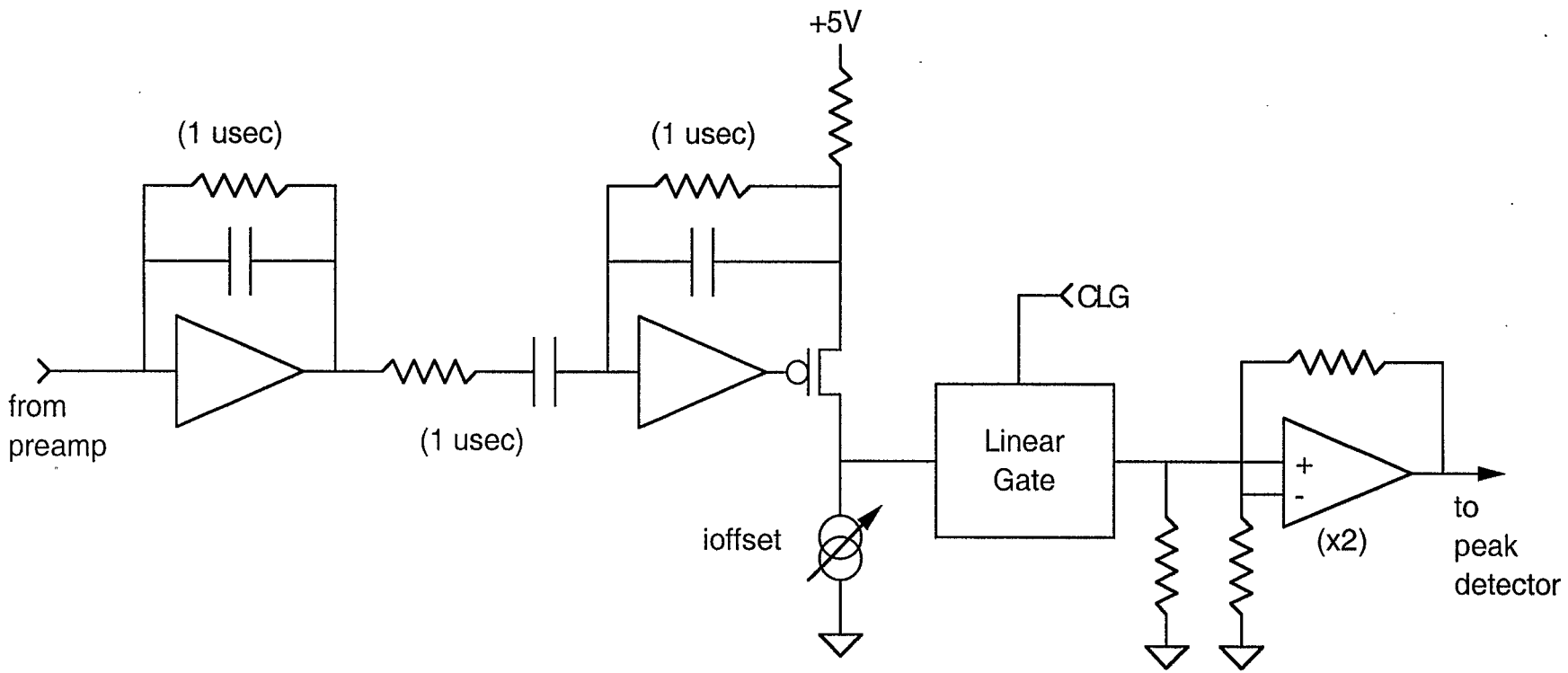
3) Key Development Milestones:
   - A) Next fab run to be potential flight-fab, via direct submission to AMI. Goal of parts available late Aug. 2001.
   - B) PHA ASIC user's manual to be distributed to team members mid-May 2001.

4) Rad-tolerance:
   - A) "Hardness-by-Design" methodology should yield high latch-up threshold (guard banding) and SEE immune flip-flops.
   - B) Plan latch-up threshold testing with help of Aerospace Corp. and total dose testing at JPL.
   - C) Backup plan -- respin with UTMC rad-hardening process additions.

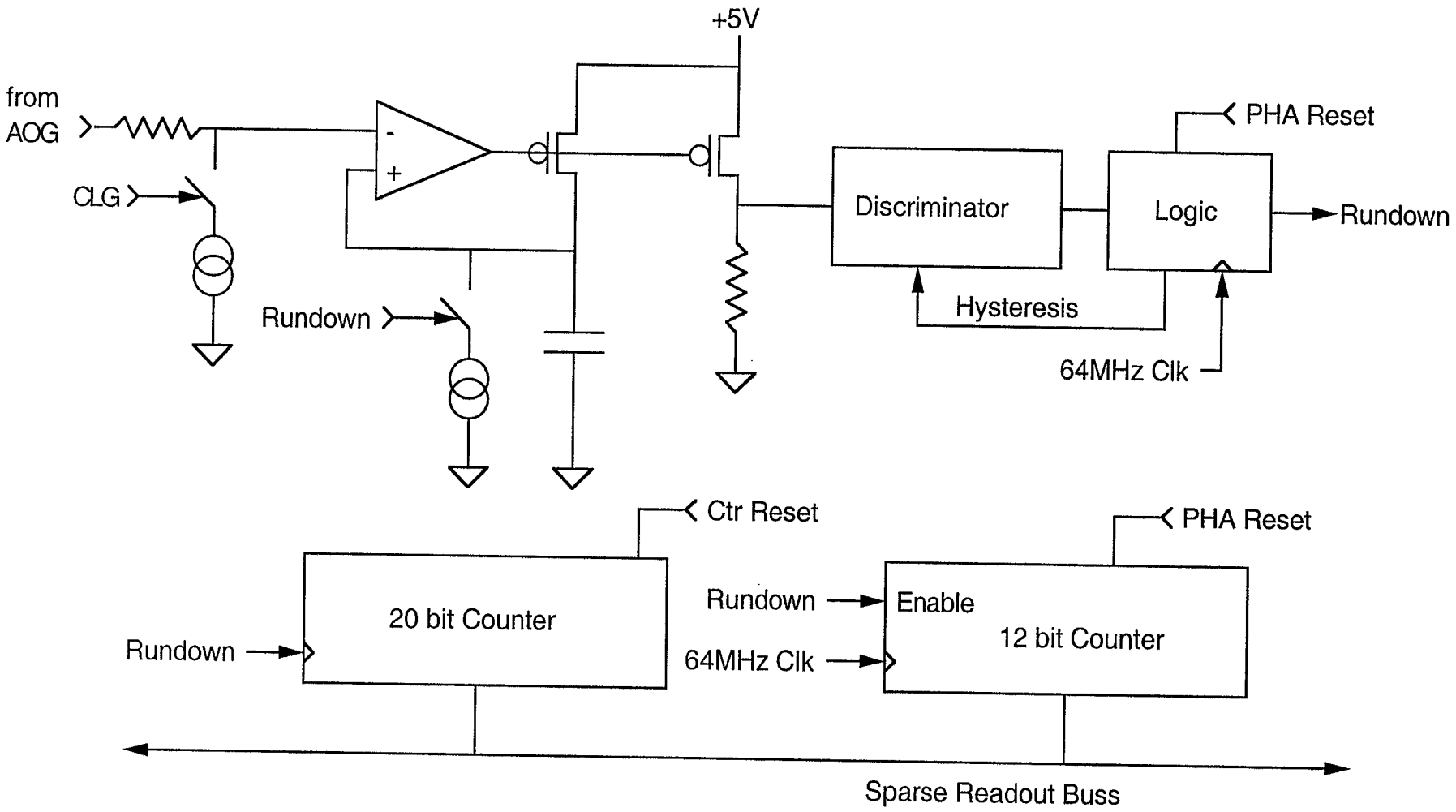
Dual Gain PHA



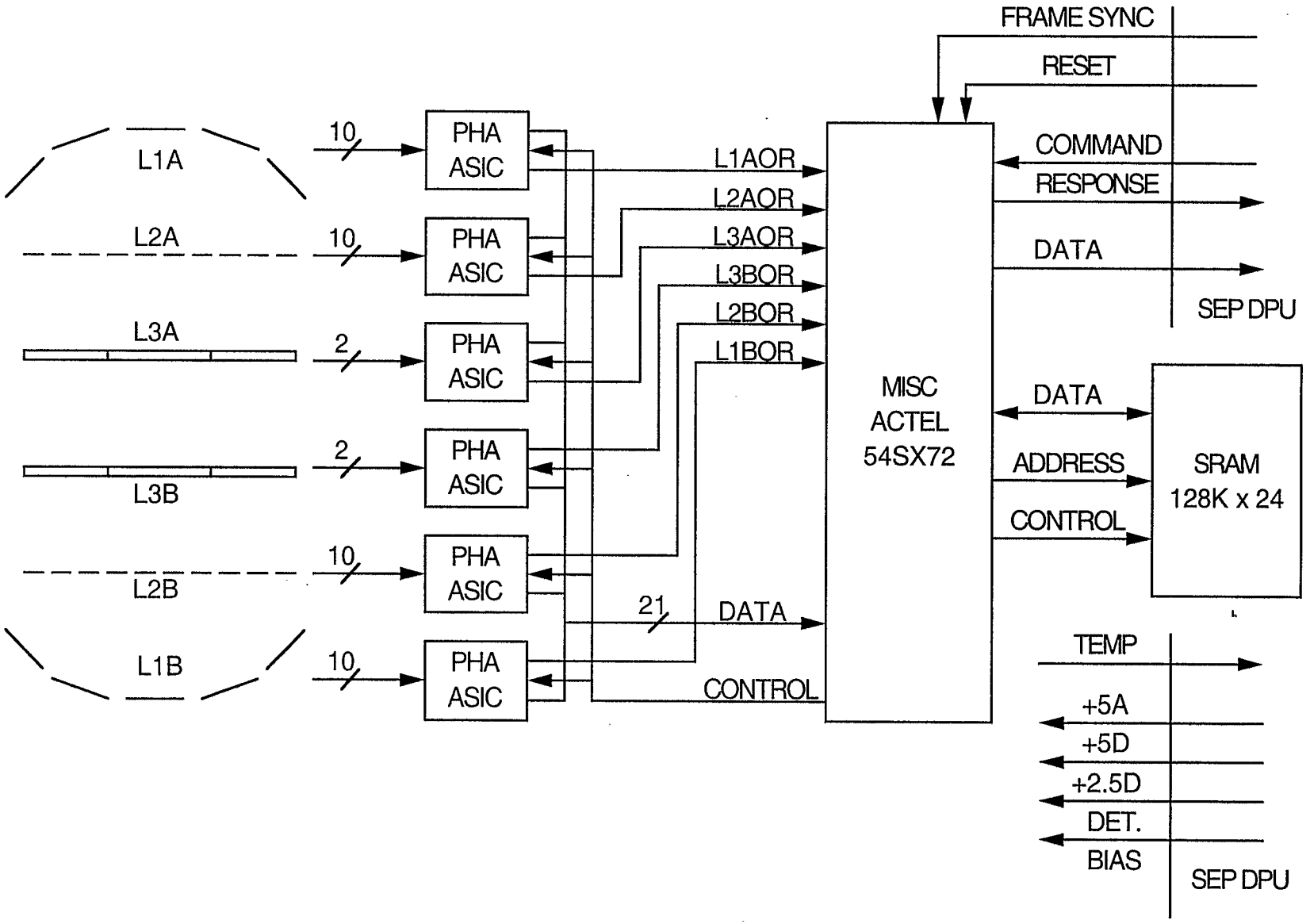
Amplifier/Offset/Gate (AOG)



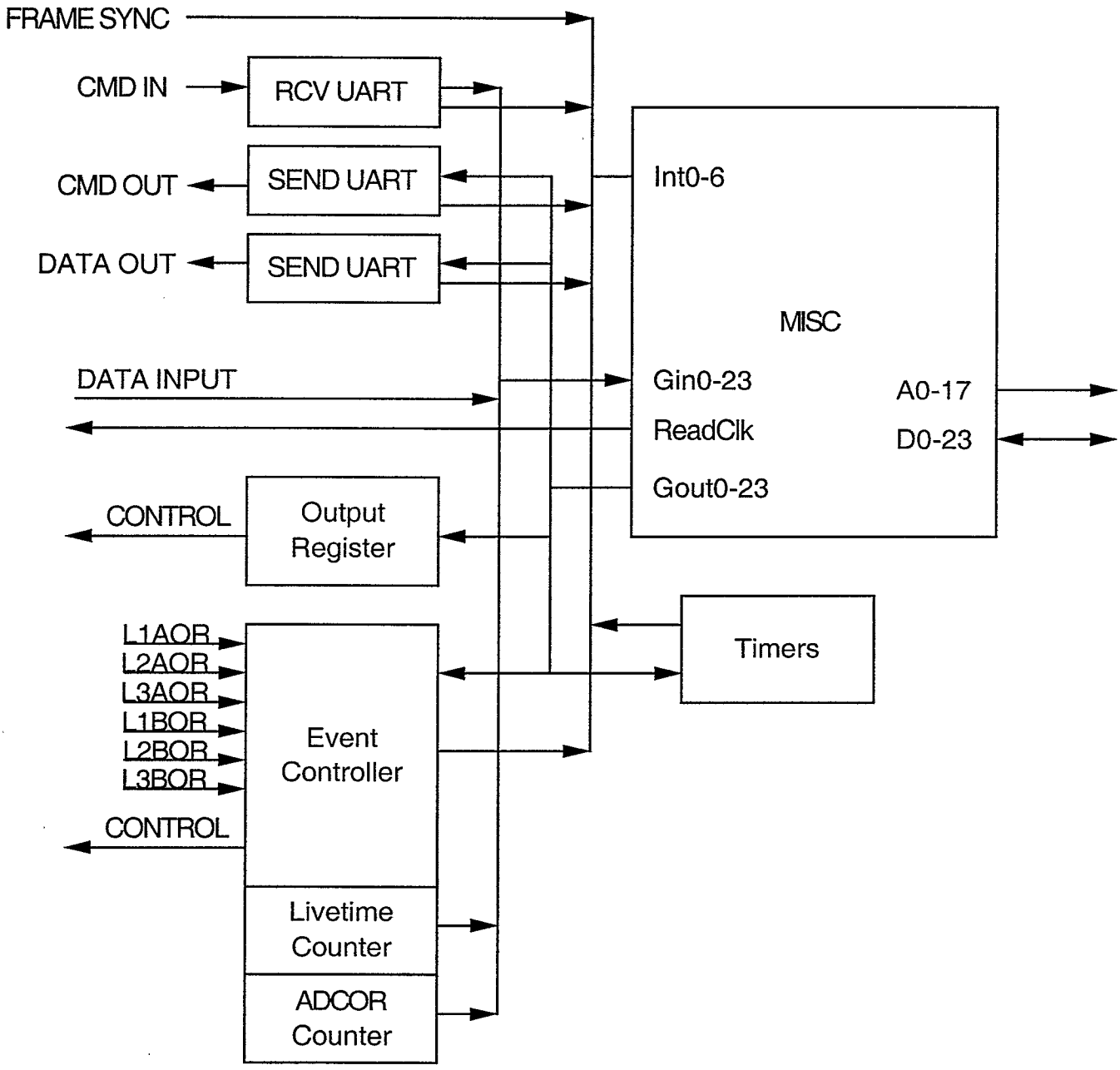
Wilkinson ADC and Rate Scalar



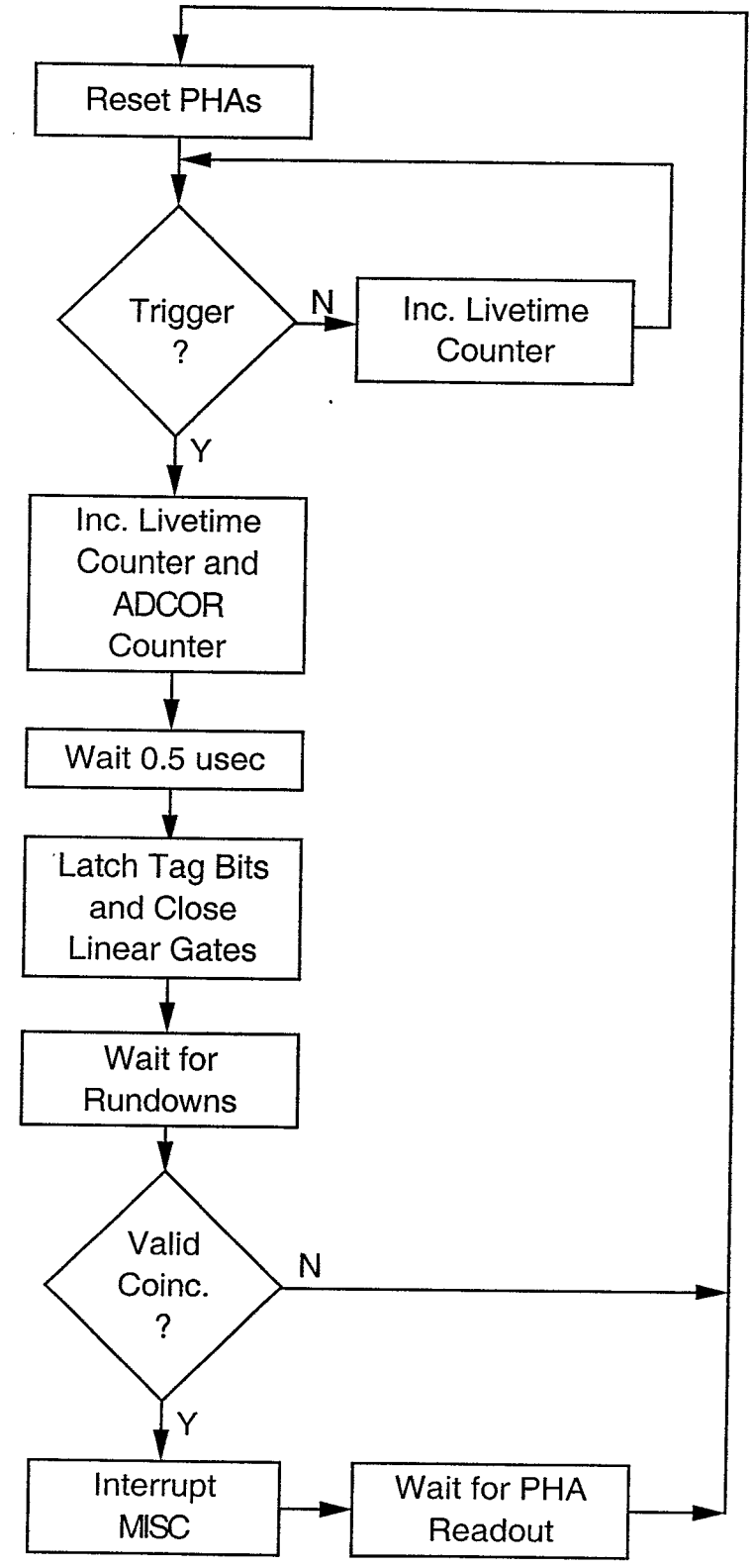
Low Energy Telescope (LET)



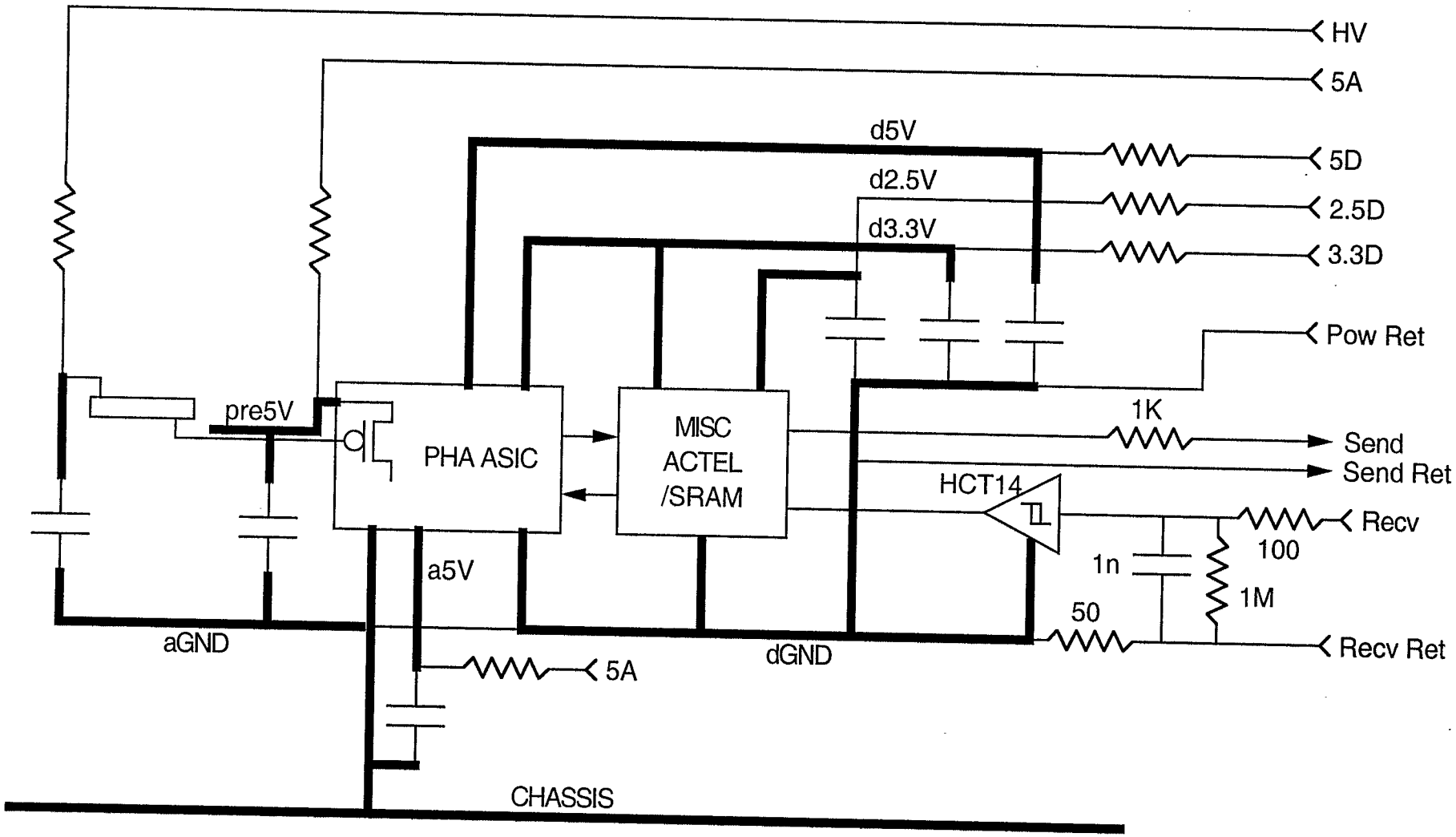
MISC ACTEL for LET



LET Event Controller Flow



LET/HET Grounding/Interface



Electronic Interfaces

1) Plan redundant wire and connector pins on all interface cables, internal and external.

2) Digital interfaces between SEP DPU and HET, LET, SIT, and SEPT are low speed (9600 baud) serial, or low speed pulsed (all 5V single-ended). Formal interface control drawings due Sep. 2001.

3) Signal and power wire count estimates made ---> preliminary connector sizes for harness diagram and weight estimate.

3) Digital interface between SEP DPU and IMPACT DPU defined by preliminary document from Dave Curtis.

4) Open item: Choice of digital interface design for SEPT. Prefer conservative heritage design which avoids coax, but will use same design as for SEP-IMPACT, if needed for EMI reduction.

Common Power/Bias Supplies and Analog Board

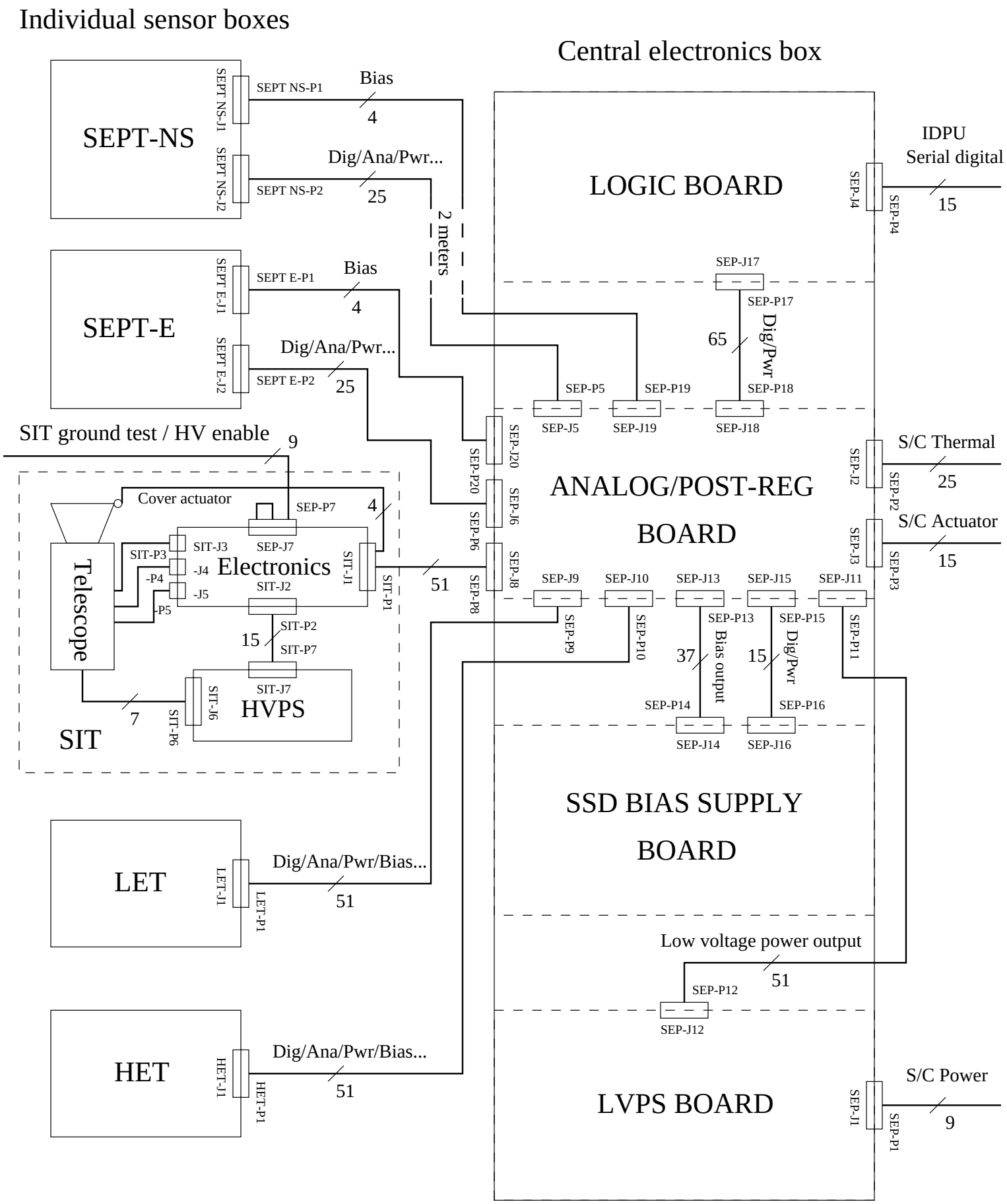
1) Low voltage power supply to be designed and built at Berkeley. List of voltage and current requirements still preliminary. All SEP instruments share power supply voltages, with common on/off command.

2) Critical analog voltages for front-end electronics to be conditioned with series regulators on SEP common analog board.

3) Two detector bias supplies required (used to be 1) for both positive and negative voltages. On/off for each supply commandable via SEP DPU.

4) Detector bias supplies and SEP common analog board to be designed and built by Space Instruments. Sub-contract awaits clarification of the slow ramp requirement for SEPT bias.

5) Analog board will include housekeeping ADC and mux for monitoring of low voltages, bias supply loads and instrument temperatures.



SEP harness schematic

BK 4/19/01

SEP LVPS voltage requirements 4/19/01

Voltage	Type	SEPT	SIT	LET	HET	Central	LVPS out
2.5 V	Digital	X	X	X	X	X	**2.5 V**
3.3 V	Digital		X	X	X	X	**3.3 V**
5.0 V	Digital	X	X			X	**5.0 V**
-5.2 V	Digital		X				**-5.2 V**
12.0 V	Analog		X			X	**13.5 V***
-12.0 V	Analog		X			X	**-13.5 V***
5.0 V	Analog	X	X	X	X	X	**6.5 V***

* A very low head-room (100mV) post-regulator, under development at UCB, will be considered so that these values may decrease significantly.

SEP LVPS power requirements [mW] 4/19/01

Voltage	Type	SEPT	SIT	LET	HET	Central	Totals
2.5 V	Digital	50*	25	43	43	25	**185**
3.3 V	Digital		118	142	142	105	**528**
5.0 V	Digital	345*	266			20	**631**
-5.2 V	Digital		465				**465**
12.0 V	Analog		197			120	**317**
-12.0 V	Analog		56			120	**156**
5.0 V	Analog	605*	248	250	65	180	**1345**
		---	---	---	---	---	---
Instrument subtotals:		**1000**	**1375**	**435**	**250**	**570**	**3630**
LVPS consumption @ ~75% efficiency:							**940**
SEP total consumption:							**4570**

* Estimates based on Phase A report values. An update from SEPT is expected in May 2001.

SEP SSD Bias Supply voltage requirements 4/19/01

Voltage Nominal	Range Min-Max	SEPT	SIT	LET	HET
10V	2 - 30V			L1	
30V	5 - 50V			L2	
250V	50 - 250V			L3	H1-6
150V	150 - 200V		SSD		
-80V	-30 to -80V*	D1-8			
-80V	-30 to -80V*	G1-8			

* Tentative range definition. Expecting an update from SEPT.

SEP SSD Bias Supply open issues 4/19/01

1. Implementation of current limiting on all bias lines.

2. Upper temperature limit assumption for leakage currents.
+40 °C has been recently proposed.

3. Monitoring of voltages and leakage currents.

4. Very slow turn-on/off ramping (~ 1 minute) for the negative supply requested. It's not obvious that it is necessary.

5. Voltage range definition for the negative bias supply for SEPT.

6. Shape, mass and power consumption.

7. Type and location of connectors.

STEREO SEP Flight Software

Personnel and Responsibilities

- **Caltech – LET, SEPT and SEP DPU**
  - Rick Cook, Andrew Davis
- **GSFC – HET and SIT**
  - Don Reames, Kristen Wortman, Bob Baker

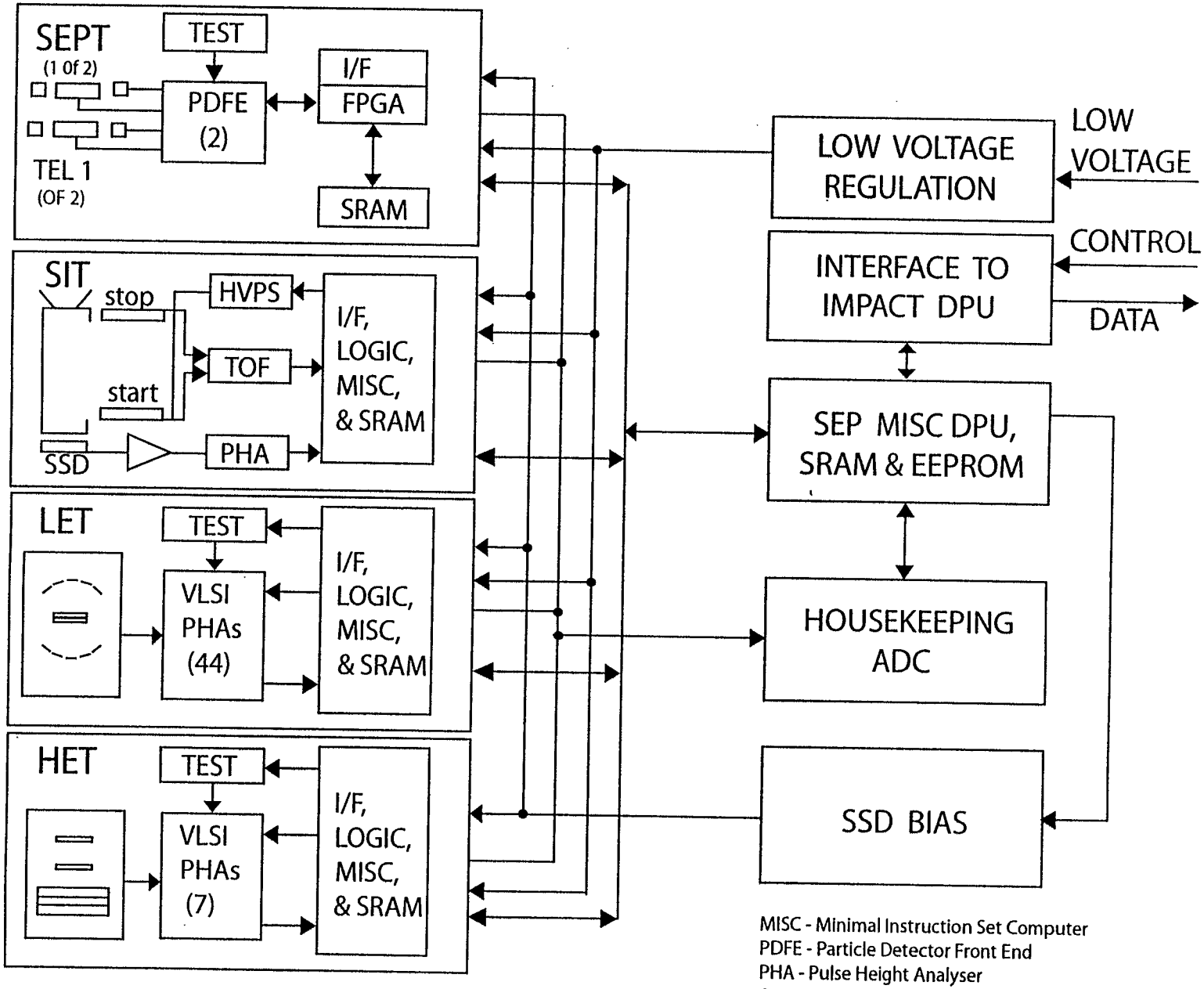
Flight Software Heritage/Experience

- **Caltech – SIS and CRIS instruments on ACE, and balloon instruments**
- **GSFC – EPACT instrument suite on WIND**

SEP Flight Software General Requirements

- **Collect science data from HET, LET, SEPT, SIT**
- **Collect housekeeping data from SEP instruments and other SEP subsystems (power supplies, bias supplies, etc)**
- **Manage setup and mode control of SEP instruments and other SEP subsystems**
- **Interface with IMPACT IDPU**
  - Process commands received through IDPU interface
  - Format SEP science and housekeeping data and send to IDPU

(See SEP block diagram)



MISC - Minimal Instruction Set Computer
PDFE - Particle Detector Front End
PHA - Pulse Height Analyser
SSD - Solid State Detector
TOF - Time of Flight

4-16-2001

Software Design Methodology

Top-Down and Bottom-Up Approaches running in parallel

- **Top-Down**
  1. Requirements definition and analysis
     - Onboard data processing requirements for each instrument
     - Housekeeping data requirements
     - Data formatting requirements
     - IMPACT IDPU interface requirements
  2. Design Phase
  3. Implementation
  4. System testing and acceptance testing
- **Bottom-Up**
  1. Small test routines – gain familiarity with MISC processor
  2. Verify Forth system on MISC with standard software test suite
  3. Prototype onboard processing algorithms to verify feasibility of MISC hardware approach

Development Environment

- Most software development and testing done on engineering test units or flight units using resident Forth system
- Code - a mixture of modular, structured Forth and assembly language
- Full simulation of MISC Forth system is available under Win32Forth
- Assembler for MISC is available under Win32Forth
- Expect a large number of intermediate software builds, tied to the development of the flight hardware

Software Quality Assurance Measures

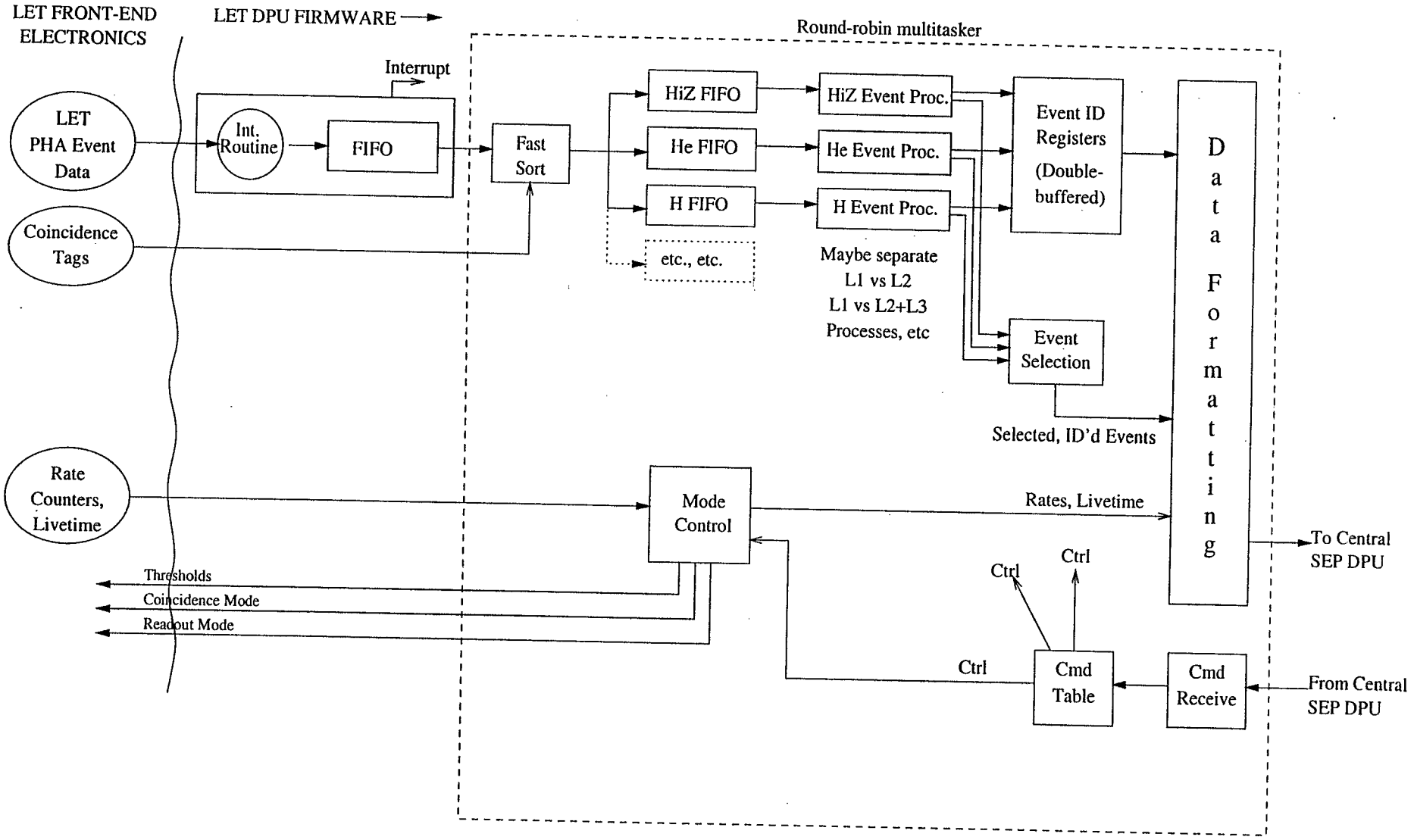
- Version numbering and documentation of changes for all source files
- Daily archiving of all source code
- Formal version control during latter stages of implementation phase
- Software walk-throughs at software peer reviews, reports at PDR and CDR
- System and acceptance tests : end-to-end instrument, electronics, and software functional tests done using accelerator tests, radiation sources, built-in self-test routines and test procedures

Current Status

- **Requirements Definition & Analysis**
  - Currently gathering instrument science data processing and housekeeping data requirements from instrument teams
  - Data format definition is in progress
  - Draft ICD between SEP DPU and IMPACT IDPU is written
- **Preliminary Design**
  - Work begun on design/data flow diagrams (see LET data flow diagram)
  - Work begun on event processing algorithms for LET, HET and SIT

LET Data Flow thru LET MISC DPU

03-27-01

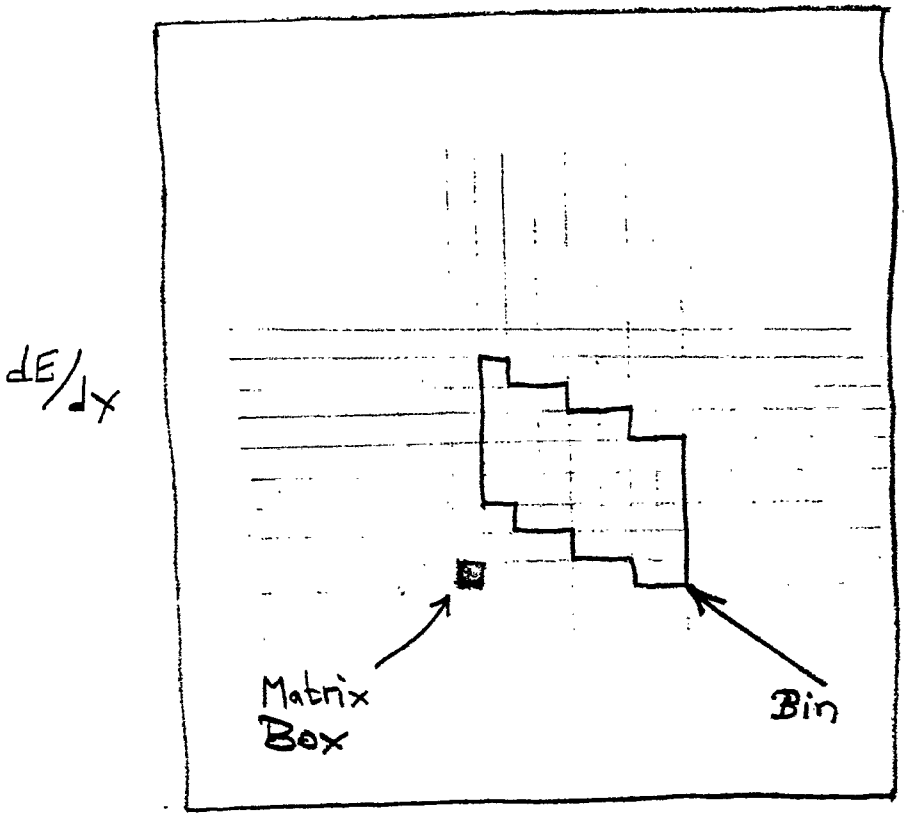


Current Status (2)

- **Prototyping**
  - L1 vs. L2+L3 Event processing algorithm for LET is implemented on the MISC in Forth
  - Same Forth code runs on the Harris RTX 2010, allowing for speed comparisons, and optimization of the MISC Forth system
  - Current version processes 13700 events/sec on MISC running at 10MHz

    (see LET event processing algorithm flow diagram and L1 vs. L2 matrix illustration)
- **MISC Forth System Functional Tests**
  - In progress, using a suite of standard Forth test routines

ILLUSTRATION of ONBOARD BINNING of EVENTS (LET, HET, similar for SIT)



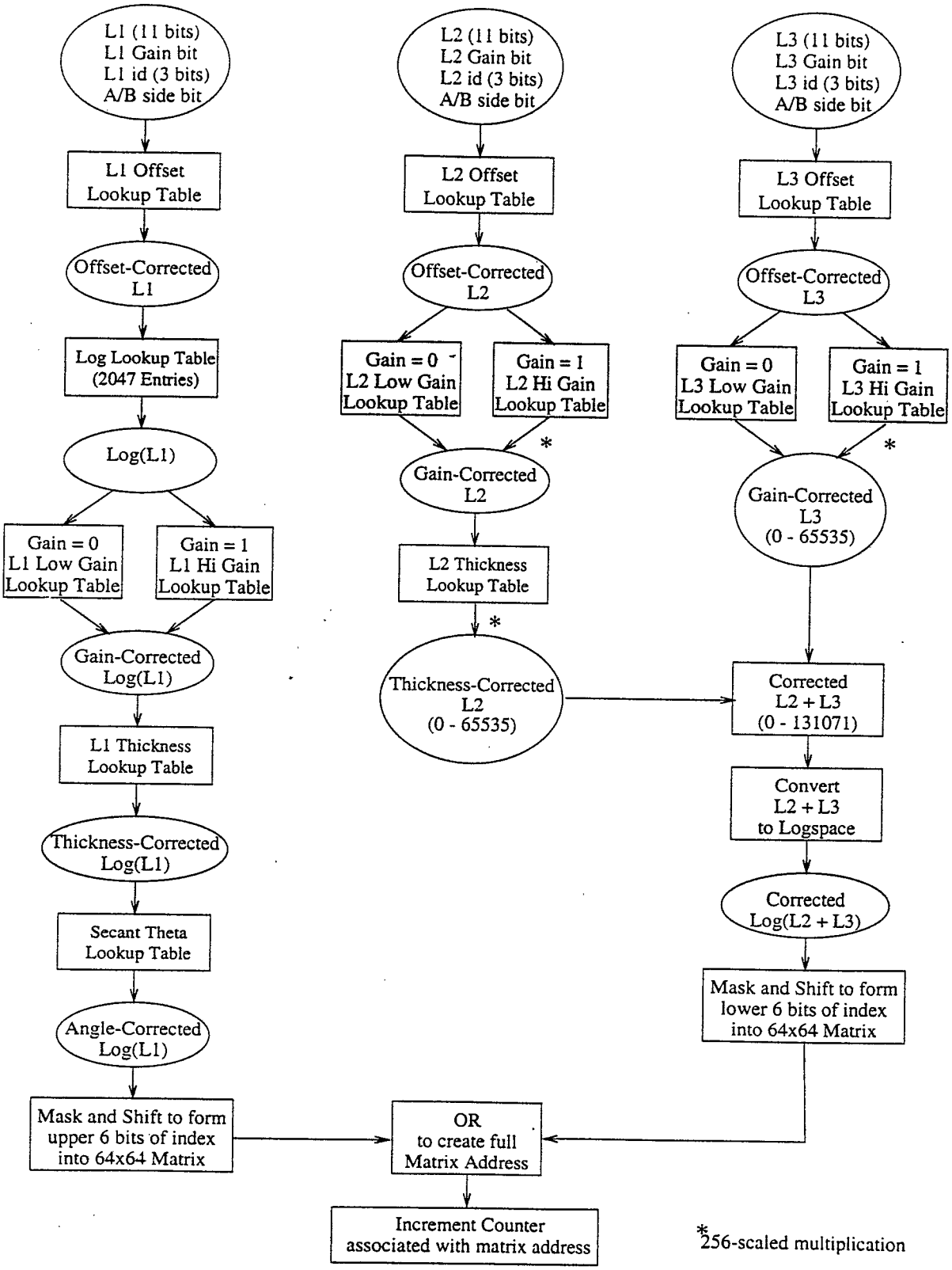
$\log(L1) \propto dE/dx$

$\log(L2+L3) \propto E'$

Any event falling into a matrix box within the larger bin causes a counter associated with the bin to be incremented.

LET L1 vs. (L2+L3) Event Processing

3-24-01



Electronics parts: 1. Reliability

· **Grade 2 parts are required on all STEREO subsystems. The guiding document in parts selection is GSFC 311-INST-001.**

· **GSFC parts specialist, Terry King, is helping us review manufacturers' screening flows and has suggested additional screening steps in order to comply with grade 2 requirement.**

· **Procurement of critical long lead-time parts (Actel FPGA, SRAM, EEPROM, …) as well as up-screening of certain devices will be coordinated with other IMPACT teams.**

· **We also plan on using heritage spare parts from previous missions (ACE, WIND, HESSI, …) upon Terry King's review and approval of the spare parts lists and date codes.**

· **Following are the long-lead items that will be discussed in more detail below:**

2. Actel FPGA

3. 128k x 24 SRAM

4. 128k x 24 EEPROM

Electronics parts: 2. Actel FPGA

High-density device needed for 3 MISCs (in LET/HET/SIT).
Low-density device needed for 1 MISC (in CPU).

Options:	**Actel**	**Actel**
Part number:	**RT54SX32S-208B**	**-72S**
Availability:	**June, 2001**	**January, 2002**
Configuration:	**32,000 gates**	**72,000 gates**
Die/package:	**1 (small)**	**1 (large)**
Core & I/O voltage:	**2.5 & 2.5/3.3/5 V**	**Same**
Rad-hardness:	**50 krad expected**	**Same expected**
Total dose test report due on 4/24/01.		
Latch-up:	**104 MeV/mg/cm^2**	**Same expected**
SEU rate:	**< 1 x 10^{-10} upsets/bit-day**	**Same expected**
Class:	**B**	**B**
Cost:	**$3120/ea**	**$4400/ea**
Delivery:	**12-18 weeks**	**Same expected**
Qty for flight:	**4 or 16 (2/MISC)**	**6 (1/MISC)**
Grade 2 adder:	**100% PIND test ($50/ea & 1-2 wks extra)**	

Electronics parts: 3. 128k x 24 SRAM

Low-power part needed for 4 MISCs (in LET/HET/SIT/CPU).

Options:	**Lockheed Martin**	**Honeywell**
Part number:	**238A792-modified**	**HLX6228**
Configuration:	**128k x 24**	**128k x 8**
Die/package:	**3**	**1**
Voltage:	**3.3 V (or 5 V)**	**3.3 V (or 5 V)**
Power:	**17 mW/MHz/die**	**9 mW/MHz**
Rad-hardness:	**1 Mrad**	**100 krad**
Latch-up:	**Immune**	**Immune**
SEU rate:	**< 1 x 10^{-10} upsets/bit-day**	**Same**
Class:	**QML H**	**B**
Cost:	**$5200/ea – Flt** **$2700/ea – EM**	**$2070/ea – Flt** **$1610/ea – EM**
Delivery:	**12 weeks - Flt** **4 weeks - EM**	**20 weeks - Flt** **18 weeks - EM**
Qty for flight:	**8 (1/MISC)**	**24 (3/MISC)**
Grade 2 adder:	**Screen flow under review for both devices**	

Electronics parts: 4. 128k x 24 EEPROM

Suitable device needed for 1 MISC (in CPU).

Options:	**Austin Semicond.**	**Space Electr.**
Part number:	**AS8ER128K32-mod**	**28LV010RP**
Configuration:	**128k x 8 (or x 32)**	**128k x 8**
Die/package:	**1–4 (Hitachi)**	**1 (Hitachi)**
Voltage:	**5 V**	**3.3 V (or 5 V)**
Power:	**N/A**	**20 mW/MHz**
Rad-hardness:	**40-100 krad**	**100 krad**
Latch-up:	**> 120 MeV/mg/cm^2**	**Same**
SEU$_{TH}$LET:	**> 90 MeV/mg/cm^2**	**Same**
Class:	**QML Q (or H)**	**P (NASA/PPL)**
Cost:	**$600/ea – Monolithic** **$1800/ea – MCM** **$TBD/ea – EM**	**$1250/ea – Flt** **$385/ea – EM**
Delivery:	**16-20 weeks - Mono** **20-22 weeks - MCM**	**18 weeks - Flt** **6-8 weeks - EM**
Qty for flight:	**6 monolith. or 2 MCM**	**6 (3/MISC)**
Grade 2 adder:	**Screen flow under review for both devices**	

SEP resources: Mass [g] 4/19/01

Component	Update	Phase A	Diff.
SIT sensor & door	500	480	20
SIT elec. boards & wiring	370	290	80
SIT HVPS	160	160	0
SIT subtotal:	1030	930	100
SEPT-NS (w/o harness)	520	440	80
SEPT-E (w/ 10cm harness)	540	460	80
SEPT subtotal:	1060	900	160
LET det. & housing	515	390	125
LET electronics	235	120	115
LET subtotal:	750	510	240
HET det. & housing	460	610	-150
HET electronics	160	90	70
HET subtotal:	620	700	-80
Cent. elec. encl. & hdwr	1030	750	280
El. boards, shields, harness	1090	940	150
Cent. elec. subtotal	2120	1690	430
SIT encl. & hdwr	200	N/A	200
SEPT-NS bracket	270	200	70
LET bracket	600	N/A	600
SEP bracket	N/A	1000	-1000
SEP total:	**6650**	**5930**	**720**
SEPT-NS harness (2m)	150	150	0
Thermal blankets	100	N/I	100

SEP resources: Power [mW] 4/19/01

Component	Update	Phase A	Diff.
SIT basic	575	660	-85
CFD (from STEP)	610	N/A	610
MISC @ 4 MHz	190	N/A	190
SIT subtotal:	1375	660	715
SEPT	1000	1040	-40
LET VLSI	250	180*	70
MISC @ 8 MHz	185	N/A	185
LET subtotal:	435	180*	255
HET VLSI	65	70*	-5
MISC @ 8 MHz	185	N/A	185
HET subtotal:	250	70*	180
Central electronics:			
Analog/Post-reg	240	210	30
Logic (MISC & oscill.)	150	500	-350
SSD bias supply	180	140	40
LVPS (75% efficient)	940	700	240
Cent. elec. subtotal:	1510	1550	-40
SEP total:	**4570**	**3500**	**1070**

N/A – Not applicable
* - Including Actels

SEP resources: Data rate [bit/s] 4/19/01

Component	Update	Phase A	Diff.
SIT	240	240	0
SEPT	60	120	-60
LET	320	320	0
HET	120	120	0
Central electronics	0	0	0
----------	------	------	------
SEP total:	**740**	**800**	**-60**

Telescope Integration/Test/Calibration With SEP - Phase 1

SEP GSE Duties:

A. No commanding.
B. Log all data to disk.
C. Display telemetry for SEP, SEPT, SIT, LET, HET.
D. Socket server for telemetry fanout to optional telescope GSEs.

SEP Development System Duties:

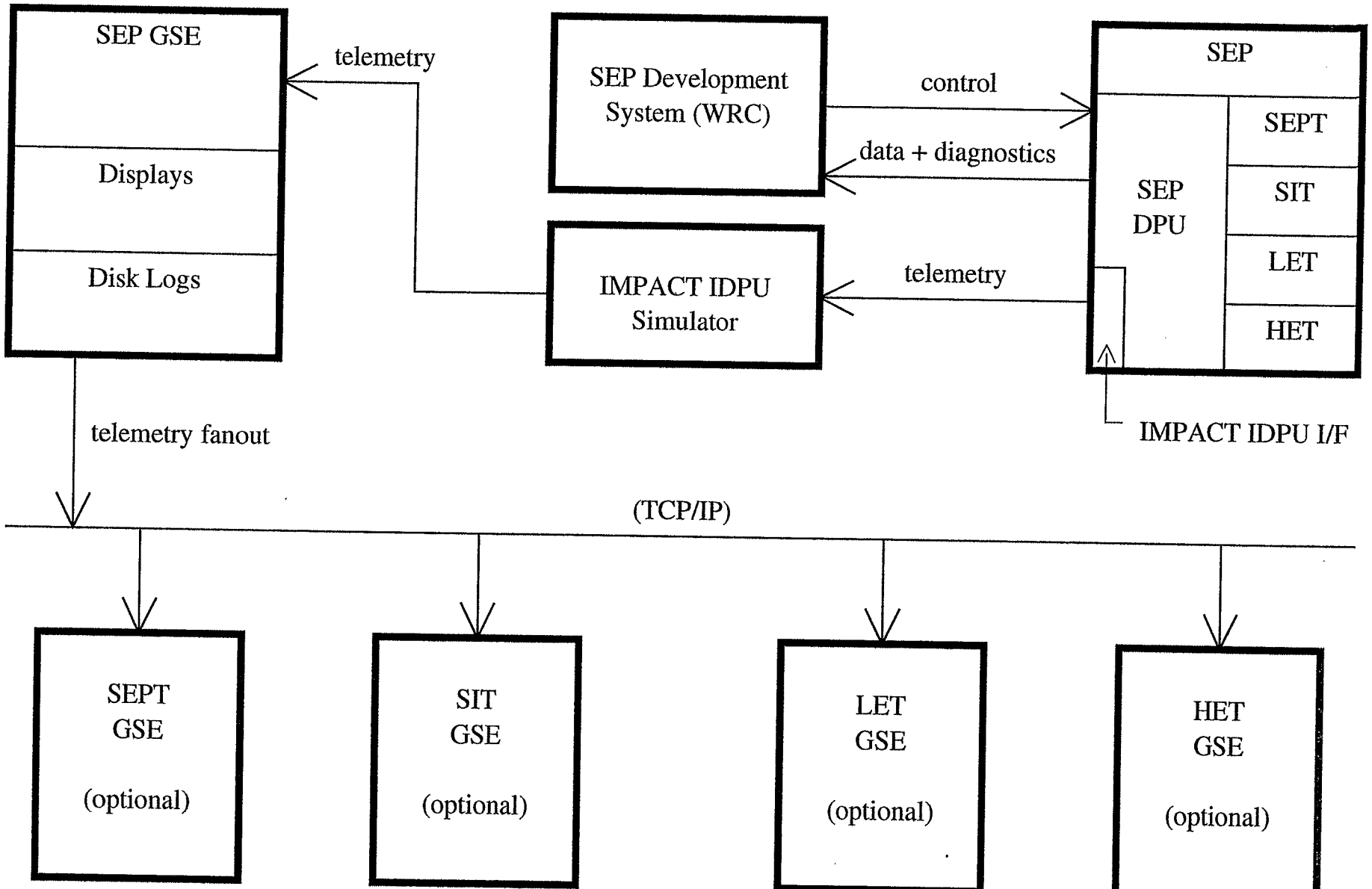
A. Load firmware.
    1. test
    2. calibration
    3. flight
B. Send commands to SEP.
C. Run Diagnostics.

Notes:

1. Telemetry may be faster than normal.
2. Telmetry may not be in normal telemetry format.

19-April-2001 SEP GSE

Telescope Integration/Test/Calibration With SEP - Phase 1



19-April-2001 SEP GSE

Telescope Integration/Test/Calibration With SEP - Phase 2

SEP GSE Duties:

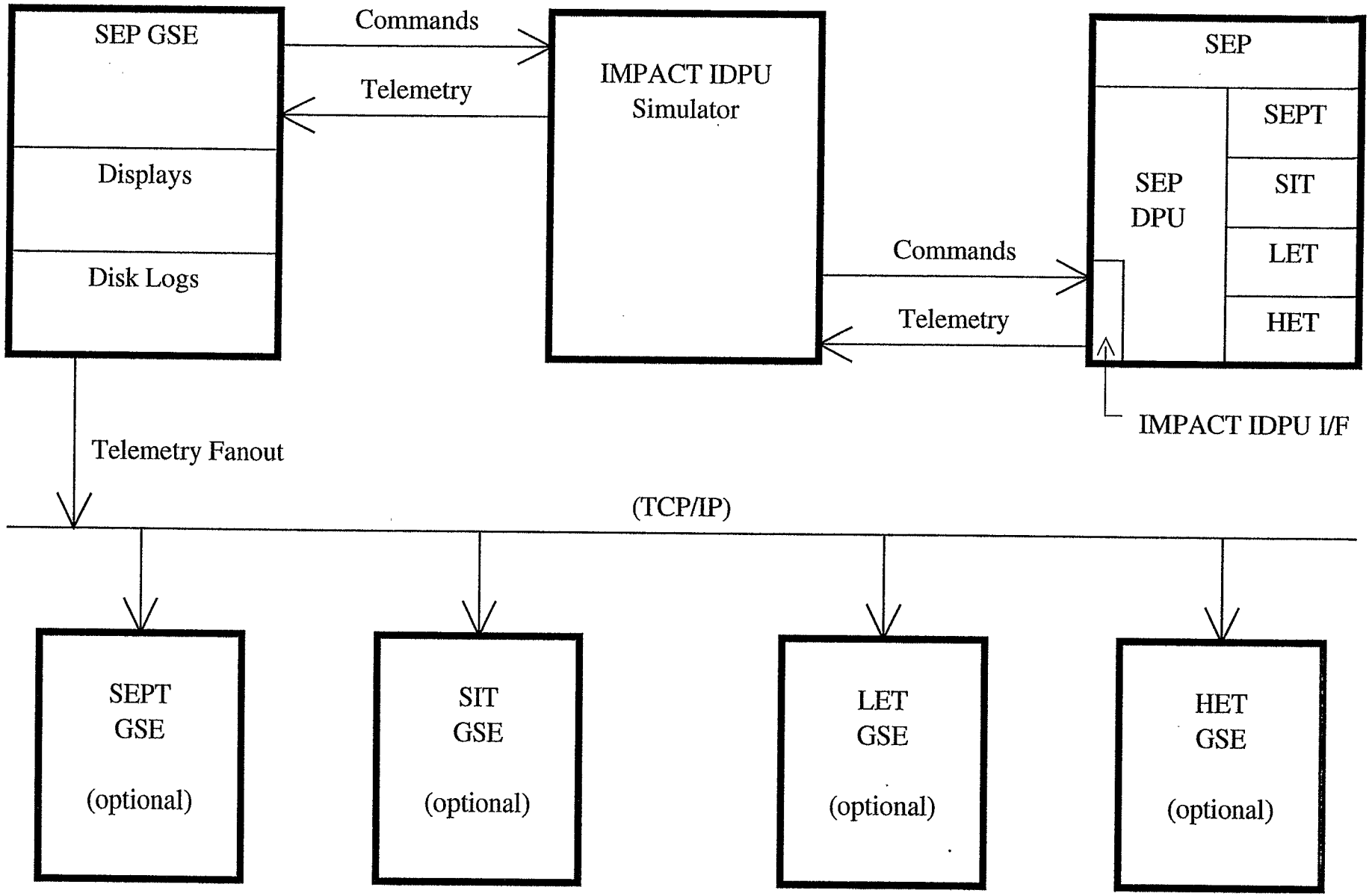
A. Communicate with IMPACT IDPU simulator thru parallel port.
B. Send SEP commands via IMPACT IDPU simulator in IMPACT IDPU format.
C. Log all telemetry to disk.
D. Display telemetry for SEP, SEPT, SIT, LET, HET.
E. Socket server for fanout to optional telescope GSEs.
F. Upload firmware?

Notes:

1. Expecting telemetry in normal SEP packets.
2. Need policy for command verification.

19-April-2001 SEP GSE

Telescope Integration/Test/Calibration With SEP - Phase 2



19-April-2001 SEP GSE

Post SEP Delivery

SEP GSE Duties:

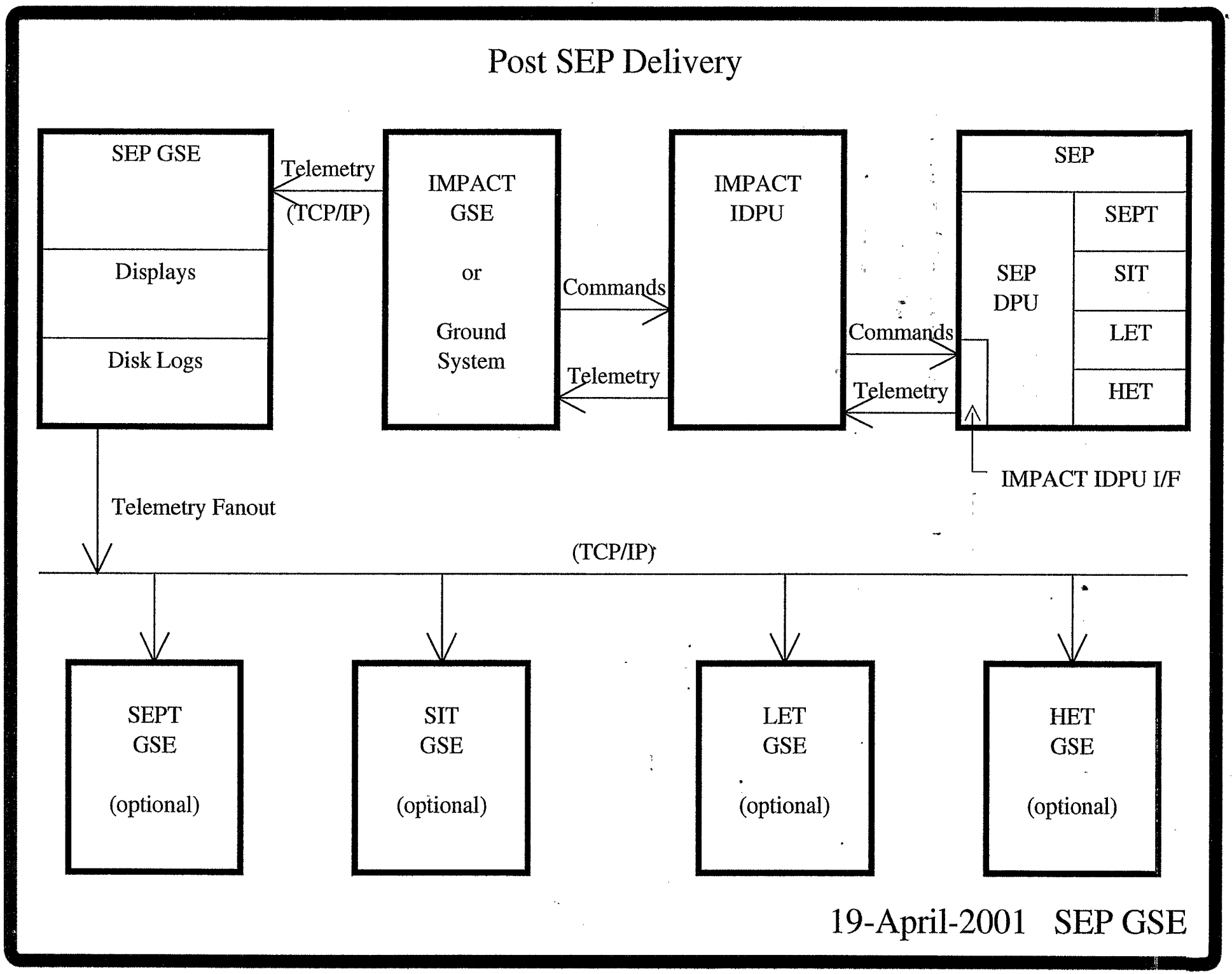
A. No commanding.
B. Connect to IMPACT GSE or ground system thru TCP/IP socket.
C. Log all telemetry to disk.
D. Display telemetry for SEP, SEPT, SIT, LET, HET.
E. Socket server for fanout to optional telescope GSEs.

Notes:

1. Expecting telemetry in the form of

   a. SEP packets,
   b. IMPACT packets, or
   c. S/C packets.

2. Fanout telemetry will be converted to normal SEP packets.


Post SEP Delivery
SEP GSE
Displays
Disk Logs
Telemetry
(TCP/IP)
IMPACT
GSE
or
Ground
System
Commands
Telemetry
IMPACT
IDPU
Commands
Telemetry
SEP
SEP
DPU
SEPT
SIT
LET
HET
IMPACT IDPU I/F
Telemetry Fanout
(TCP/IP)
SEPT
GSE
(optional)
SIT
GSE
(optional)
LET
GSE
(optional)
HET
GSE
(optional)
19-April-2001 SEP GSE

Introduction

- SEPT has 4 PDFE's (Particle Detector Front End ASIC)
- They are under full control of one SEPT-FPGA (SEPTIC, Actel 54SX32).
- Set-up, Commanding and Data collection of SEPT is done via bi-directional serial interface (SEP/DPU - SEPT) with 9600 bps (TBC).

Set-up

- SEPT needs several parameters after start-up from SEP/DPU:
  - PDFE chips set-up
  - choice of operational modes
  - internal parameters

- FPGA has many different parameters and modes to choose (see: *Solar Electron and Proton Telecope Integrated Circuit (SEPTIC) data sheet*)

- SEPT team will provide a **list of control strings** (concatenated commands, parameters, etc.) for different scenarios to control SEPT to ease the operation and reduce complexity of SEP software.

- SEPT has no default internal set-up and must hence be **set-up after each power-up** and **after each internal latch-up reset** from SEP-DPU.

Commanding

- SEPT needs commanding from SEP-DPU after set-up

nominal operation scenario:

1. Set up desired mode per command string and start data SEPT internal data acquisition.
2. Send command to collect data (compressed spectrum) after 1 minute and transfer data to telemetry.
3. Repeat step 2 forever
4. break step 3 if mode change request occurs or latch up happens
   -> step 1.

Note: SEPT has a interrupt line to SEP-DPU for notification of exceptions (like latch-up)

Data transfer

- Data transfer from SEP to SEPT will occur only after proper set-up and specific command to read out data.
- No SEPT data transfer occurs without SEP-commanding.
- Commands received by SEPT will be echoed to SEP (= life test of connection).
- SEPT will reply data in predefined size and format
- **Reply data types**:

- Echos of commands
- Science Data
- Housekeeping and
- Test Data

Latch-Up / Reset

- After latch-up detection (detected by SEPT internal monitor) SEPT-FPGA will break supply lines of analog part and set all internal control lines to tri-state to get rid of any voltage on analog board.

- SEP/DPU will receive notification via Interrupt line.

- Serial interface SEPT-SEP will still operate during latch-up reset.

- After TBD seconds SEPT unit has to be set-up again from SEP/DPU (with latest set-up commands) and data acquisition can be started again.

Housekeeping Data

- SEPT provides several housekeeping data (leakage currents, temperature, parameters, etc) on request in predefined format.
- Commands have to be sent from SEP/DPU to SEPT for acquisition and readout of housekeeping data.
- No housekeeping data will be collected or transferred without command.

Ground Testing / In-Flight Testing

- A wide range of commands is foreseen for testing of SEPT unit during different instrument integration levels and during flight.
- SEP/DPU has to send commands for testing to SEPT. No test will occur without command from SEP/DPU.
- Predefined command sequences will be provided for testing of SEPT.
- In-Flight “calibration” can be done by means of SEPT internal test generator. Operation has to be controlled from SEP/DPU. Test data must be collected (after read out command) and transferred to telemetry.
- Possibility of through passing of command from GSE to SEPT via SEP/DPU should be provided.

Summary

- SEPT unit has only low level intelligence and needs to be set-up and controlled from SEP/DPU.
- Commands have to be sent from SEP/DPU to SEPT for acquisition and readout of any kind of data.
- SEP/DPU has to provide operation (including test) scenario by sending of appropriate commands at appropriate time.
- SEPT will provide all data in simple predefined format. SEP/DPU is requested to convert data into telemetry format.
- SEPT will do **nothing** without command from SEP/DPU.