SIT Stuff for SEP Peer Review

19 Apr 2001

Telescope

- TOF vs E
- FOV
- Energy 1 SSD
 - surface barrier or ion implant
 - 15mm x 40 mm
 - 500u
- TOF 1 START & 1 STOP
 - 10 cm flight path
 - chevron pair micro-channel plates
 - 1000v bias per plate, commandable
- Foils 2
 - Ni
 - -1000Å, on grid

Suprathermal Ion Telescope (SIT)



SIT Telescope Cross Section



BLOCK DIAGRAMS

SIT - Box-Level Block Diagram



SIT BLOCK DIAGRAM



SEP Peer Review 4/01

7/17/2001

SIT FUNCTIONAL BLOCK DIAGRAM



SIT ENERGY SYSTEM BLOCK DIAGRAM



SIT TOF BLOCK DIAGRAM



(Put TOF Schematics Here) - TOF amplifier - TOF CFD



TOF DIGITAL BLOCK DIAGRAM



Front-End Logic Tasks

- Collect Events and present them to MISC
- Receive Commands from MISC and Execute them
 - VLSI initialization and control
 - HV control (Digital to Analog conversion)
- Provide 10MHz clock for TOF Circuit







SIT Event Pre-Processing in Front-End Logic

MISC Tasks

- Initialization of Self and VLSI
 - Power-on reset
 - External reset from SEP CPU
 - Watchdog timer?
- Event Processing
 - Event binning/matrix rate counting
 - Event prioritization and storage
- TOF Calibration
- Singles Rate Collection (counting done in TOF)
- Command Processing
- Output data Formatting and Transmitting
 - rate compression
 - buffer management
 - output data to SEP CPU





HVPS

- Provides bias voltages to operate the microchannel plates and to "focus" the secondary electrons produced by incoming ions
- Nominal voltages: 3400,3200,2200,2000,1000 and 950 v
- Top voltage controlled by command, others change proportionally
- 0-5v control voltage
- Maximum output ~4200v
- On/Off Command : 5v level
- Disable plug to prevent operation during ground testing
- Operates on +/- 12v
- Supplied in housing by UCB

Board Outlines















SIT Electronics Assembly



MOTHER BOARD

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~ 3.2 cm



Output Data

- PHA Events 24 bits
 - Energy 11 bits + ramp bit
 - TOF 8 bits
 - Misc 4 bits
- Singles Rates
- Matrix Rates
 - Low time resolution
 - High Time resolution
- Housekeeping
- Status (?)

Output Data Format

• TBD

Bit rates

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Commissioning

- Turn ON LV with all of SEP shortly after launch
- Open acoustic cover TBD
 - soon to prevent sticking
 - late enough to avoid major periods (> few seconds) of sun in FOV
- Put in Science Mode turn on and ramp up HV
 - conducted over several (e.g. 5) days
 - requires commanding and data viewing during real-time pass each day
- Verify Proper Operation observe/process science data

Commanding

- Commissioning Phase
 - Power, cover, HV commands several commands/day, several days
 - Verification of Operation few tens of commands
 - Possible table upload to correct problems
- Science Mode
 - Possibly a few commands/week to calibrate sensor
 - No other periodic commands required
 - Rarely a table upload to compensate for gain drifts or other problems

Purging

- Clean dry (bottled) GN2 will be used to purge SIT telescope during integration and test at UMd
- Continuous N2 purge of telescope required during instrument testing on bench and on S/C (with obvious exceptions for environmental tests).
- Purge on pad?
- SIT will be connected to SEP purge manifold and will purge at same time as rest of SEP.
- Flow rate TBD but ~ 0.5 SCFH, Pressure TBD
- Special filters for particulates?
 - Not required for SIT but necessary to meet cleanliness?

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PROTOTYPE UNIT

	TASK	UMD	GSFC	CIT	UCB	MPAe
Prototype						
	Assemble Prototype Telescope		Х			
	Test Prototype Telescope	Х				
	Modify TOF Amp/Disc Design	Х				
	Build/test prototype analog TOF board	Х				
	Deliver Prototype Digital TOF system					Х
	Integrate Analog and Digital TOF boards	Х				
	Test Prototype TOF System	Х				
	Charge Amp Design	Х				
	Provide "Data Sheet" for VLSI			Х		
	Assist Design to I/F CSA to VLSI			Х		
	Outline SIT Logic Requirements	Х				
	Detailed Front-end Logic Design		Х			
	Prototype ACTEL Design		Х			
	Specify CPU I/F requirements			Х		
	Prototype MISC Design		Х	Х		
	Procure prototype MISC parts (ACTEL,RAM)		Х	Х		
	Generate data processing algorithms	Х				
	Prototype MISC firmware		Х			
	Design/Procure Prototype Energy PCB	Х				
	Provide Prototype VLSI			Х		
	Provide ACTEL Socket			Х		
	Provide Other Proto E parts	Х				
	Stuff Prototype Energy/Logic/MISC Board		Х			
	Test Prototype Energy Board	Х				
	Deliver prototype HVPS to UMD				Х	
	Test Prototype HVPS	Х				
	Test Harness design/build/test	Х				
	-					
	Assemble/Test SIT Prototype	Х				

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FLIGHT MODEL UNIT 1

FM1 Procure SSD/MCP/Foils X X Design/Build Sunshade/Cover X X Build FM1 Telescope X X Test FM1 Telescope X X Generate TOF analog board parts list X X Procure TOF analog board parts X X Layout flight TOF analog board X X Assemble FM1 TOF analog board X X Assemble FM1 TOF analog board X X Deliver FM1 TOF analog board X X Deliver FM1 TOF analog board X X Deliver FM1 TOF analog board X X Procure flight Energy PCB X X Procure flight Energy PCB X X Procure flight Font-end logic X X Deliver flight front-end logic X X Design flight front-end logic ACTEL X X Make flight front-end logic ACTEL X X Design flight SACTEL X X Design flight MISC ACTEL X X Assemble FM1 energy board X X <th></th> <th>TASK</th> <th>UMD</th> <th>GSFC</th> <th>CIT</th> <th>UCB</th> <th>MPAe</th>		TASK	UMD	GSFC	CIT	UCB	MPAe
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Test FM1 motherboard X		Assemble FM1 motherboard		Х			
		Test FM1 motherboard	Х				
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Post-coat assy & test X		Post-coat assy & test	Х				

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FLIGHT MODEL UNIT 2

	TASK	UMD	GSFC	СІТ	UCB	MPAe
FM2						
	Build FM2 Telescope		Х			
	Test FM2 Telescope	Х				
	Assemble FM2 TOF analog board		Х			
	Test FM2 TOF analog board	Х				
	Deliver FM2 TOF digital board					Х
	Integrate FM2 TOF A and D boards	Х				
	Test FM2 TOF	Х				
	Assemble FM2 energy board		Х			
	Test FM2 energy board	Х				
	Deliver FM2 HVPS to UMD				Х	
	Test FM2 HVPS	Х				
	Assemble FM2 motherboard		Х			
	Test FM2 motherboard	Х				
	Assemble and Test FM2 unit	Х				
	Conformal coat E, Logic and MB		Х			
	Post-coat assy & test	Х				
	Deliver FM1 and FM2 to Caltech	Х				
GSE						
	CPU Simulator	Х				
	SIT Stimulus Unit	Х				