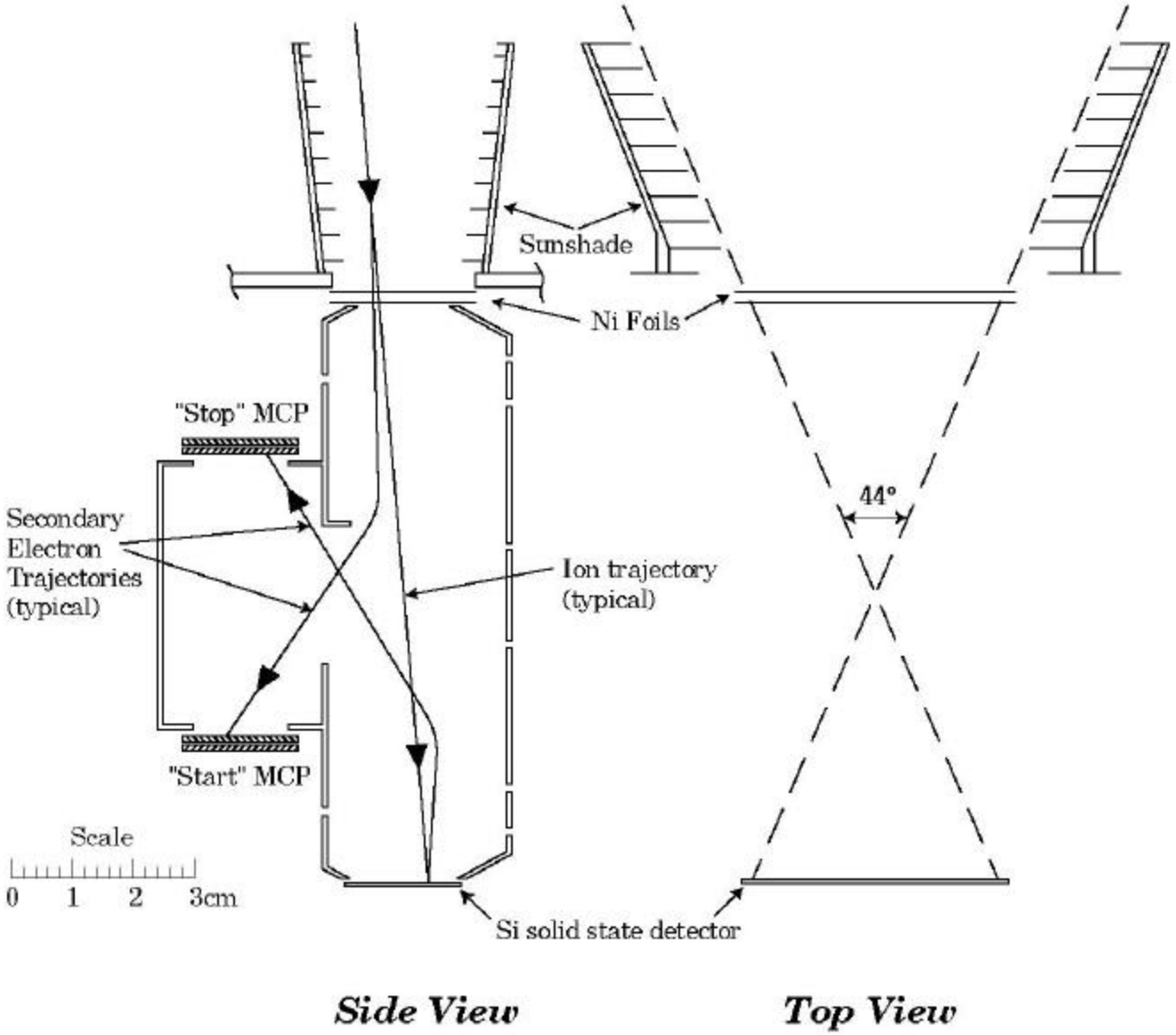
SIT Stuff for SEP Peer Review

19 Apr 2001

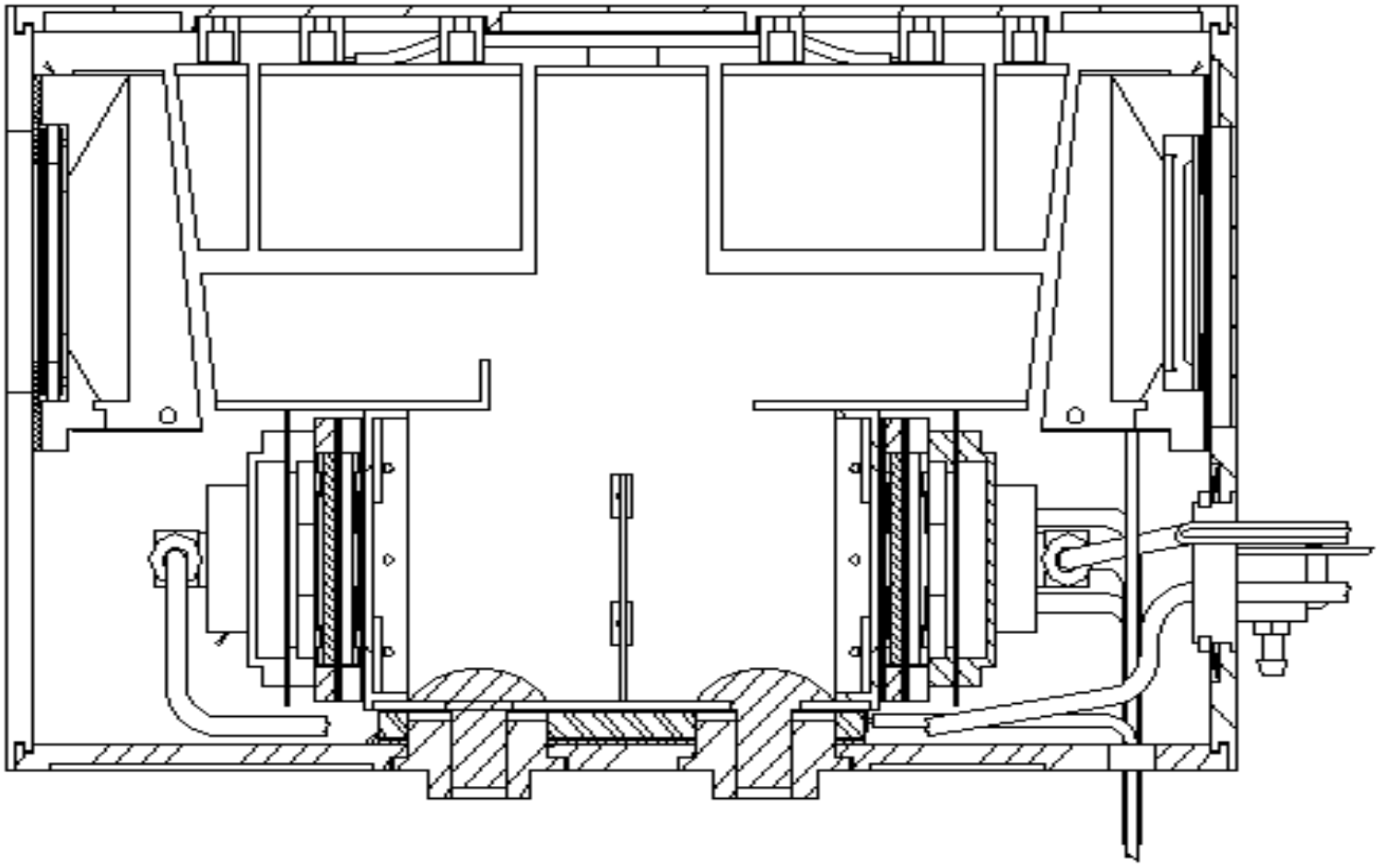
Telescope

- TOF vs E
- FOV
- Energy - 1 SSD
  - surface barrier or ion implant
  - 15mm x 40 mm
  - 500u
- TOF - 1 START & 1 STOP
  - 10 cm flight path
  - chevron pair micro-channel plates
  - 1000v bias per plate, commandable
- Foils - 2
  - Ni
  - 1000Å, on grid

Suprathermal Ion Telescope (SIT)

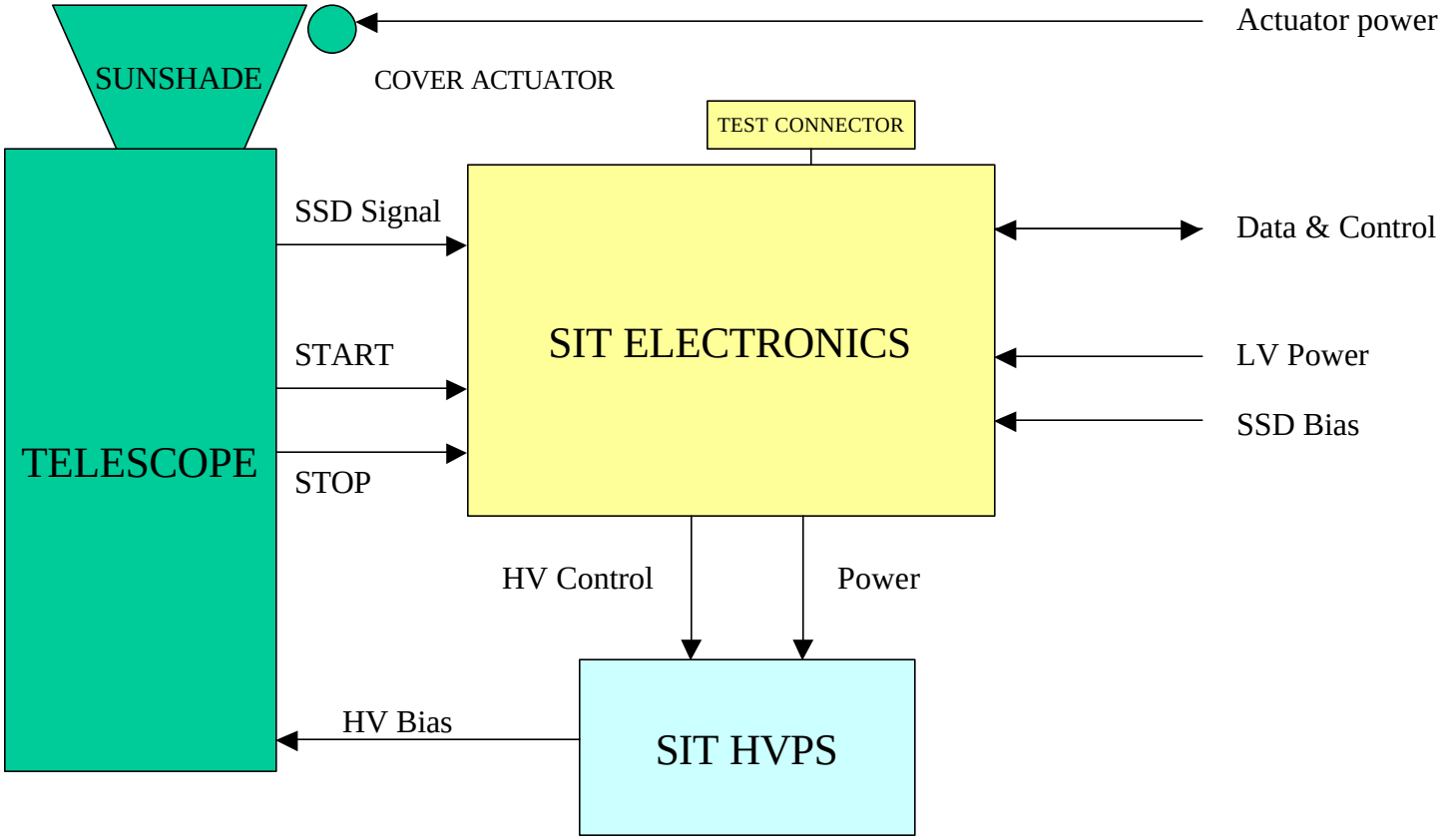


SIT Telescope Cross Section

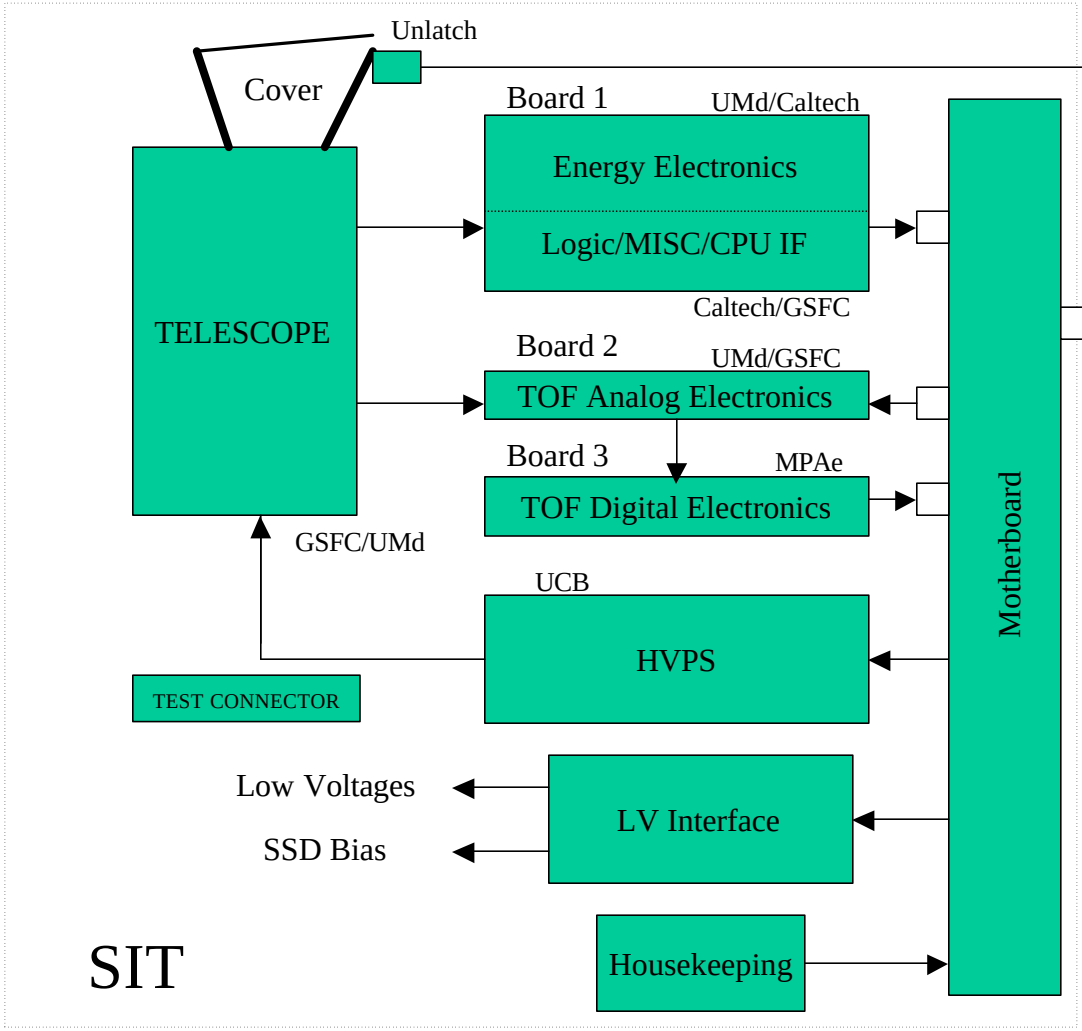


BLOCK DIAGRAMS

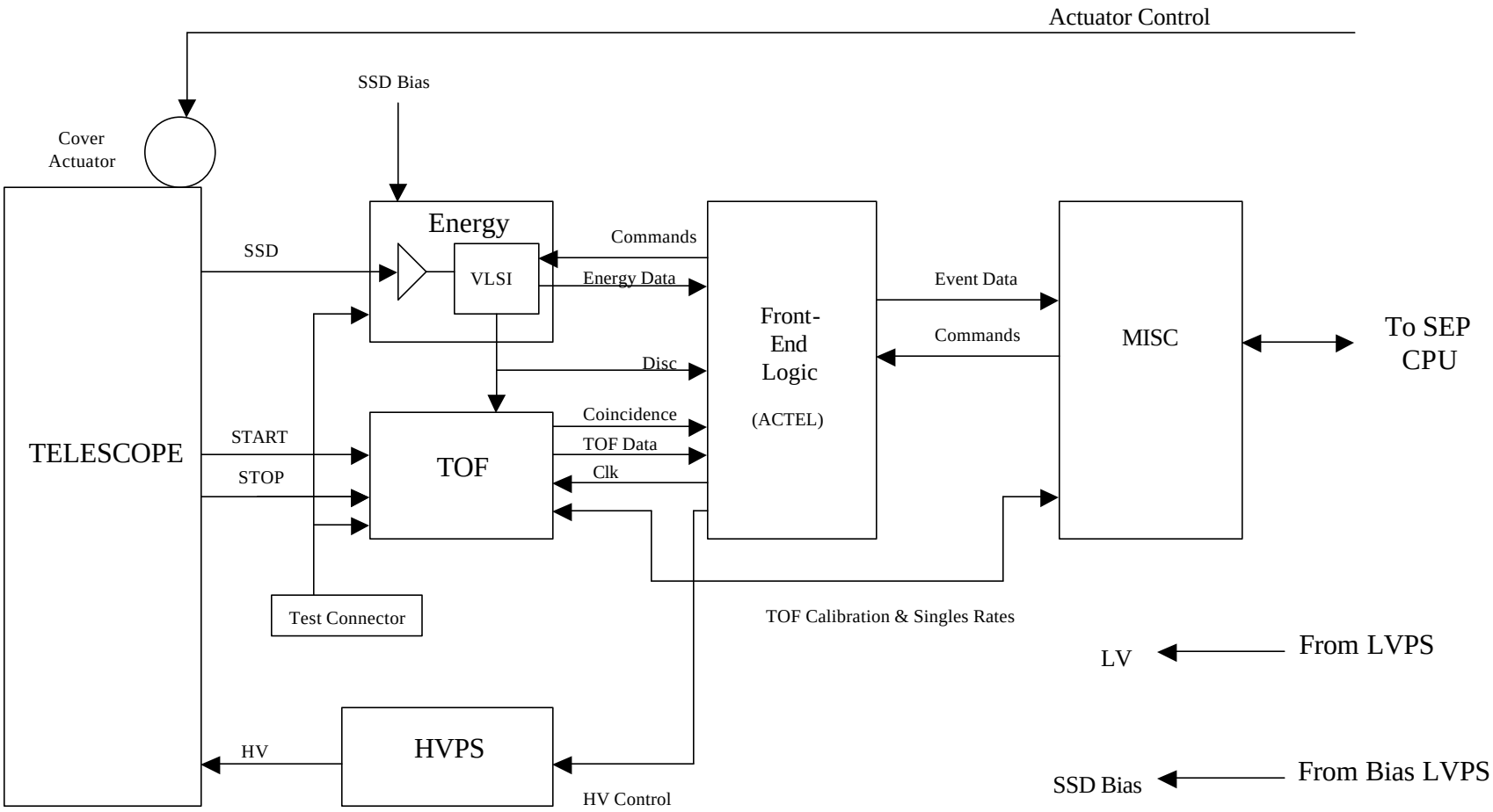
SIT - Box-Level Block Diagram



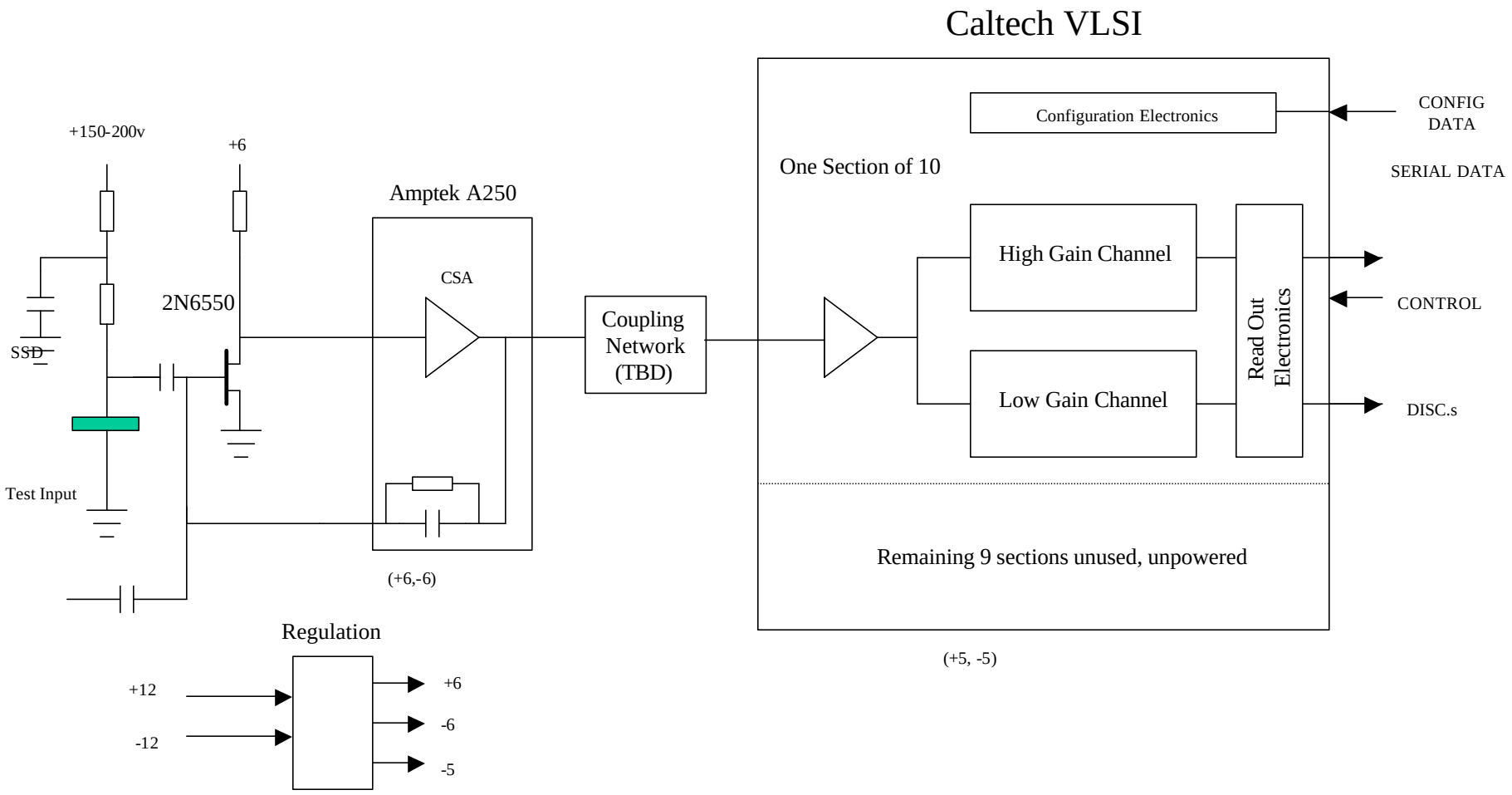
SIT BLOCK DIAGRAM



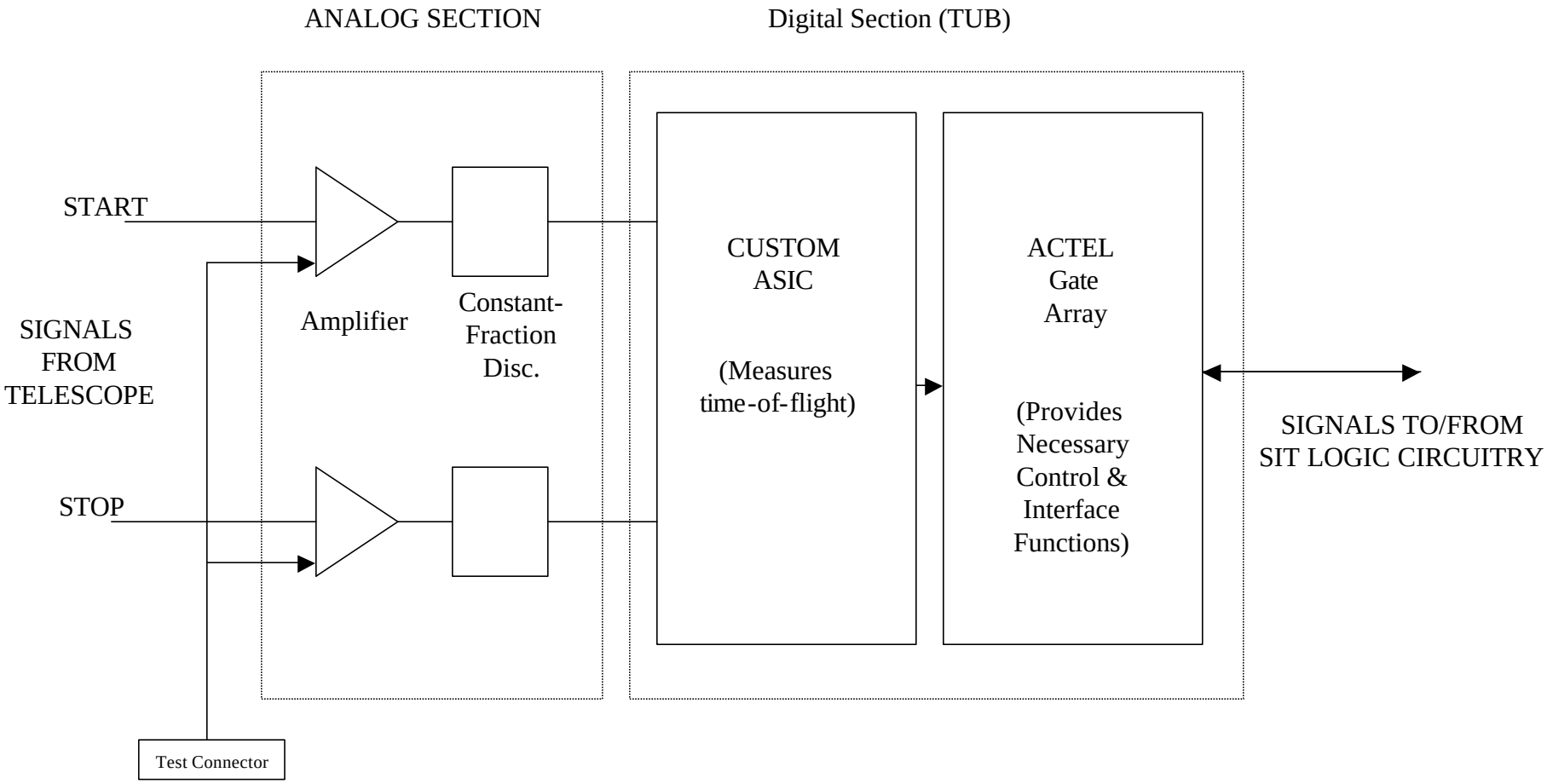
SIT FUNCTIONAL BLOCK DIAGRAM



SIT ENERGY SYSTEM BLOCK DIAGRAM

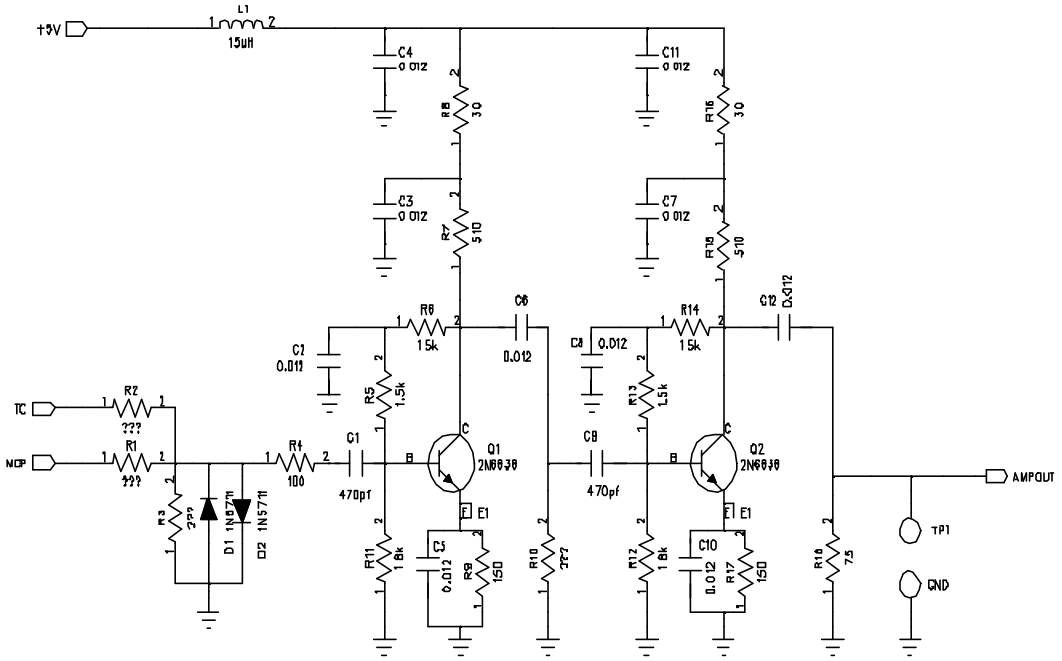


SIT TOF BLOCK DIAGRAM



(Put TOF Schematics Here)
- TOF amplifier
- TOF CFD

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN.	DATED.
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED.	DATED.

COMPANY. UNIVERSITY of MARYLAND

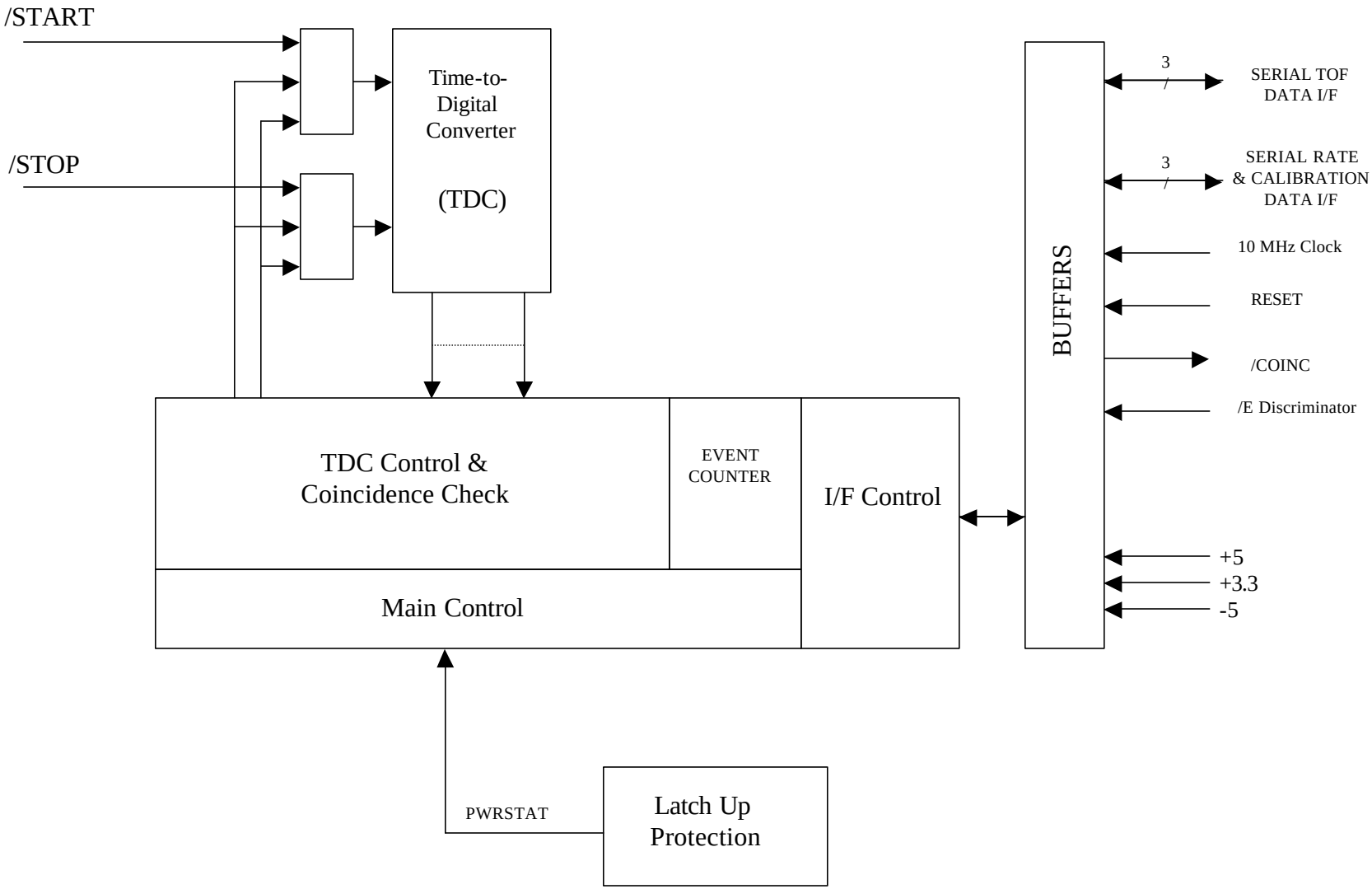
TITLE

SIT TOF AMPLIFIER

CODE.	SIZE:	DRAWING NO:	REV.

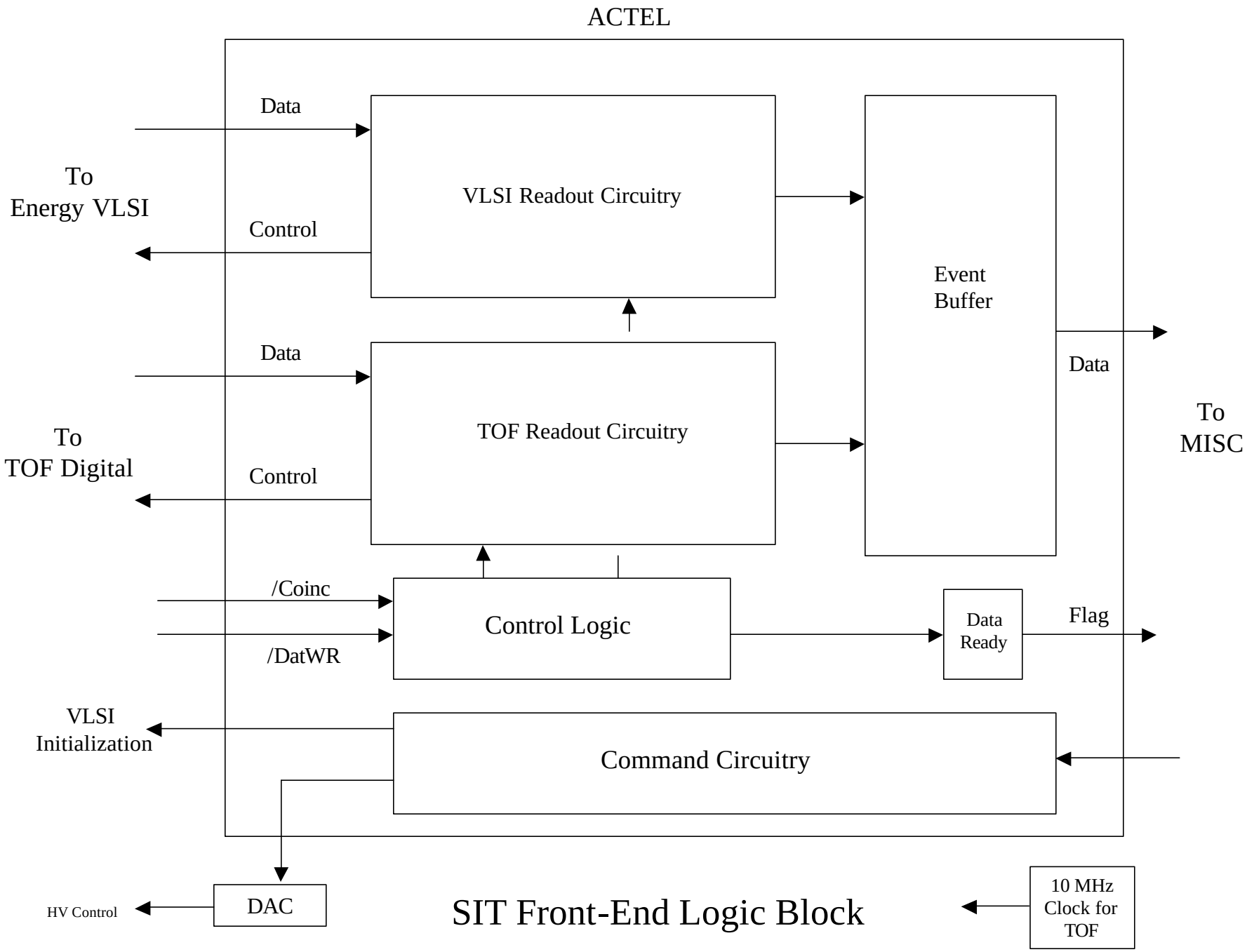
SCALE: SHEET: OF

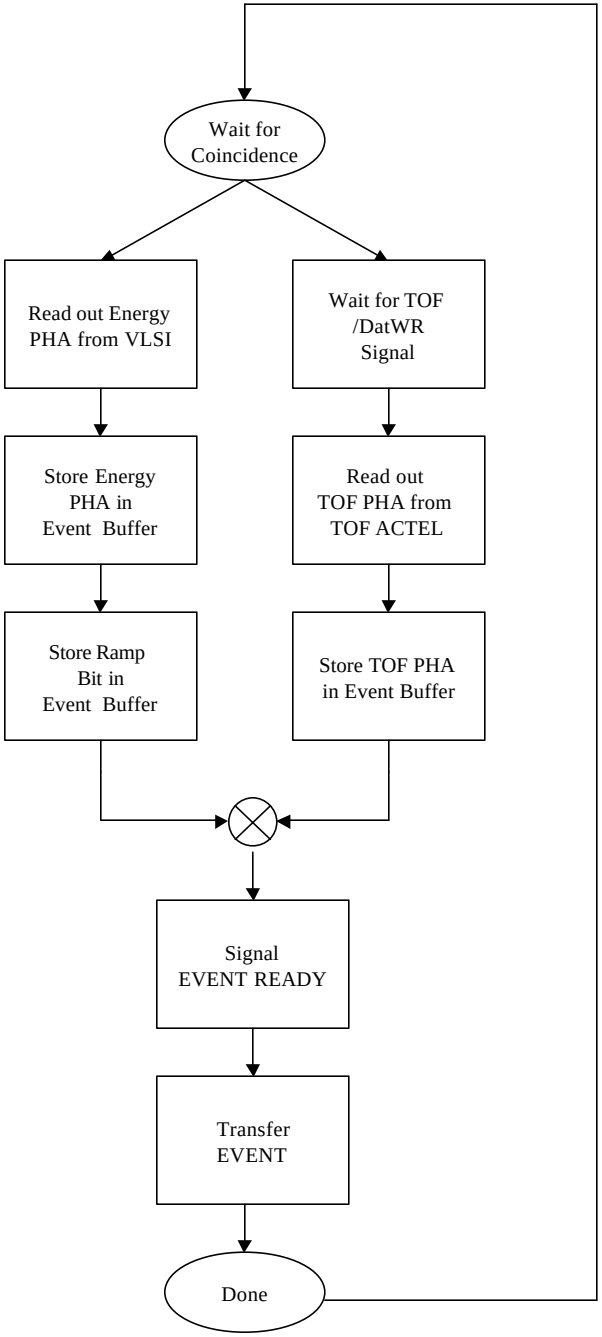
TOF DIGITAL BLOCK DIAGRAM



Front-End Logic Tasks

- Collect Events and present them to MISC
- Receive Commands from MISC and Execute them
  - VLSI initialization and control
  - HV control (Digital to Analog conversion)
- Provide 10MHz clock for TOF Circuit

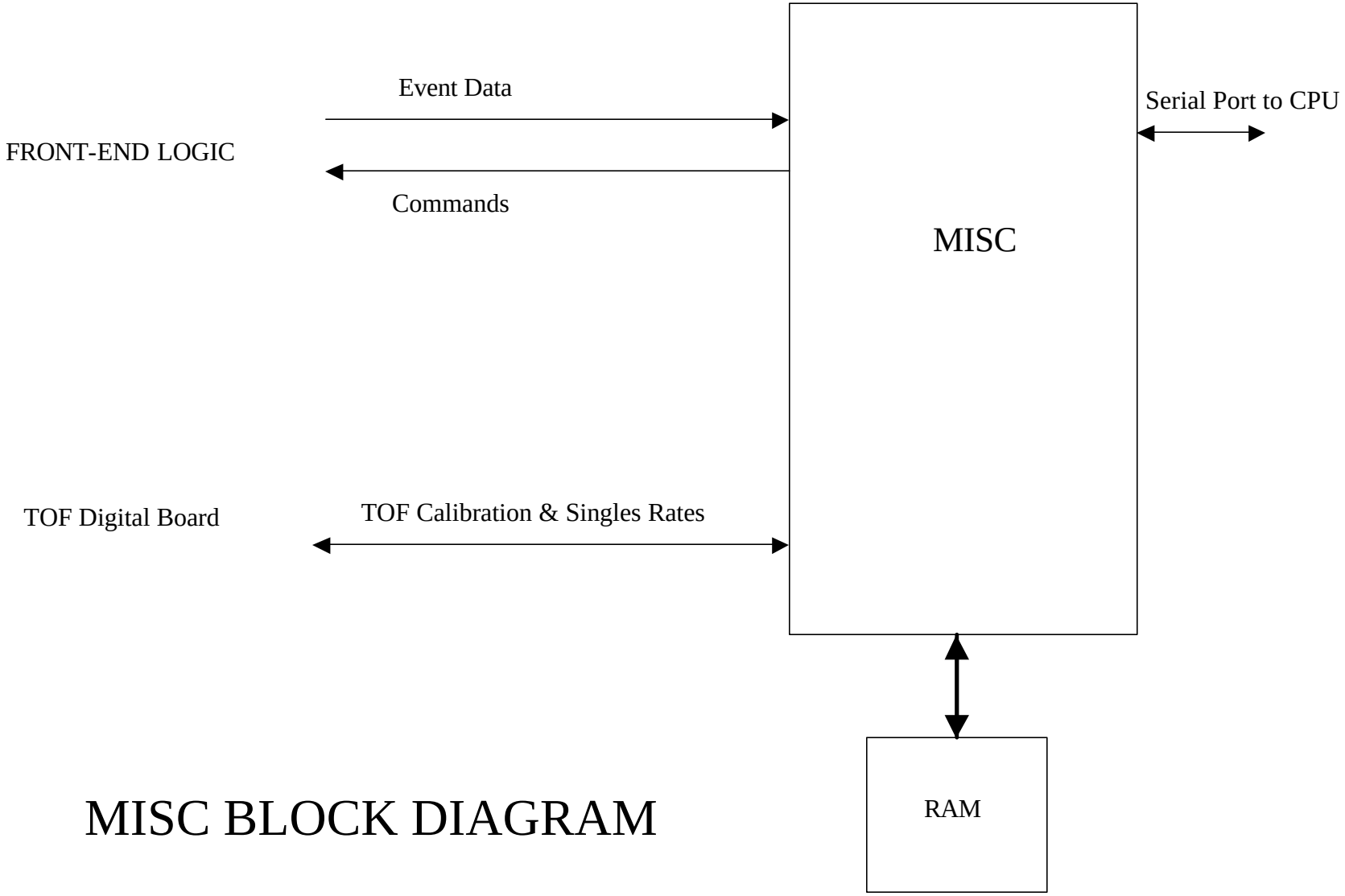

ACTEL
Data
To
Energy VLSI
Control
VLSI Readout Circuitry
Event
Buffer
Data
To
MISC
Data
To
TOF Digital
Control
TOF Readout Circuitry
/Coinc
/DatWR
Control Logic
Data
Ready
Flag
VLSI
Initialization
Command Circuitry
HV Control
DAC
SIT Front-End Logic Block
10 MHz
Clock for
TOF



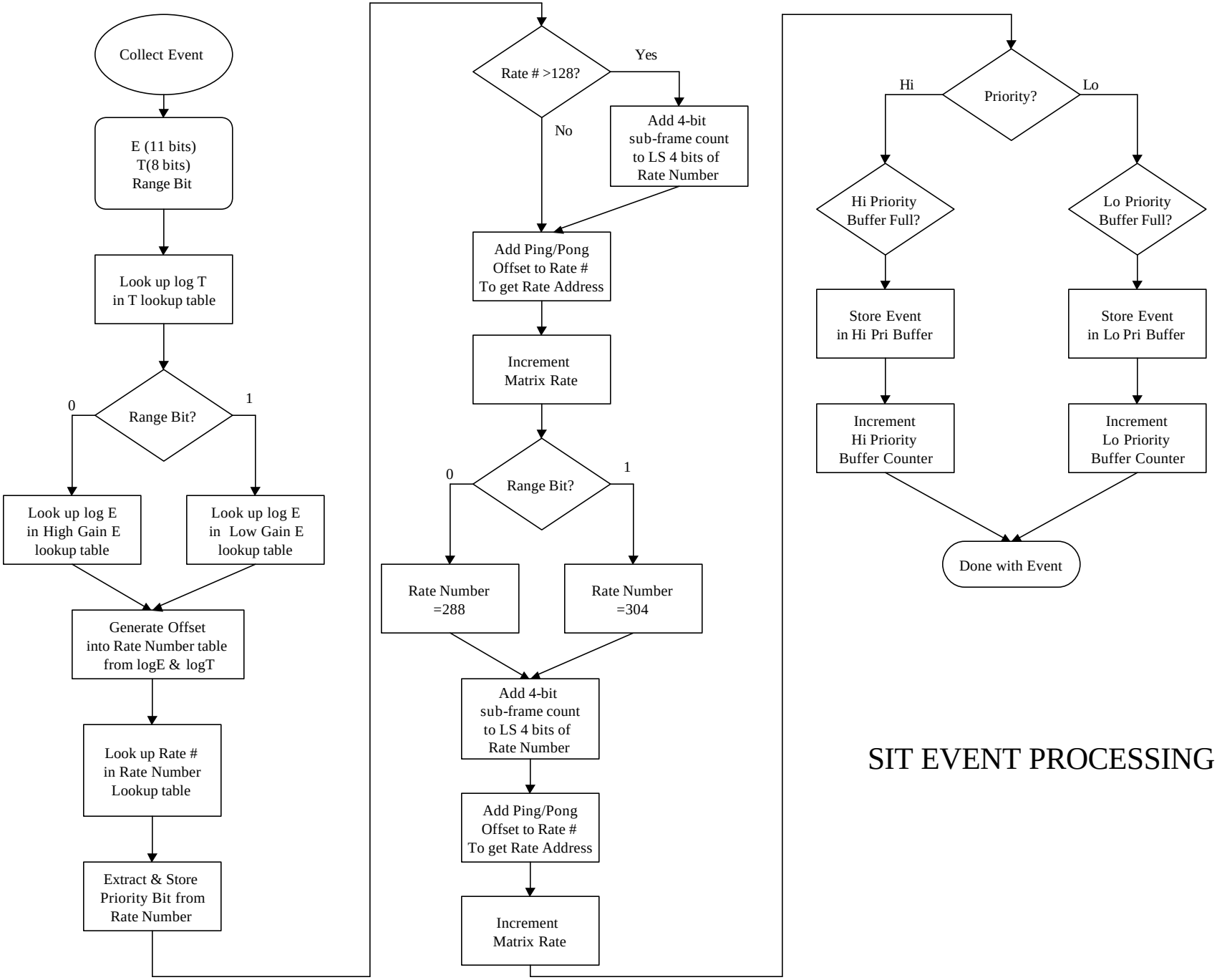
SIT Event Pre-Processing in Front-End Logic

MISC Tasks

- Initialization of Self and VLSI
  - Power-on reset
  - External reset from SEP CPU
  - Watchdog timer?
- Event Processing
  - Event binning/matrix rate counting
  - Event prioritization and storage
- TOF Calibration
- Singles Rate Collection (counting done in TOF)
- Command Processing
- Output data Formatting and Transmitting
  - rate compression
  - buffer management
  - output data to SEP CPU



MISC BLOCK DIAGRAM



SIT EVENT PROCESSING

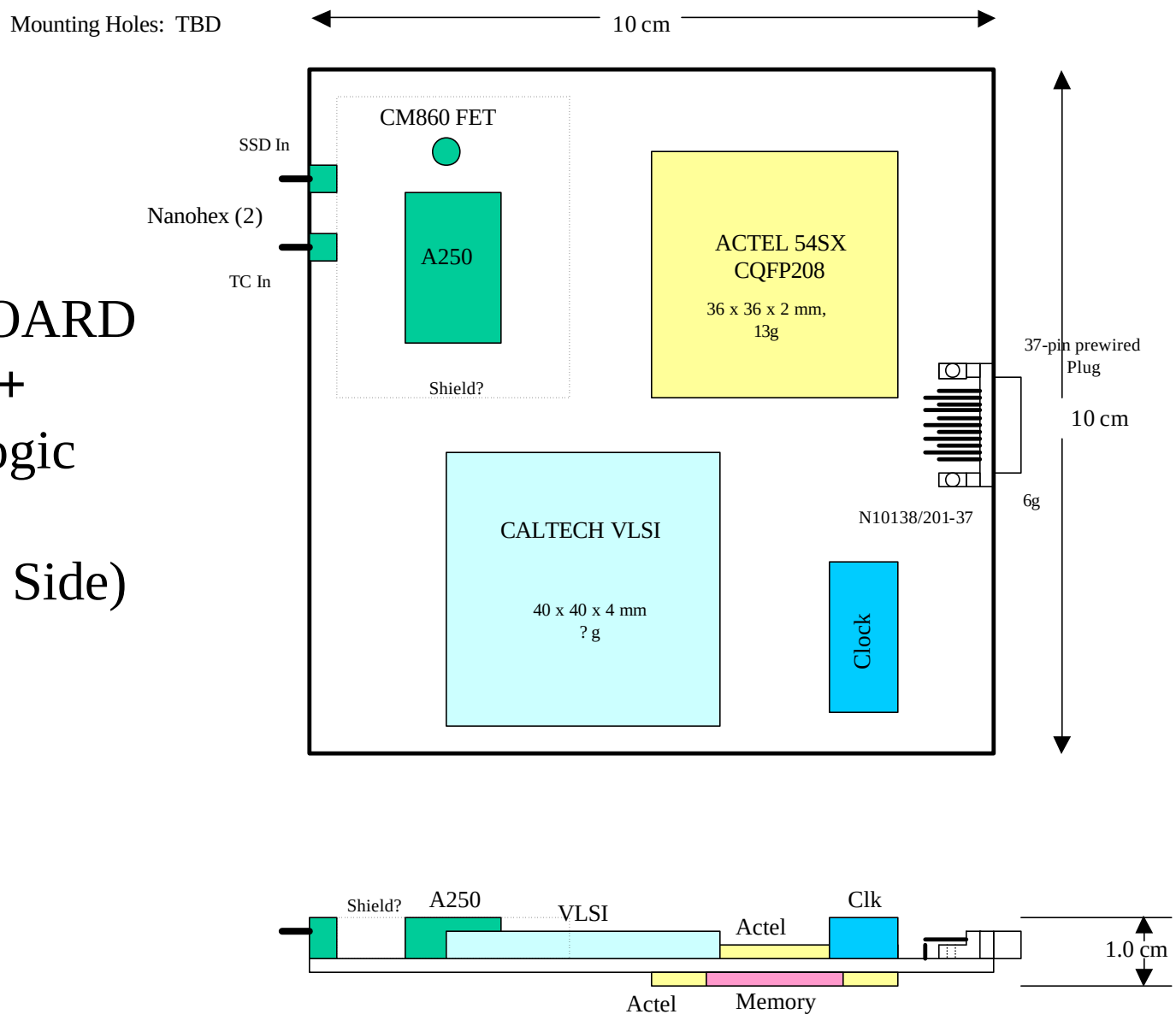
HVPS

- Provides bias voltages to operate the microchannel plates and to "focus" the secondary electrons produced by incoming ions
- Nominal voltages: 3400,3200,2200,2000,1000 and 950 v
- Top voltage controlled by command, others change proportionally
- 0-5v control voltage
- Maximum output ~4200v
- On/Off Command : 5v level
- Disable plug to prevent operation during ground testing
- Operates on +/- 12v
- Supplied in housing by UCB

Board Outlines

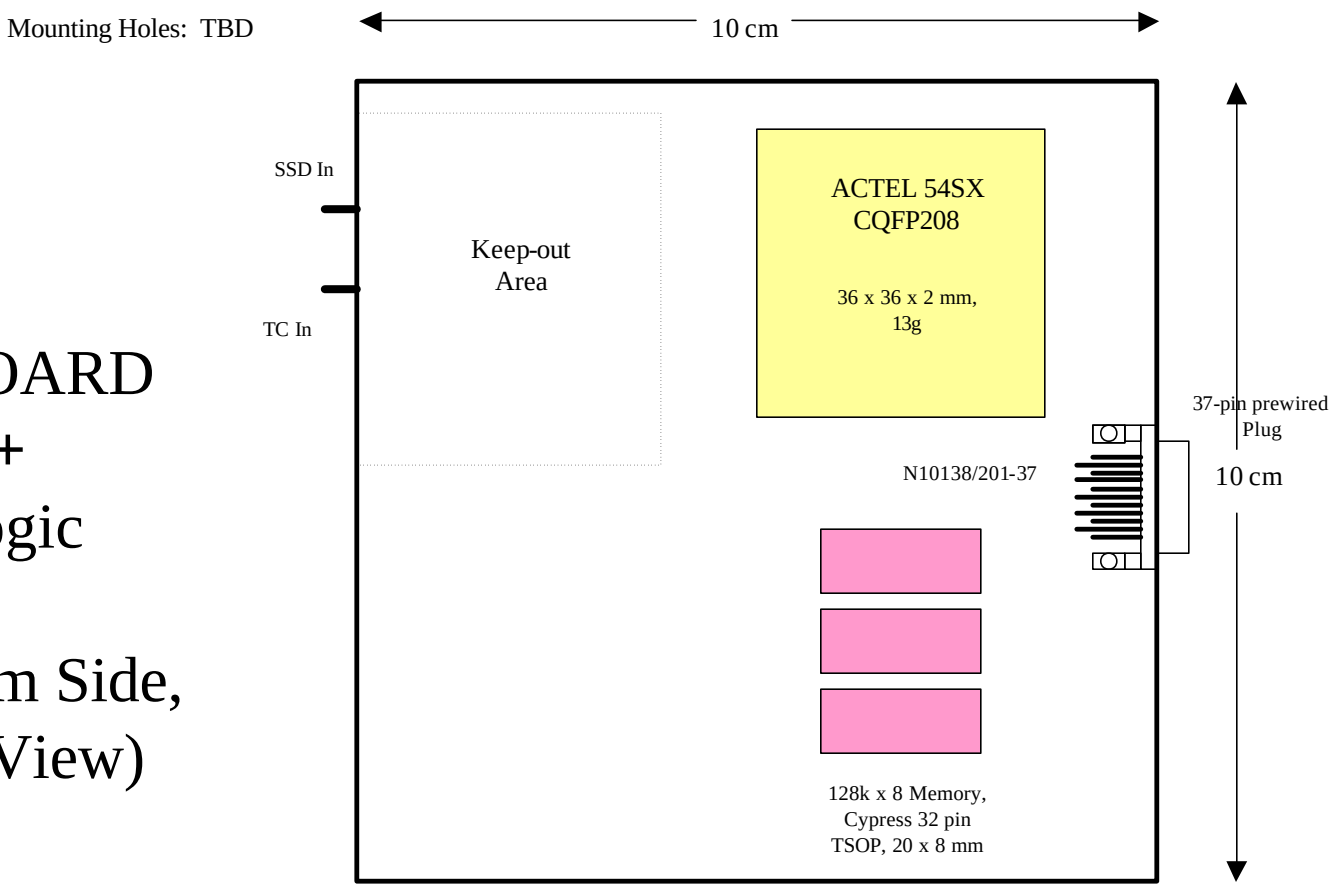
E BOARD + Logic

(Top Side)

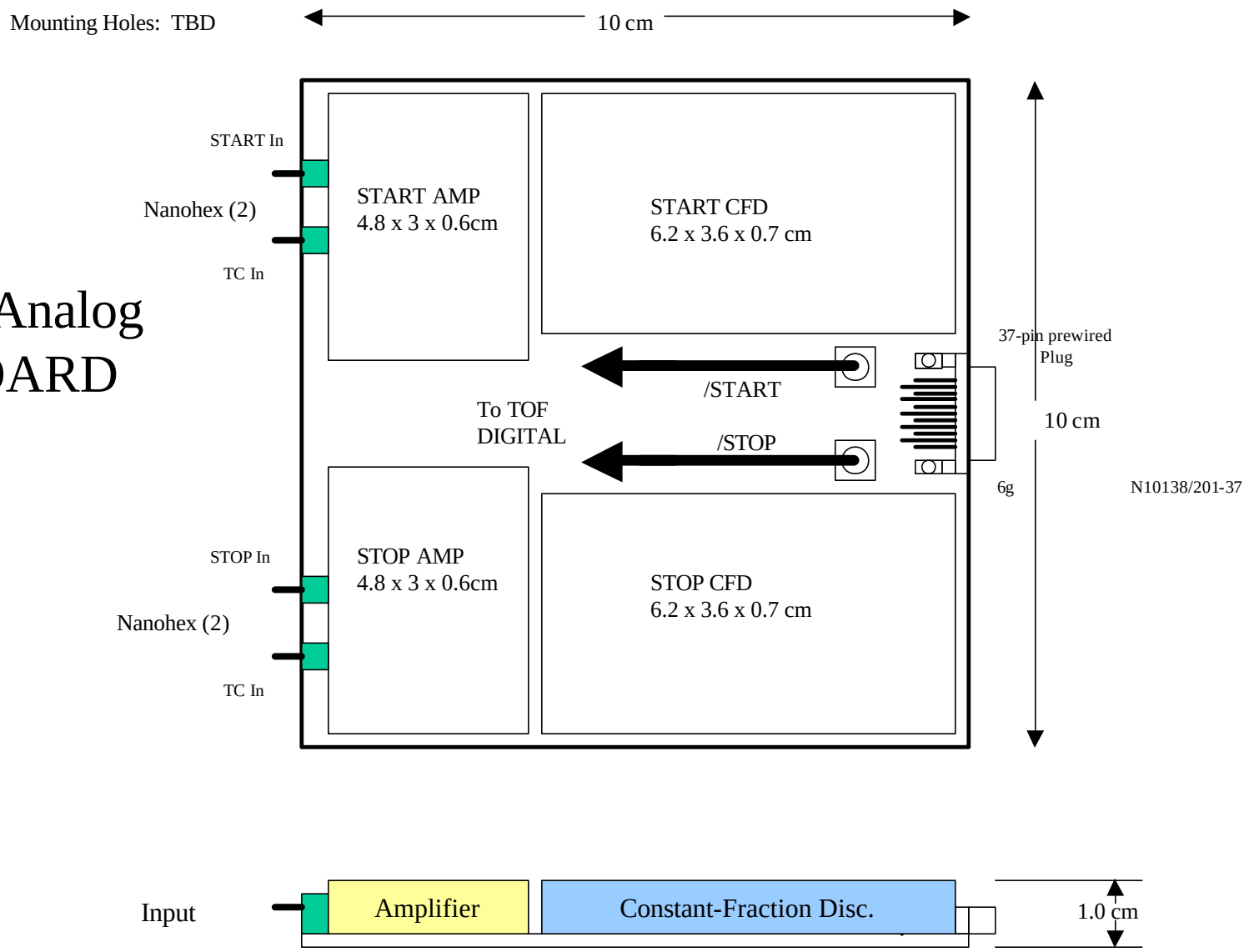


E BOARD + Logic

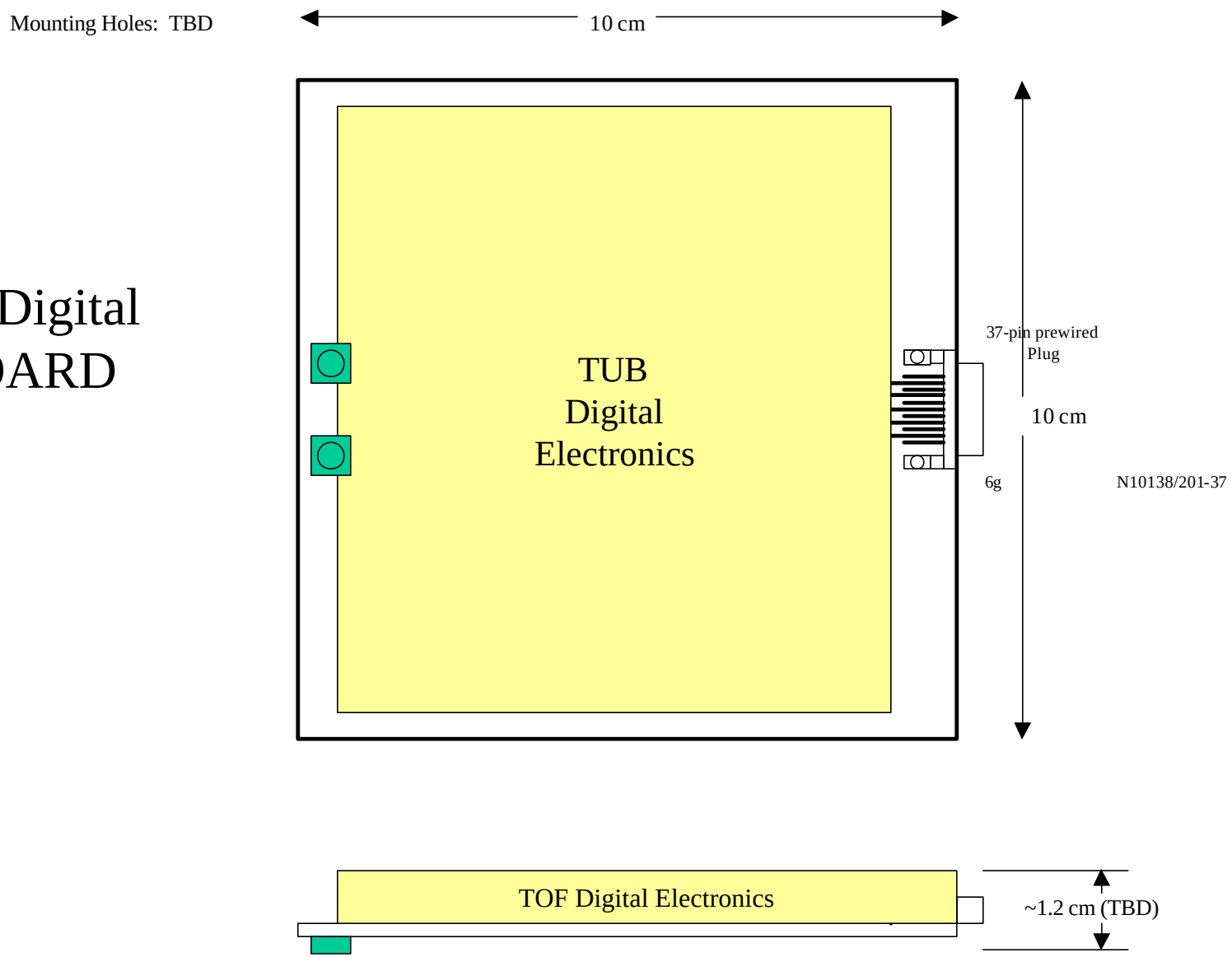
(Bottom Side, Top View)

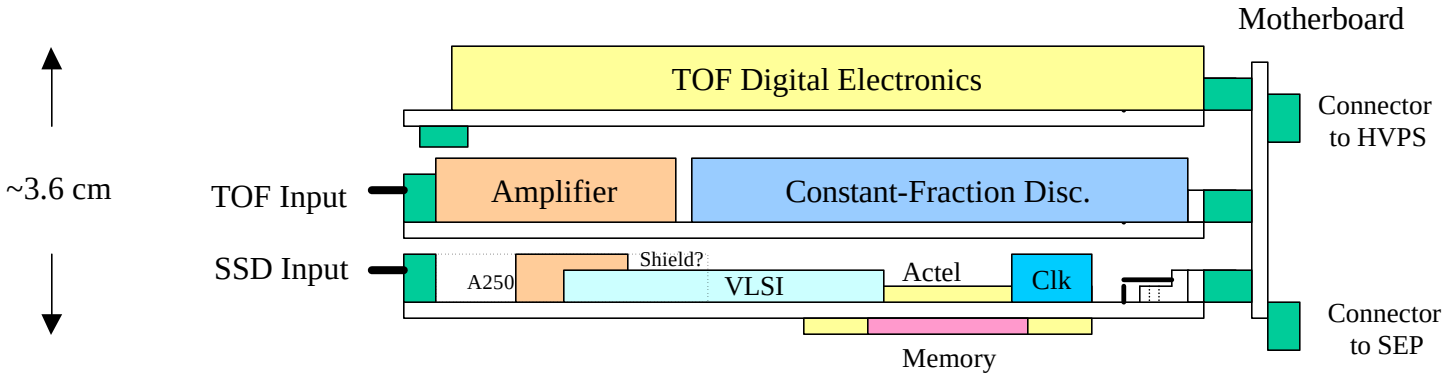


TOF Analog BOARD



TOF Digital BOARD



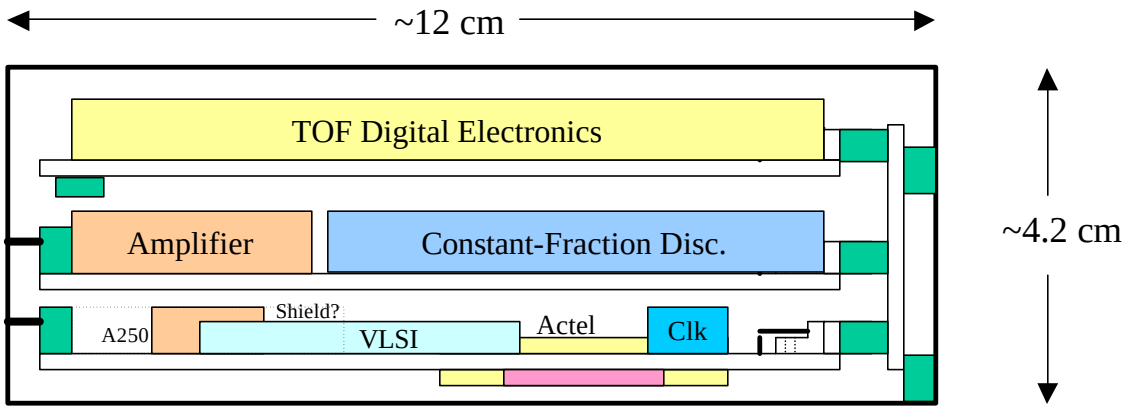


SIT Electronics Assembly

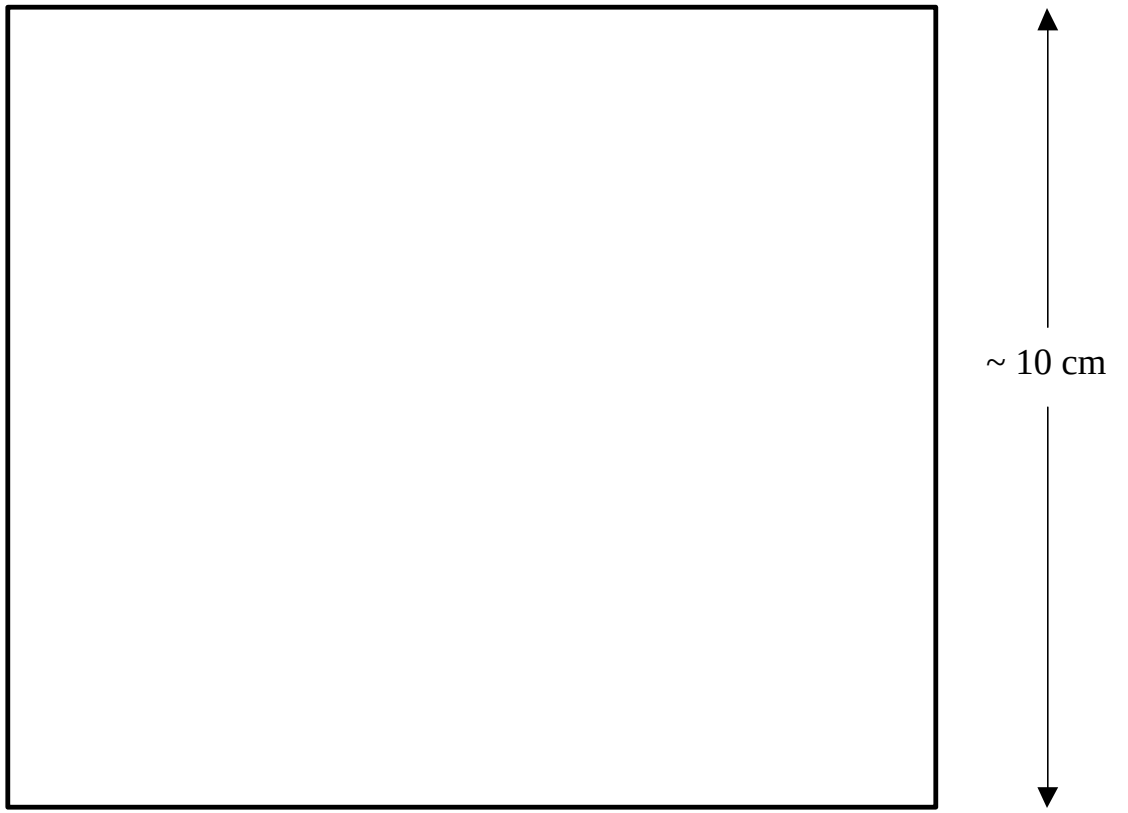
MOTHER BOARD

Overall Size

Side View



TOP View



Output Data

- PHA Events - 24 bits
  - Energy 11 bits + ramp bit
  - TOF 8 bits
  - Misc - 4 bits
- Singles Rates
- Matrix Rates
  - Low time resolution
  - High Time resolution
- Housekeeping
- Status (?)

Output Data Format

- TBD

Bit rates

-

Commissioning

- Turn ON LV with all of SEP - shortly after launch
- Open acoustic cover - TBD
  - soon to prevent sticking
  - late enough to avoid major periods (> few seconds) of sun in FOV
- Put in Science Mode - turn on and ramp up HV
  - conducted over several (e.g. 5) days
  - requires commanding and data viewing during real-time pass each day
- Verify Proper Operation - observe/process science data

Commanding

- Commissioning Phase
  - Power, cover, HV commands - several commands/day, several days
  - Verification of Operation - few tens of commands
  - Possible table upload to correct problems

- Science Mode
  - Possibly a few commands/week to calibrate sensor
  - No other periodic commands required
  - Rarely a table upload to compensate for gain drifts or other problems

Purging

- Clean dry (bottled) GN2 will be used to purge SIT telescope during integration and test at UMd
- Continuous N2 purge of telescope required during instrument testing on bench and on S/C (with obvious exceptions for environmental tests).
- Purge on pad?
- SIT will be connected to SEP purge manifold and will purge at same time as rest of SEP.
- Flow rate TBD but ~ 0.5 SCFH, Pressure TBD
- Special filters for particulates?
  - Not required for SIT but necessary to meet cleanliness?

WHO DOES WHAT
page 1 of 3

PROTOTYPE UNIT

	TASK	UMD	GSFC	CIT	UCB	MPAe
Prototype						
	Assemble Prototype Telescope		X			
	Test Prototype Telescope	X				
	Modify TOF Amp/Disc Design	X				
	Build/test prototype analog TOF board	X				
	Deliver Prototype Digital TOF system					X
	Integrate Analog and Digital TOF boards	X				
	Test Prototype TOF System	X				
	Charge Amp Design	X				
	Provide "Data Sheet" for VLSI			X		
	Assist Design to I/F CSA to VLSI			X		
	Outline SIT Logic Requirements	X				
	Detailed Front-end Logic Design		X			
	Prototype ACTEL Design		X			
	Specify CPU I/F requirements			X		
	Prototype MISC Design		X	X		
	Procure prototype MISC parts (ACTEL,RAM)		X	X		
	Generate data processing algorithms	X				
	Prototype MISC firmware		X			
	Design/Procure Prototype Energy PCB	X				
	Provide Prototype VLSI			X		
	Provide ACTEL Socket			X		
	Provide Other Proto E parts	X				
	Stuff Prototype Energy/Logic/MISC Board		X			
	Test Prototype Energy Board	X				
	Deliver prototype HVPS to UMD				X	
	Test Prototype HVPS	X				
	Test Harness design/build/test	X				
	Assemble/Test SIT Prototype	X				

WHO DOES WHAT
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FLIGHT MODEL UNIT 1

	TASK	UMD	GSFC	CIT	UCB	MPAe
FM1						
	Procure SSD/MCP/Foils	X				
	Design/Build Sunshade/Cover		X			
	Build FM1 Telescope		X			
	Test FM1 Telescope	X				
	Generate TOF analog board parts list	X				
	Procure TOF analog board parts		X			
	Layout flight TOF analog board	X				
	Procure flight TOF analog board PCBs	X				
	Assemble FM1 TOF analog board		X			
	Test FM1 TOF analog board	X				
	Deliver FM1 TOF digital board					X
	Integrate FM1 TOF A and D boards	X				
	Test FM1 TOF	X				
	Procure flight Energy PCB	X				
	Generate final Energy board parts list	X				
	Deliver flight VLSI chips			X		
	Procure Parts: ACTELs, RAM			X		
	Other parts		X			
	Design flight front-end logic		X			
	Make flight front-end logic ACTEL		X			
	Generate final MISC firmware		X			
	Make flight MISC ACTEL		X			
	Assemble FM1 energy board		X			
	Test FM1 energy board	X				
	Deliver FM1 HVPS to UMD				X	
	Test FM1 HVPS	X				
	Layout and procure flight motherboard PCB	X				
	Procure parts for motherboard		X			
	Assemble FM1 motherboard		X			
	Test FM1 motherboard	X				
	Assemble and Test FM1 unit	X				
	Conformal coat E, Logic and MB		X			
	Post-coat assy & test	X				

WHO DOES WHAT
page 3 of 3

FLIGHT MODEL UNIT 2

	TASK	UMD	GSFC	CIT	UCB	MPAe
FM2						
	Build FM2 Telescope		X			
	Test FM2 Telescope	X				
	Assemble FM2 TOF analog board		X			
	Test FM2 TOF analog board	X				
	Deliver FM2 TOF digital board					X
	Integrate FM2 TOF A and D boards	X				
	Test FM2 TOF	X				
	Assemble FM2 energy board		X			
	Test FM2 energy board	X				
	Deliver FM2 HVPS to UMD				X	
	Test FM2 HVPS	X				
	Assemble FM2 motherboard		X			
	Test FM2 motherboard	X				
	Assemble and Test FM2 unit	X				
	Conformal coat E, Logic and MB		X			
	Post-coat assy & test	X				
	Deliver FM1 and FM2 to Caltech	X				
GSE						
	CPU Simulator	X				
	SIT Stimulus Unit	X				