Minimum Hardware Considerations

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CHAPTER 11
MINIMUM HARDWARE CONSIDERATIONS

The 8XC196KC/KD has several basic requirements for operation within a system. It requires an external source of power, ground, the clock signal, and the RESET# signal. This chapter describes options for providing the basic requirements and describes other hardware considerations.

11.1. MINIMUM CONNECTIONS

Figure 11-1 shows a minimum hardware configuration. For predictable performance, it is important to tie unused inputs to V_{CC} or V_{SS} as shown in the sample circuit. Otherwise, unused inputs can float to a mid-voltage level and draw excessive current. External interrupt signals, such as NMI, may generate spurious interrupts if left unconnected.

NOTE

The RC network connected to V_{PP} is required only when the Powerdown feature is being used. Refer to Chapter 12, "Special Operating Modes," for information about Powerdown operation.

If HSI.2 and HSI.3 are configured as outputs, do not tie them to ground as shown in Figure 14-1.

11.1.1. Port Connections

The Port 0 pins also function as analog inputs into the A/D converter and they may be allowed to float. However, we do recommend that you connect unused Port 0 pins to V_{CC} or V_{SS}.

The quasi-bidirectional port pins (P1.0–P1.7, P2.6, and P2.7) have weak internal pull-ups. These pins may be allowed to float.

In the minimum configuration, the system address/data bus (AD0–AD15) functions as Ports 3 and 4 with a default value of 0FFFFH. Since the Port 3 and 4 outputs are open-drain outputs, they will float unless they are connected to external circuitry. To prevent potential problems, either tie the pins to ground or write zeros to Ports 3 and 4.

11.2. POWER AND GROUND PINS

Power to the 8XC196KC/KD flows through several pins. V_{CC} supplies the positive voltage to the digital portion of the device, while V_{REF} supplies the positive voltage to the A/D converter and Port 0. Connect V_{CC} and V_{REF} to +5V power supplies. If the A/D converter will be used, connect V_{REF} to a separate reference supply to minimize noise during A/D conversions.

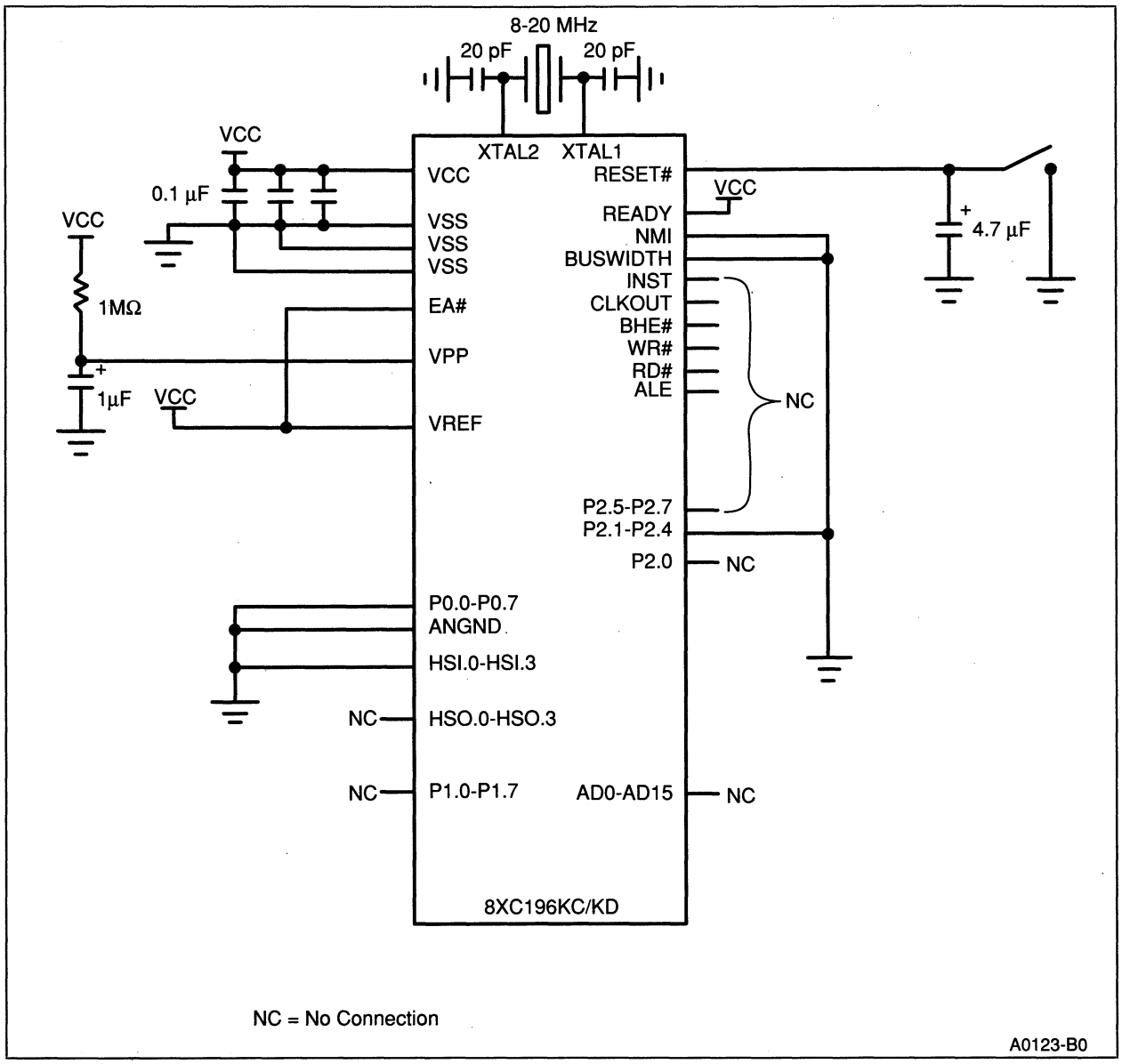

Figure 11-1. 8XC196KC/KD Minimum Hardware Connections

The V_{SS} pins and ANGND must all be nominally at the same potential (± 50 mV). For best A/D operation, connect ANGND and V_{SS} to a single point as close to the device as possible. Use the shortest possible path to connect the V_{SS} lines to ground. Add decoupling capacitors between each V_{SS} pin and V_{CC}.

Figure 11-2 shows connections for V_{CC}, V_{REF}, V_{SS}, and ANGND

NOTE

Even if the A/D converter will not be used, V_{REF} and ANGND must be connected to provide power to Port 0. Refer to Chapter 9, "Analog-to-Digital Converter," for a detailed discussion of A/D power and ground recommendations.

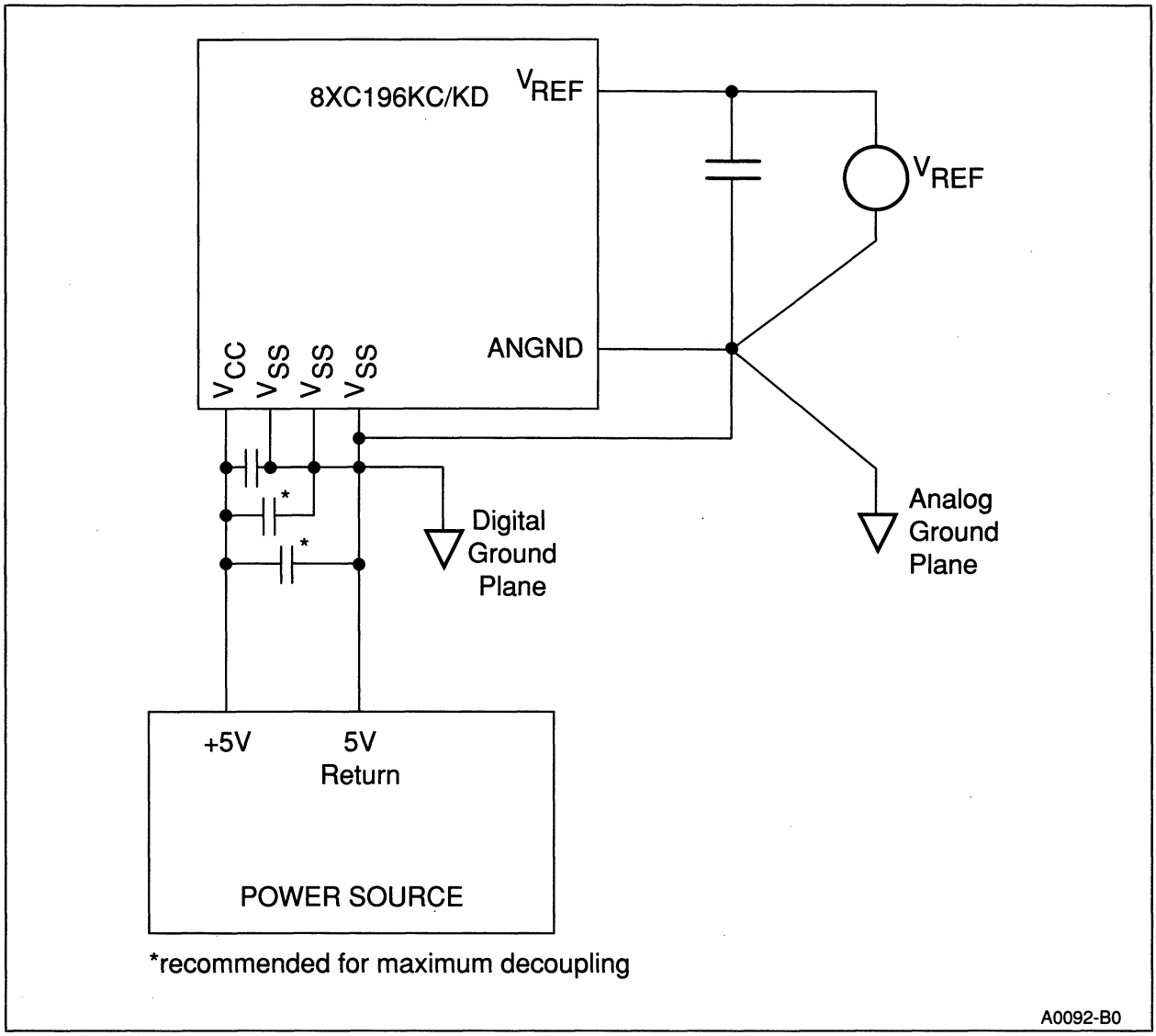

Figure 11-2. Power and Return Connections

11.2.1. Noise Protection Tips

The fast rise and fall times of high-speed CMOS logic often produces noise spikes on the power supply lines and outputs. To minimize noise, it is important to follow good design and board layout techniques. We recommend liberal use of decoupling capacitors and transient absorbers. Connect 0.01 µF bypass capacitors between V_{CC} and each V_{SS} pin and between V_{REF} and ANGND to reduce noise. Place the capacitors as close to the device as possible.

Multilayer printed circuit boards with separate V_{CC} and ground planes also help to minimize noise. For more information on noise protection, refer to Application Note AP-125, "Designing Microcontroller Systems for Noisy Environments."

11.3. CLOCK SOURCES

The 8XC196KC/KD can either generate the clock signal on-chip or use an external clock input signal. To use the on-chip oscillator, connect an external crystal to XTAL1 and XTAL2. Otherwise, connect an external clock input signal to XTAL1 and let XTAL2 float.

11.3.1. On-Chip Oscillator

The on-chip oscillator circuit consists of a crystal-controlled, positive reactance oscillator (see Figure 11-3). In this application, the crystal operates in a parallel resonance mode.

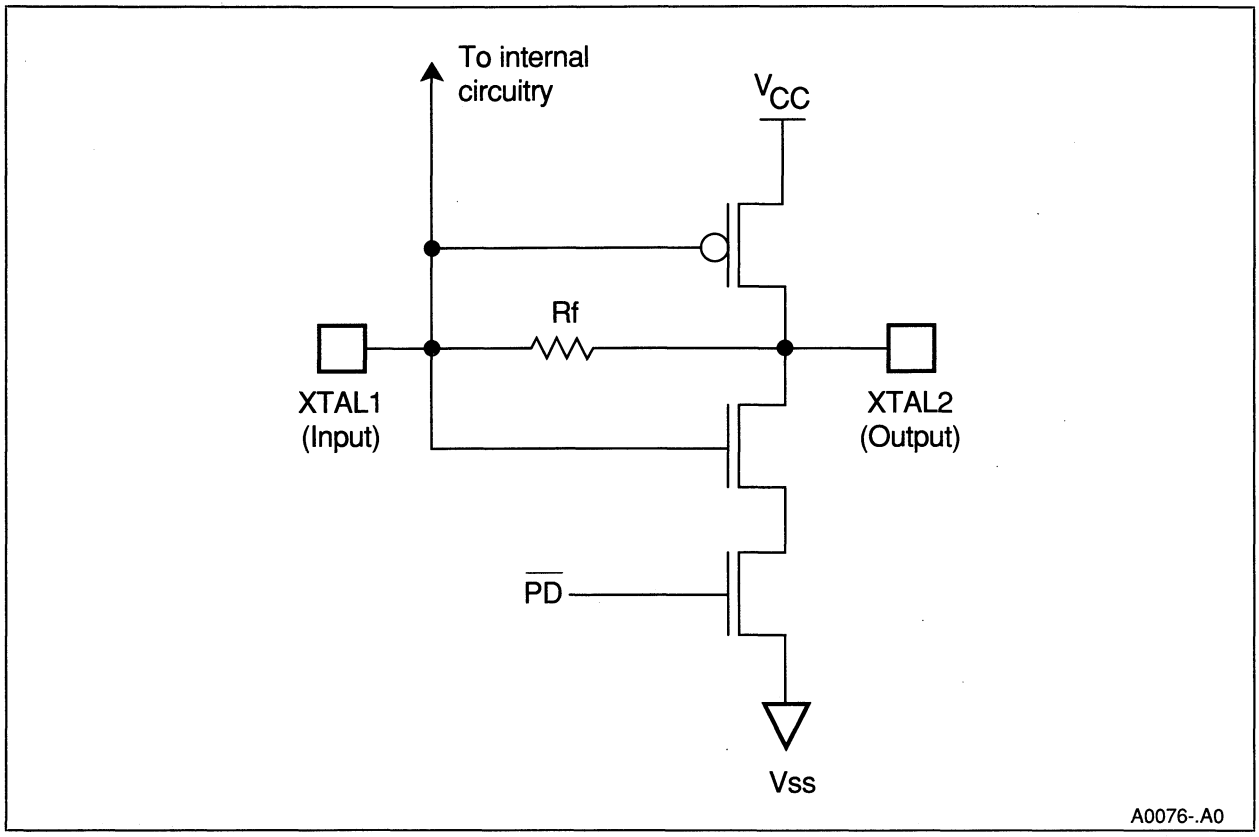

Figure 11-3. On-Chip Oscillator Circuit

The feedback resistor, Rf, consists of paralleled *n*-channel and *p*-channel FETs controlled by the internal powerdown signal (PD). In Powerdown mode, Rf acts as an open and the output drivers are disabled, which disables the oscillator. Both XTAL1 and XTAL2 have built-in electrostatic discharge (ESD) protection.

11.3.1.1. USING CRYSTAL OSCILLATORS

Figure 11-4 shows the connections between the external crystal and the 8XC196KC/KD. Consult the manufacturer's data sheet for performance specifications and required capacitor values. When designing an external oscillator circuit, consider the effects of parasitic board capacitance, extended operating temperatures, and crystal specifications. With quality

components, 20 pF load capacitors (C_L) are usually adequate for any frequency above 1 MHz.

Noise spikes on the XTAL1 or XTAL2 pin can cause a miscount in the internal clock-generating circuitry. Capacitive coupling between the crystal oscillator and traces carrying fast-rising digital signals can introduce noise spikes. To reduce this coupling, mount the crystal oscillator and capacitors near the device and use short, direct traces to connect to XTAL1, XTAL2, and V_{SS}. To further reduce the effects of noise, use grounded guard rings around the oscillator circuitry and ground the metallic crystal case.

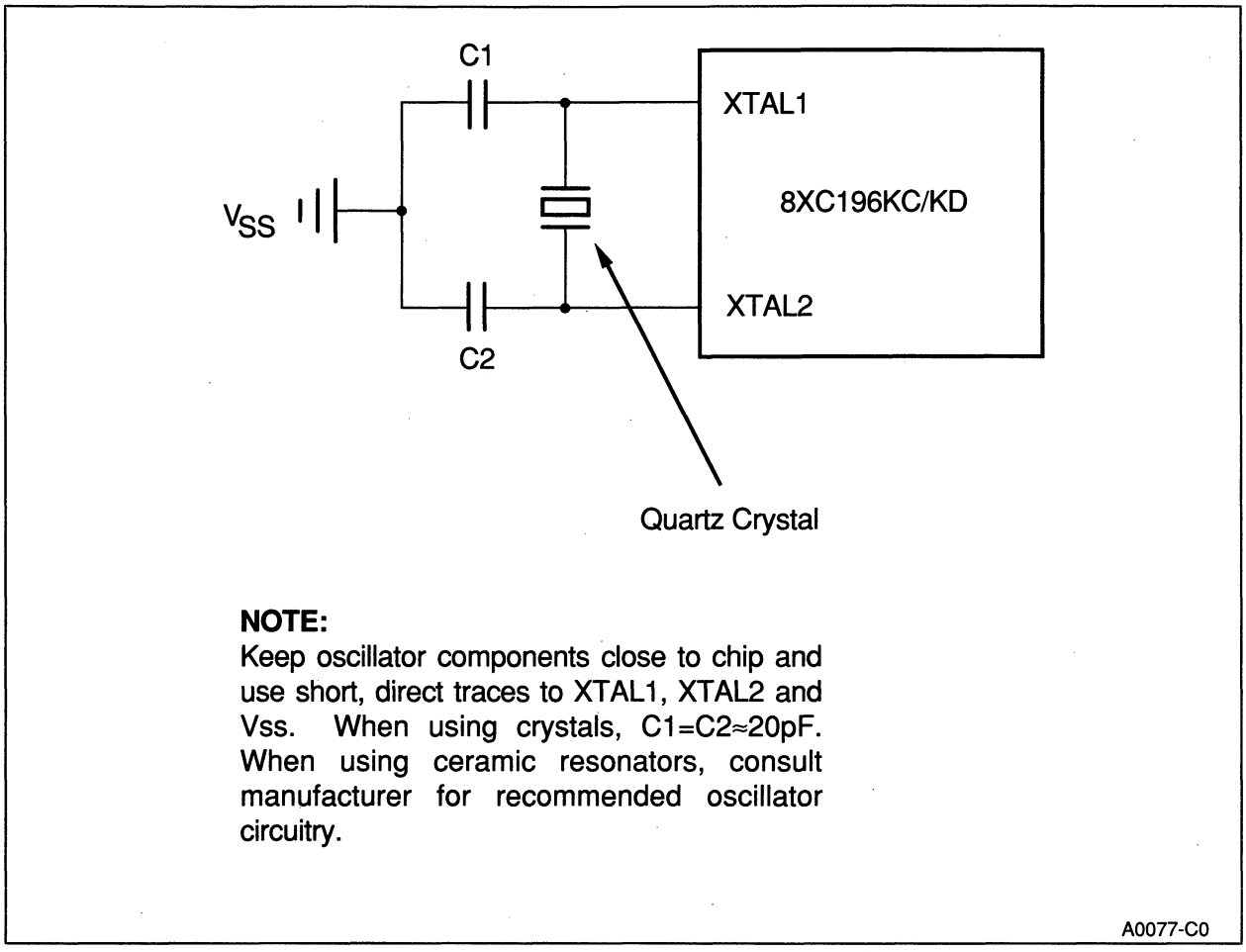

Figure 11-4. External Crystal Connections

11.3.1.2. USING CERAMIC RESONATORS

In cost-sensitive applications, you may choose to use a ceramic resonator instead of a crystal oscillator. Ceramic resonators may require slightly different load capacitor values and circuit configurations. Consult the manufacturer's data sheet for the required oscillator circuitry.

11.3.2. Using an External Clock Signal

To use an external clock source, apply a clock signal to XTAL1 and let XTAL2 float. An example of this circuit is shown in Figure 11-5. See the data sheet for the required XTAL1 voltage drive levels.

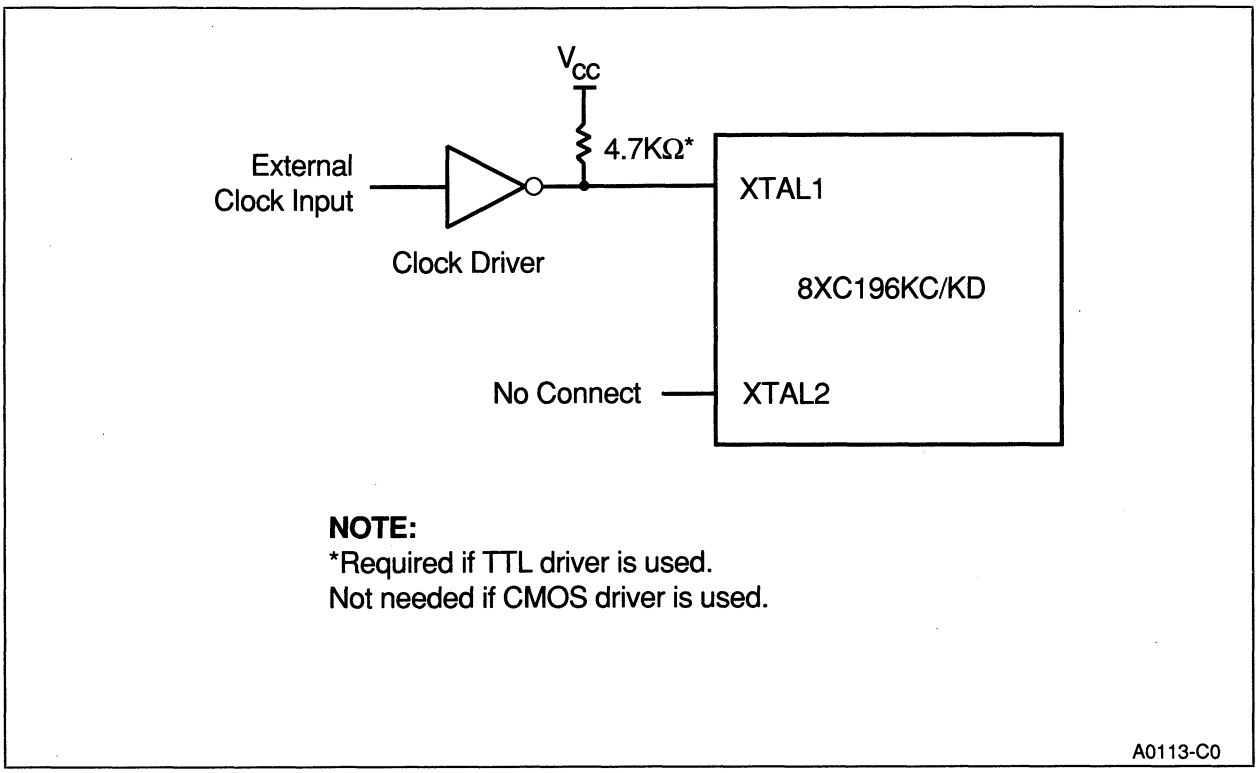

Figure 11-5. External Clock Connections

The external clock source must meet the minimum high and low times (T_{XHXX} and T_{XLXX}) and the maximum rise and fall transition times (T_{XLHX} and T_{XHXL}) to ensure proper operation (see Figure 11-6). The longer the rise and fall times, the higher the probability that external noise will affect the clock generator circuitry and cause unreliable operation. See the data sheet for actual specifications.

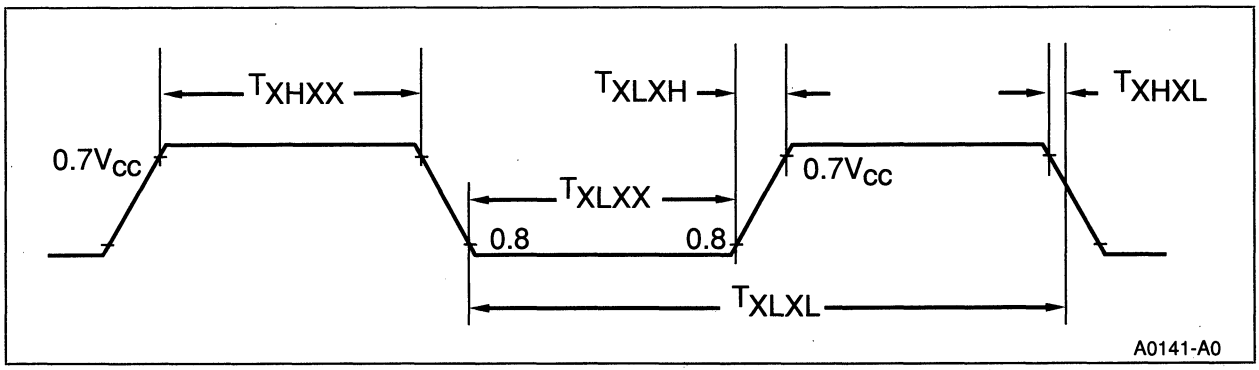

Figure 11-6. External Clock Drive Waveforms

At power-on, the interaction between the internal amplifier and its feedback capacitance (i.e., the Miller effect) may cause a load of up to 100 pF at the XTAL1 pin, if the signal at XTAL1 is small, such as might be the case during start-up of the external oscillator. This problem will go away when the XTAL1 input signal meets the V_{IL} and V_{IH1} specifications (see the data sheet). If these specifications are met, the XTAL1 pin capacitance will not exceed 20 pF.

11.4. RESETTING THE 8XC196KC/KD

Reset forces the 8XC196KC/KD into a known state. (See Table B-3 in Appendix B and Table C-3 in Appendix C for pin and register status after reset.) The device remains in its reset state until RESET# is deasserted. When RESET# is deasserted, the bus controller fetches the Chip Configuration Byte (CCB) from location 2018H, loads it into the Chip Configuration Register (CCR), and then fetches the first instruction at location 2080H. Figure 11-7 shows the reset-sequence timing. Depending upon when RESET# is brought high, the CLKOUT signal may become out of phase with the PH1 internal clock. When this occurs, the clock generator immediately resynchronizes CLKOUT as shown in Case 2.

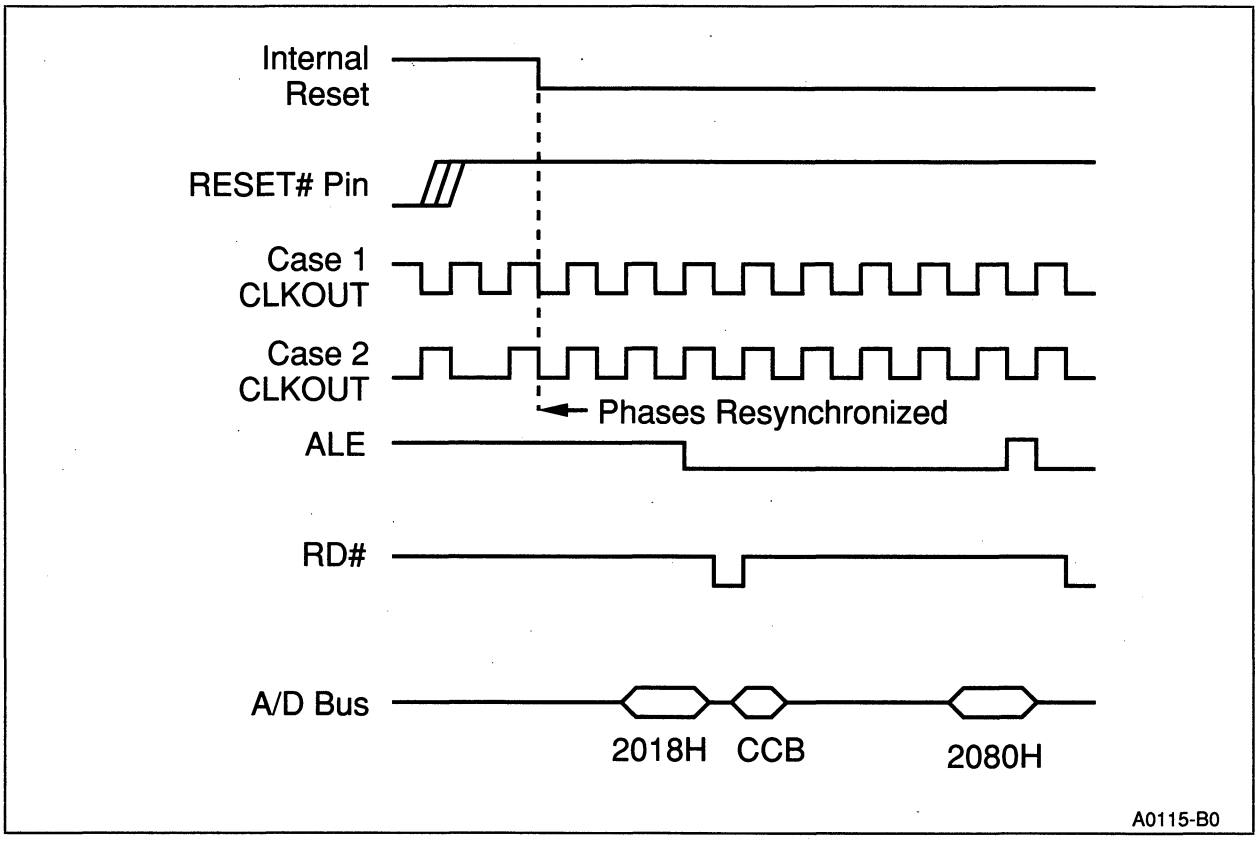

Figure 11-7. Reset Timing Sequence

The following events will reset the 8XC196KC/KD (see Figure 11-8):

- An external device drives the RESET# pin low
- The CPU issues the Reset (RST) instruction
- The CPU issues an IDLPD instruction with an illegal key operand
- The Watchdog timer (WDT) overflows

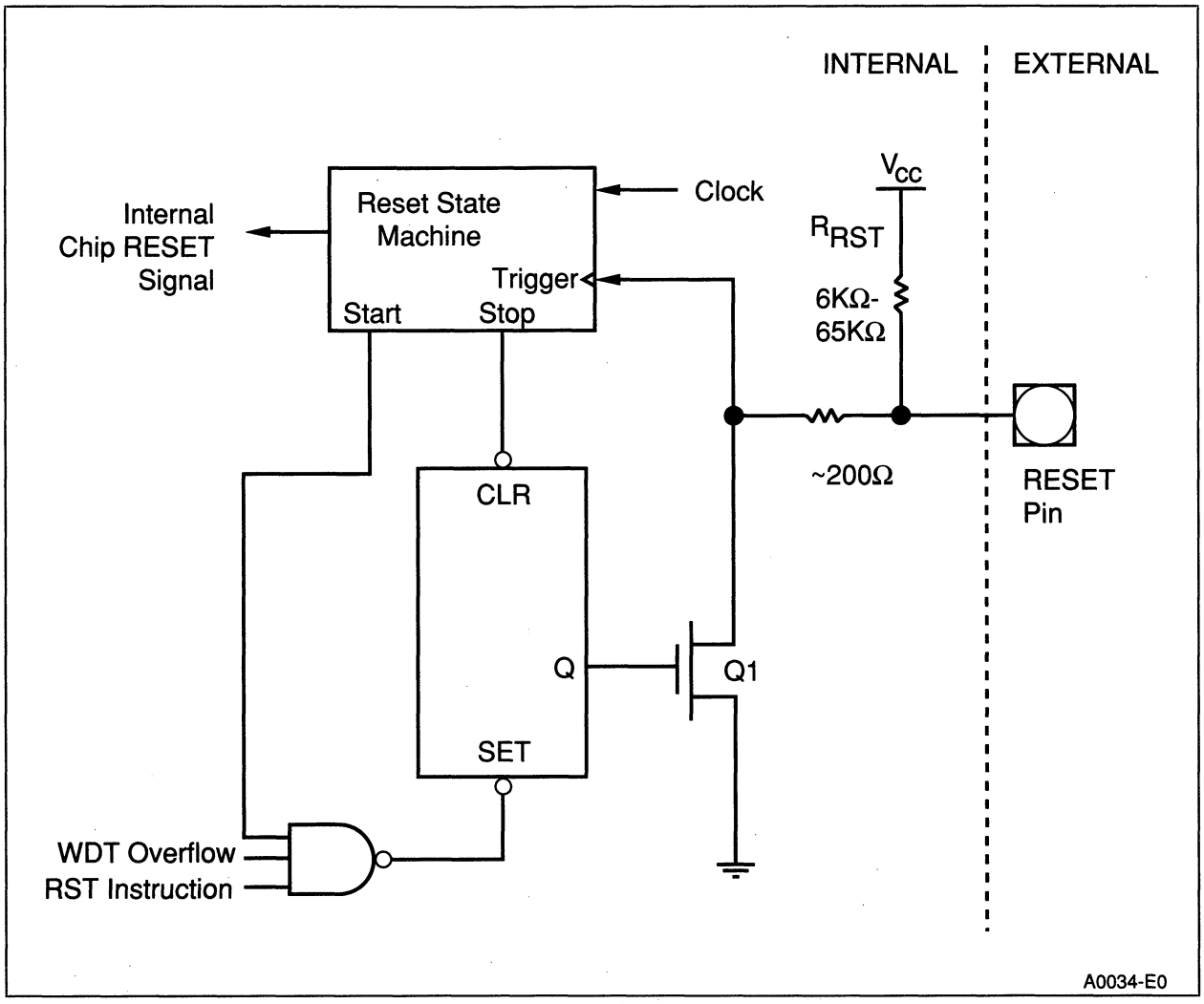

Figure 11-8. Reset Pin Internal Circuit

11.4.1. Pulling the RESET# Pin Low

To reset the device, hold the RESET# pin low for at least one state time after the power supply is within tolerance and the oscillator has stabilized. When RESET# is first asserted, the device turns on a pull-down transistor (Q1) for 16 state times. This enables the RESET# signal to function as the system reset.

11.4.1.1. EXTERNAL RESET CIRCUITS

The simplest way to reset an 8XC196KC/KD is to insert a capacitor between the RESET# pin and V_{SS}, as shown in Figure 11-9. The 8XC196KC/KD has an internal pull-up which has a value between 6 KΩ and 65 KΩ (R_{RST}). RESET# should remain asserted for at least one state time after V_{CC} and XTAL1 have stabilized and meet the operating conditions specified in the data sheet. A 4.7 µF or greater capacitor should provide sufficient reset time, as long as V_{CC} rises quickly.

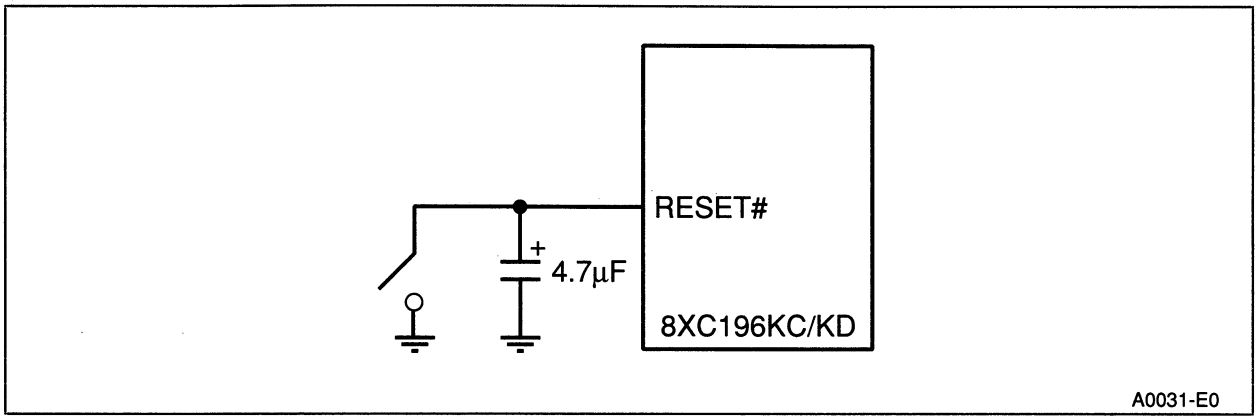

Figure 11-9. Minimum Reset Circuit

This minimum circuit is not adequate when the RESET# pin provides the system reset. The other devices may not be reset because the capacitor will keep the voltage above V_{IL},. Since RESET# is asserted for only 16 state times, it may be necessary to lengthen and buffer the system-reset pulse. Figure 11-10 shows an example of a system-reset circuit. In this example, D2 creates a wired-OR gate connection to the reset pin. An internal 8XC196KC/KD reset, system power up, or the closing of SW1 will generate the system-reset signal.

11.4.2. Issuing the Reset (RST) Instruction

The RST instruction (opcode FFH) resets the 8XC196KC/KD by pulling RESET# low for 16 state times. It also clears the program status word (PSW), sets the master program counter (PC) to 2080H, and resets the Special Function Registers (SFRs). See Table C-3 in Appendix C for the reset values of the SFRs.

Putting pull-ups on the address/data bus causes unimplemented areas of memory to be read as 0FFH. If unused internal OTPROM memory is set to 0FFH, then execution from any unused memory locations will reset the 8XC196KC/KD.

11.4.3. Issuing an Illegal IDLPD Key Operand

The 8XC196KC/KD resets itself if an illegal key operand is used with the IDLE/POWERDOWN (IDLPD) command. The legal keys are "1" for Idle mode and "2" for Powerdown mode. If any other value is used, the device executes a reset sequence. (See Appendix A for a description of the IDLPD command.)

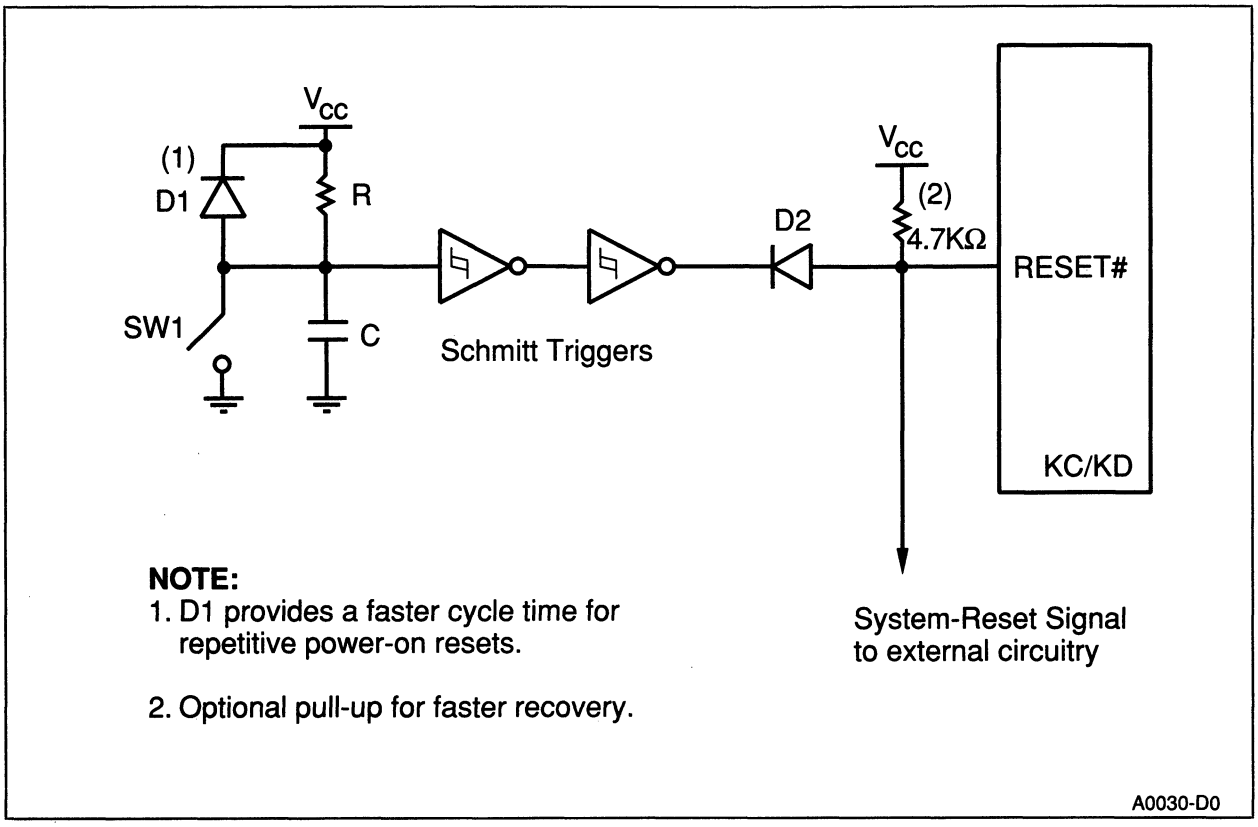

Figure 11-10. Example System Reset Circuit

11.4.4. Enabling the Watchdog Timer

The Watchdog timer (WDT) is a 16-bit ripple counter that resets the device when the counter overflows. When enabled, the Watchdog timer (WDT) monitors the execution of the user program. If the counter is not periodically cleared within 64K state times, it will reset the device. This prevents a runaway process from hanging up the system.

To clear the WATCHDOG register, send a "1EH" followed immediately by an "E1H" to location 0AH. Clearing this register the first time enables the WDT with an initial value of 0000H, which is incremented once every state time. If the counter overflows to 0000H, it drives the RESET# signal low and holds it low for 16 state times (see Figure 11-8). Once enabled, only a reset can disable the WDT.

If enabled, the WDT continues to run in Idle mode. The user program must service the WDT before it times out or it will reset the device, which causes it to exit Idle mode.