Pulse Width Modulator 10

CHAPTER 10
PULSE WIDTH MODULATOR

The 8XC196KC/KD has three Pulse Width Modulator (PWM) modules (see Figure 10-1). Each outputs a variable duty cycle pulse at a fixed frequency. These outputs may be used to drive motors that require an unfiltered PWM waveform for optimal efficiency, or they may be filtered to produce a smooth analog signal.

This chapter provides a functional overview of the Pulse Width Modulator modules, describes how to program them, and provides sample circuitry for converting the PWM outputs to analog signals.

Refer to Appendix C for details about the registers discussed in this chapter and to Appendix B for information about the PWM*x* output pins.

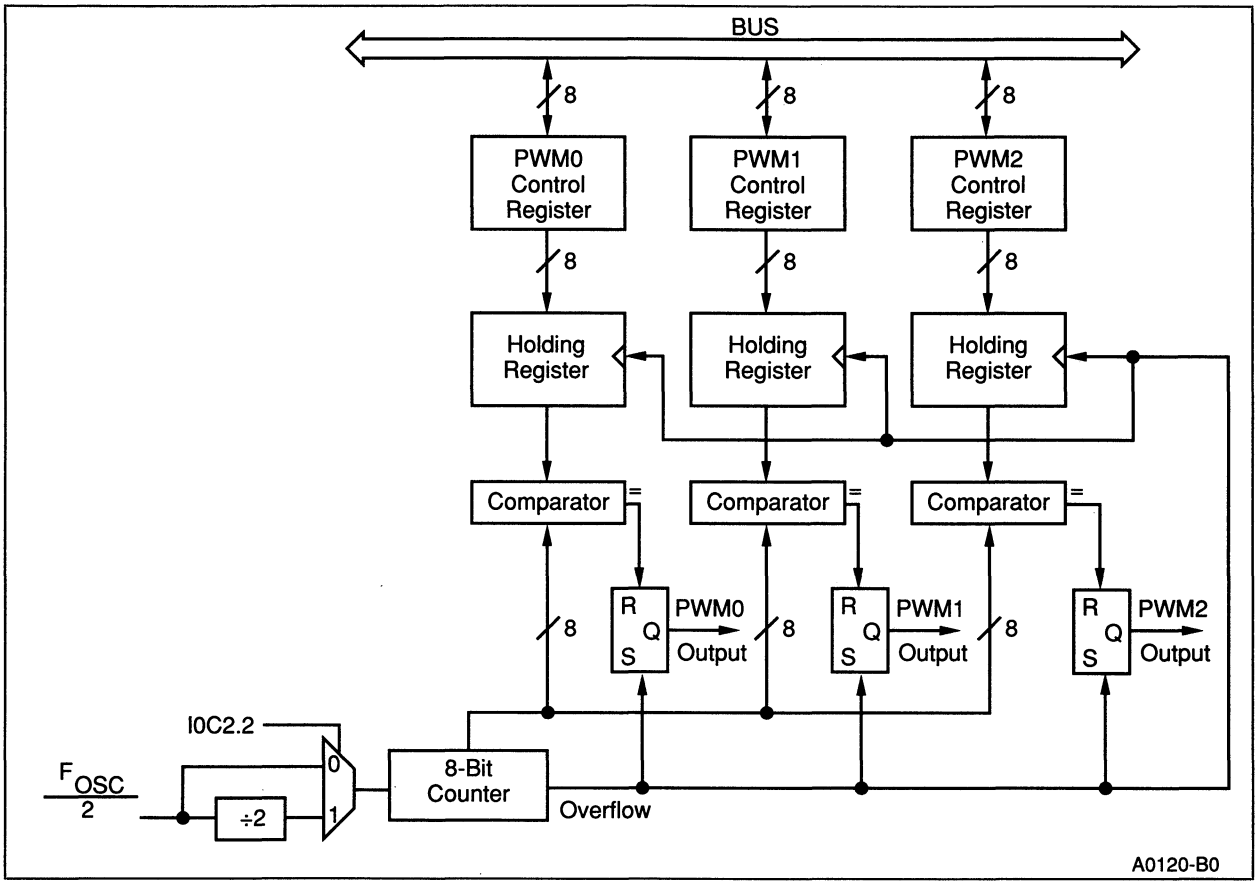

Figure 10-1. PWM Block Diagram

10.1. PWM FUNCTIONAL OVERVIEW

The PWM modules have the following main components:

- An eight-bit counter
- A divide-by-two clock prescaler
- Three comparators
- Three control registers (PWM*x*_CONTROL, where *x* is 0, 1, or 2)
- Three holding registers
- Three RS flip-flops

The SLOW_PWM bit (IOC2.2) controls the PWM output period by enabling or disabling the divide-by-two clock prescaler. Enabling the prescaler causes the 8-bit counter to increment once every two state times; disabling it causes the counter to increment once every state time.

Each control register contains an 8-bit value that is loaded into a holding register when the 8-bit counter overflows. The comparators compare the contents of the holding registers to the counter value. When the counter value is equal to zero, the PWM*x* output is driven high. It remains high until the counter value matches the value in the holding register, at which time the output is pulled low. (Loading PWM*x*_CONTROL with 00H forces the output to remain low.) When the counter overflows, the output is again switched high. Figure 10-2 shows typical PWM output waveforms.

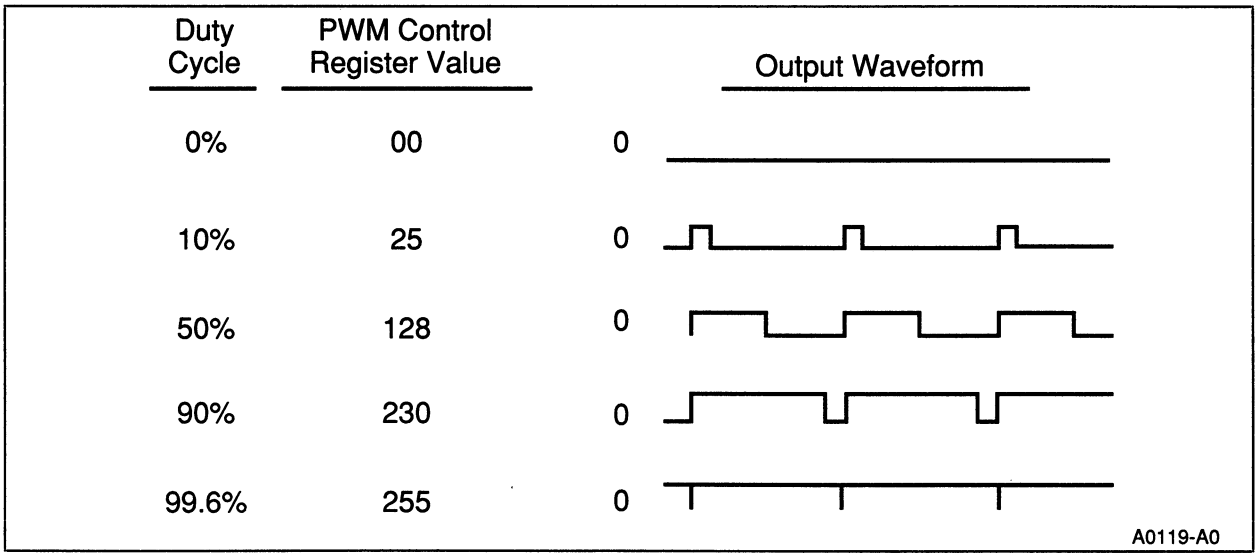

Figure 10-2. PWM Output Waveforms

10.2. PROGRAMMING THE PWM DUTY CYCLE

The PWM*x*_CONTROL register, in conjunction with the SLOW_PWM bit (IOC2.2), determines how long the PWM*x* output is held high during the pulse, effectively controlling the duty cycle. The value written to PWM*x*_CONTROL register can be from 0 to 255 state times (0% to 99.6% duty cycle). Setting IOC2.2 enables the PWM's divide-by-two clock prescaler; the total length of the pulse is 512 state times and the PWM*x*_CONTROL value is multiplied by 4. Clearing IOC2.2 disables the prescaler; the total pulse length is 256 state times and the PWM*x*_CONTROL value is multiplied by 2. Table 10-1 lists sample output frequencies.

Table 10-1. PWM Output Frequencies

	XTAL1 Frequency (F_{OSC})			
IOC2.2	**8 MHz**	**10 MHz**	**16 MHz**	**20 MHz**
0	15.6 KHz	19.6 KHz	31.25 KHz	39.1 KHz
1	7.8 KHz	9.8 KHz	15.63 KHz	19.5 KHz

Use the following formulas to calculate the PWM period and the time that the PWM output is high. Note that PWM*x*_CONTROL is an 8-bit value and F_{OSC} is the XTAL1 frequency, in MHz.

	Clock Prescaler Disabled (IOC2.2=0)	**Clock Prescaler Enabled (IOC2.2=1)**
PWM Period (in µsec.) =	$\frac{512}{F_{OSC}}$	$\frac{1024}{F_{OSC}}$
PWM*x* High (in µsec.) =	$\frac{PWMx\_CONTROL \times 2}{F_{OSC}}$	$\frac{PWMx\_CONTROL \times 4}{F_{OSC}}$

For example, if F_{OSC} equals 16 MHz, then the period of the PWM output waveform is 32 µs. If PWM0_CONTROL equals 8AH (138 decimal) and IOC2.2 is clear, PWM0 is held high for 17.25 µs (and low for 14.8 µs) of the total 32 µs, resulting in a duty cycle of approximately 54%. When IOC2.2 is set, the same values would produce a period of 64 µs and PWM0 would be held high for 34.5 µs (and low for 29.5 µs), for the same duty cycle, approximately 54%.

10.3. ENABLING THE PWM OUTPUTS

Each PWM output is multiplexed with a port pin. Table 10-2 shows the alternate port function along with the register setting that selects the PWM output instead of the port function. Selecting the PWM1 or PWM2 output function disables the quasi-bidirectional Port 1 function and enables strong pull-ups and pull-downs.

Table 10-2. PWM Output Alternate Functions

PWM Output	Alternate Port Function	PWM Output Enabled When:
PWM0	P2.5	IOC1.0 = 1
PWM1	P1.3	IOC3.2 = 1
PWM2	P1.4	IOC3.3 = 1

10.4. GENERATING ANALOG OUTPUTS

Both the PWM modules and the High-Speed Output (HSO) module can generate a rectangular pulse train that varies in duty cycle and period. Filtering this output will create a smooth analog signal. To make a signal swing over the desired analog range, first buffer the signal and then filter it. Figure 10-3 is a block diagram of the type of circuit needed to create the smooth analog signal. Use either a simple RC network or an active filter.

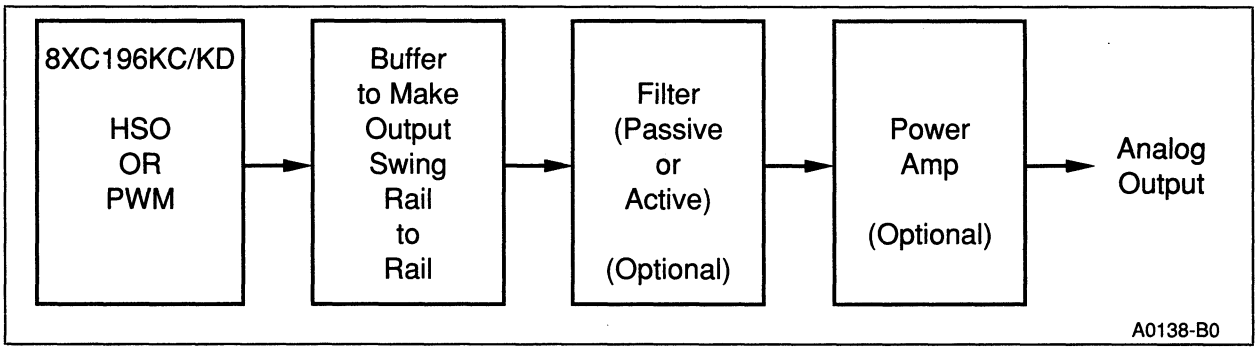

Figure 10-3. D/A Buffer Block Diagram

Figure 10-4 shows a sample circuit used for low output currents (less than 100 µA). Consider temperature and power-supply drift when selecting components for the external D/A circuitry. With proper components, a highly accurate 8-bit D/A converter can be made using either the PWM or HSO outputs. The HSO could theoretically extend the accuracy to sixteen bits, but temperature and noise problems would be difficult to control.

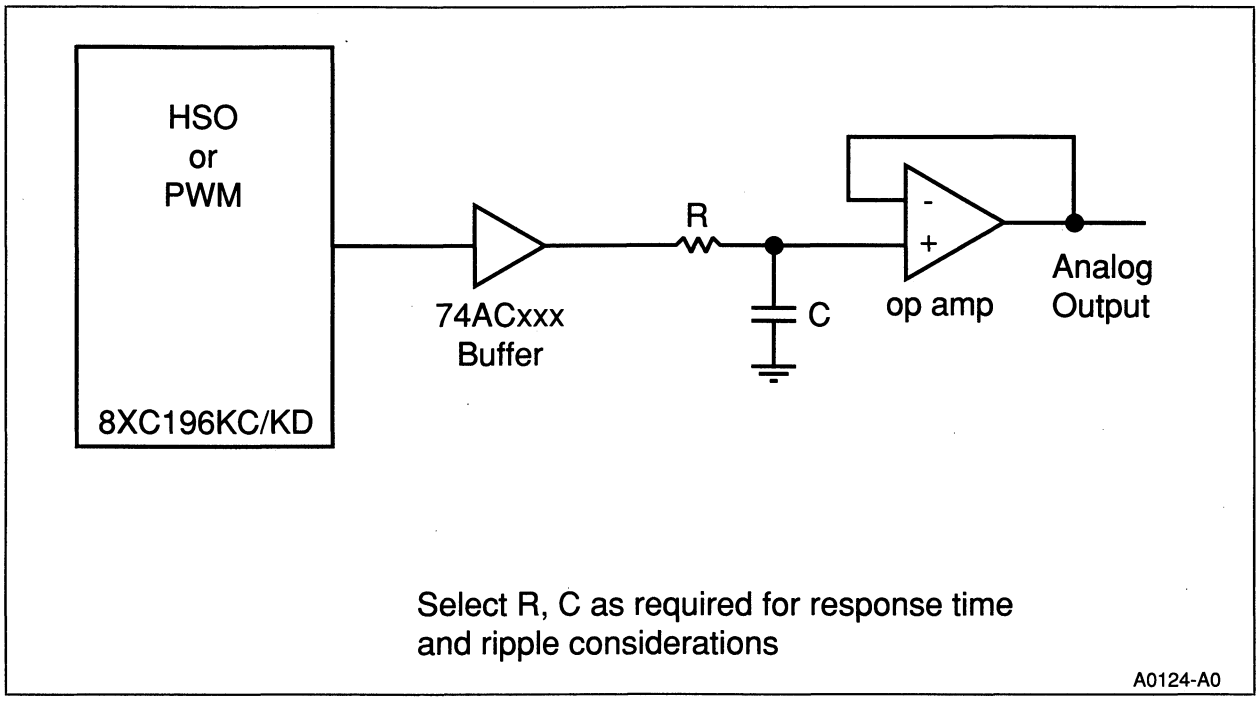

Figure 10-4. PWM to Analog Conversion Circuitry