12 Special Operating Modes

CHAPTER 12
SPECIAL OPERATING MODES

The 8XC196KC/KD supports three special operating modes: Idle, Powerdown, and On-Circuit Emulation (ONCE). Idle and Powerdown modes reduce power consumption; the On-Circuit Emulation (ONCE) mode is a test mode that electrically isolates the chip from the other system components. This chapter provides an overview of each mode and then describes how to enter and exit each mode. (Refer to Appendix A for descriptions of the instructions discussed in this chapter, to Appendix B for information about the signals, and to Appendix C for details about the registers.)

12.1. IDLE MODE

In Idle mode, the CPU clocks are frozen at logic state zero, but the peripheral clocks and CLKOUT remain active. The CPU stops executing instructions, but the internal RAM, timer/counters, serial port, and interrupt system continue functioning. Power consumption is reduced to about 40% of the normal consumption.

The bus-control pins (ALE, RD#, WR#, INST, and BHE#) are driven to their inactive states. If they are being used as I/O ports, Ports 3 and 4 will retain the value present in their data latches. If these ports are being used as the address/data bus, the pins will float.

If enabled, the Watchdog timer continues to run in Idle mode. The device must be awakened within every 64K state times to clear the WATCHDOG (0AH) register or the timer will reset the device.

12.1.1. Entering Idle Mode

To enter Idle mode, execute the IDLPD #1 instruction.

12.1.2. Exiting Idle Mode

Either an interrupt or a hardware reset will bring the device out of Idle mode. Because all peripherals remain active in Idle mode, any enabled interrupt source can generate the interrupt. When an interrupt occurs, the CPU exits Idle mode and begins executing the corresponding interrupt service routine. After completing the interrupt service routine, the CPU fetches and then executes the instruction that follows the IDLPD #1 instruction.

12.2. POWERDOWN MODE

Powerdown mode places the 8XC196KC/KD into a very low power state. If V_{CC} is maintained, the Special Function Registers (SFRs) and register RAM retain their data. All peripherals are powered down, all internal clocks are frozen at logic state zero, and the oscillator is shut off. Power consumption drops into the microwatt range (refer to the data sheet for exact specifications). I_{CC} is reduced to device leakage.

During Powerdown, the internal oscillator and clock generator are disabled. The bus-control pins (ALE, RD#, WR#, INST, and BHE#) are driven to their inactive states. All of the output pins hold the values in their data latches. If ports 3 and 4 were being used as I/O ports (EA# = 0), their pins will hold the last output value. If ports 3 and 4 were being used as an address/data bus (EA# = 1), their pins will float.

Figure 12-1 is a simplified drawing of the internal powerdown circuitry. Table 12-1 describes the internal signals shown in the figure. The IDLPD #2 instruction sets Q1, turning off the internal phase clocks, and clears Q2, turning off the internal oscillator.

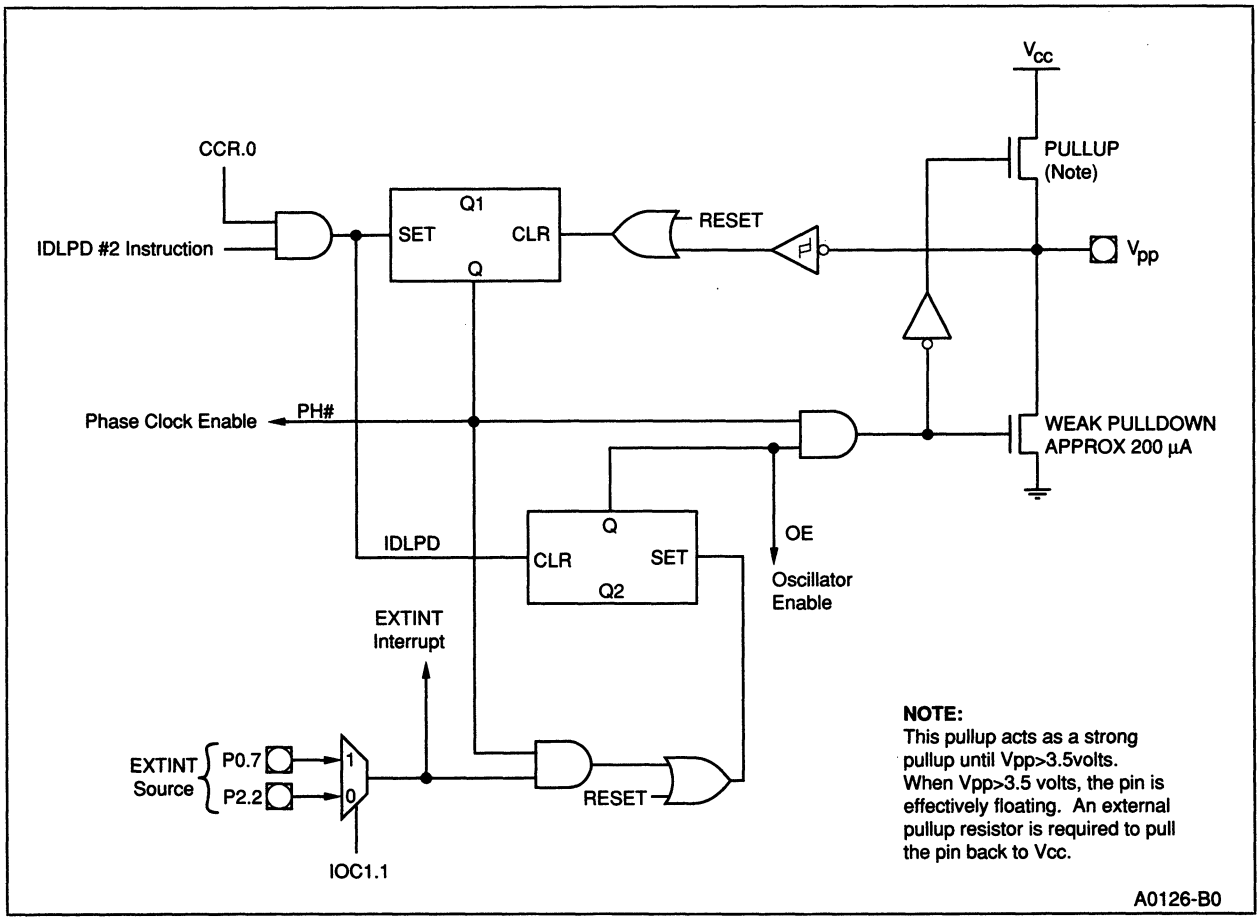

Figure 12-1. Simplified Powerdown Circuit

Table 12-1. Internal Powerdown Signals

Signal Name	Description
IDLPD	Idle/Powerdown. This signal causes the device to enter the Powerdown mode. It disables the phase clock enable (PH#) and oscillator enable (OE) signals. The IDPLD #2 instruction generates this signal.
OE	Oscillator Enable. This signal enables the oscillator during normal operating mode. During Powerdown, it disables the internal oscillator.
PH#	Phase Clock Enable. This signal enables the internal phase clocks during normal operation. During Powerdown, it disables the internal phase clocks.
RESET	Internal Reset. This signal is an inverted version of the external RESET# signal.

12.2.1. Disabling Powerdown Mode

The Powerdown mode is disabled when the PD bit (CCR.0) is cleared. The CCR is loaded from the Chip Configuration Byte (location 2018H) when the device is reset.

12.2.2. Entering Powerdown Mode

Before entering Powerdown, complete the following tasks:

- Complete all serial port transmissions or receptions. When the device exits Powerdown, the serial port activity will continue where it left off and incorrect data may be transferred or received.
- Complete all analog conversions. If Powerdown occurs during the conversion, the result will be incorrect.
- If the Watchdog timer (WDT) is enabled, clear the WATCHDOG register just before issuing the Powerdown instruction. This ensures that the device can exit Powerdown cleanly. Otherwise, the WDT could reset the 8XC196KC/KD before the oscillator stabilizes. (The WDT cannot reset the device during Powerdown because the clock is stopped.)

Upon completion of these tasks, execute the IDLPD #2 instruction to enter Powerdown mode. The IDLPD #2 instruction sets Q1, turning off the internal phase clocks, and clears Q2, turning off the internal oscillator (see Figure 12-1).

NOTE

The EXTINT pin must be held low while the device is in Powerdown.

12.2.3. Exiting Powerdown Mode

Powerdown is exited by driving the V_{PP} pin low or by asserting either the RESET# or the EXTINT signal.

12.2.3.1. DRIVING V_{PP} LOW

The fastest way to exit Powerdown mode is to drive the V_{PP} pin low for at least 50 ns. This clears Q1 (see Figure 12-1), which enables the internal phase clocks, but it does not set Q2. The internal oscillator remains disabled, so use this method only when an external clock provides the clock signal.

12.2.3.2. ASSERTING RESET#

Another way to exit Powerdown mode is to assert the RESET# signal. RESET# must be held low until the oscillator has stabilized. The oscillator design must be characterized to determine how long it takes to stabilize. When using an external clock, RESET# must remain low for at least one state time. When RESET# is asserted, the internal reset signal clears Q1 and sets Q2, immediately enabling both the internal phase clocks and the internal oscillator (see Figure 12-1).

12.2.3.3. ASSERTING EXTINT

The final way to exit Powerdown mode is to assert the EXTINT signal for at least 50 ns. EXTINT is normally a sampled interrupt input. However, the Powerdown circuitry uses it as a level-sensitive input. The EXTINT interrupt need not be enabled for it to bring the device out of Powerdown. The EXTINT_SRC bit (IOC1.1) defines the source of EXTINT. Setting IOC1.1 selects P0.7 as the source; clearing IOC1.1 selects P2.2 as the source. Figure 12-2 shows the power-up and power-down sequence when using EXTINT to exit Powerdown.

If the EXTINT signal will be used to exit from Powerdown mode, we recommend that you connect the external RC circuit shown in Figure 12-3 to the V_{PP} pin. The discharging of the capacitor causes a delay that allows the oscillator to stabilize before the internal phase clocks are enabled.

When an EXTINT signal is received, Q2 is set, which enables the internal oscillator circuitry and turns on the weak pull-down (see Figure 12-1). This weak pull-down causes the external capacitor (C_1) to begin discharging at a typical rate of 100µA to 200 µA. When the V_{PP} voltage drops below the threshold voltage (about 2.5 V), the Schmitt trigger clears Q1, which enables the phase clocks (PH# = 0), and the device resumes code execution.

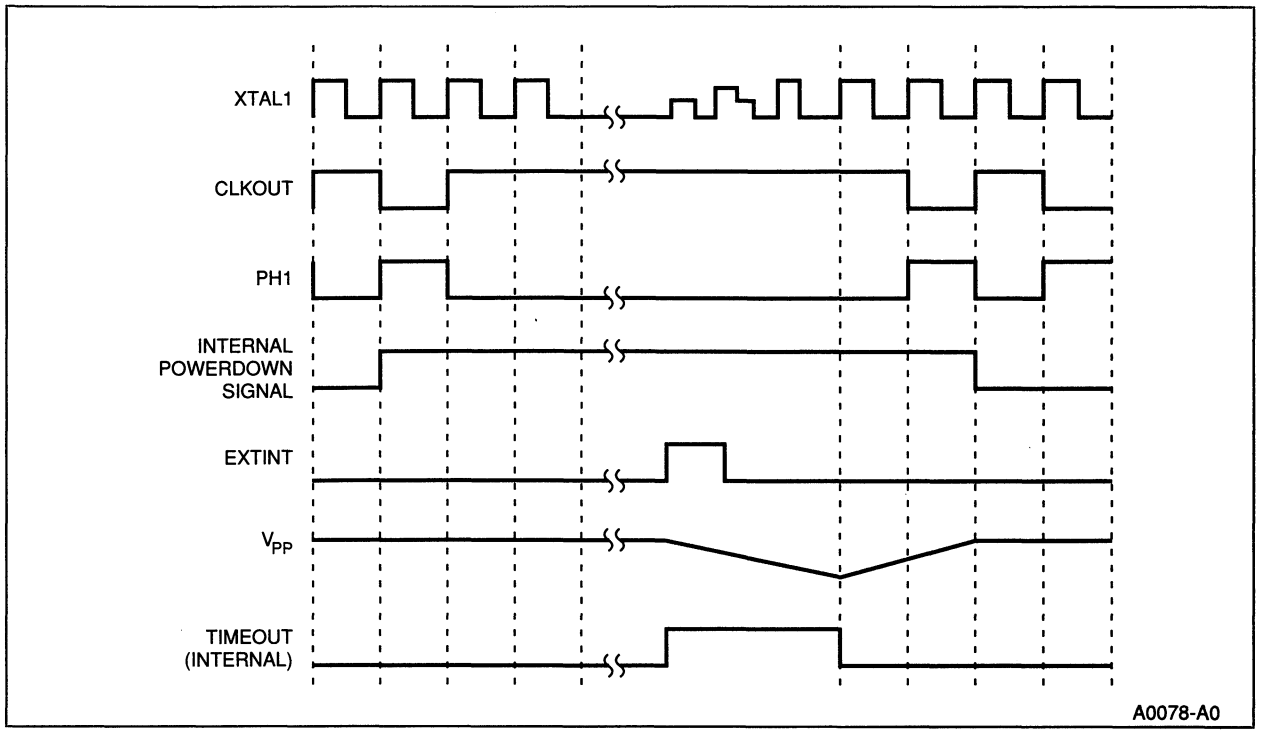

Figure 12-2. Power-Up and Power-Down Sequence

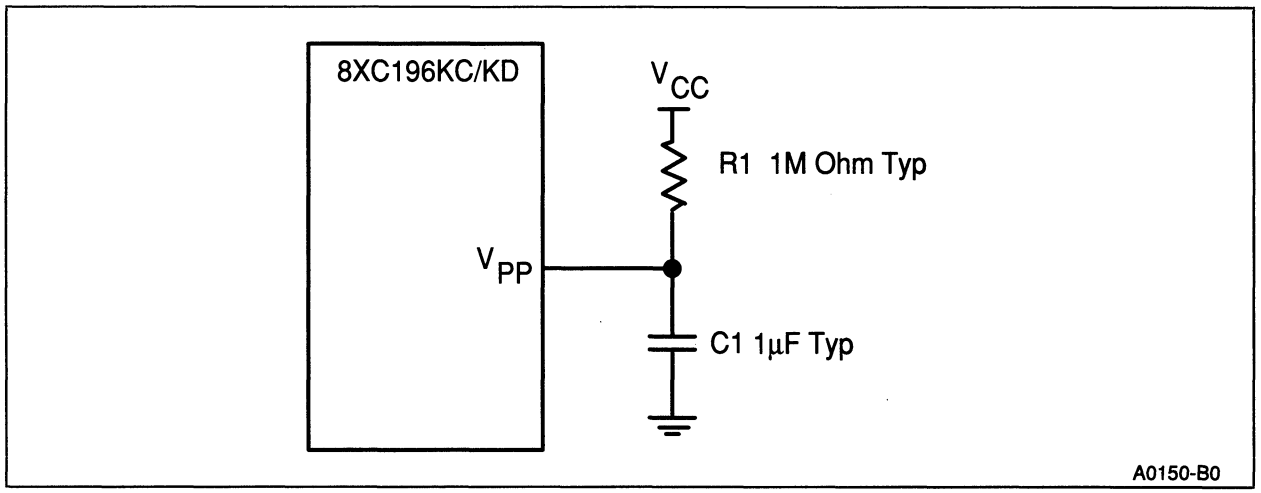

Figure 12-3. V_{PP} External RC Circuit

The pull-up transistor turns on when the V_{PP} voltage drops below the threshold and quickly pulls the pin back up to about 3.5 V. The pull-up becomes ineffective and the external resistor (R_1) takes over and pulls the voltage up to V_{CC} (see recovery time in Figure 12-4). The time constant follows an exponential charging curve; if C_1 = 1 µF and R_1 = 1 MΩ, the recovery time will take several seconds.

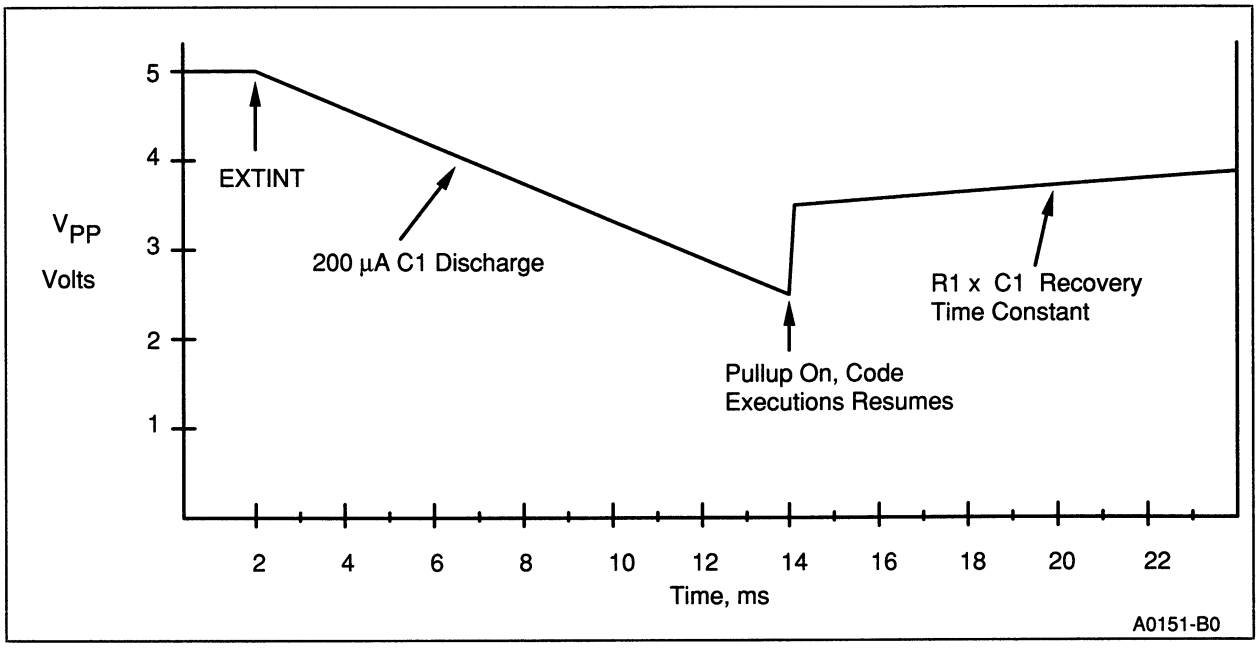

Figure 12-4. Typical V_{PP} Voltage While Exiting Powerdown

12.2.3.3.1. Selecting R_1 and C_1

Select components that produce a sufficient discharge time to permit the internal oscillator circuitry to stabilize. Because many factors can influence the discharge time requirement, you should always fully characterize your design under worst-case conditions to verify proper operation.

Select a resistor that will not interfere with the discharge current. An R_1 value between 200 KΩ and 1 MΩ should perform satisfactorily.

When selecting the capacitor, determine the worst-case discharge time needed for the oscillator to stabilize, then use this formula to calculate an appropriate value for C_1:

$$C_1 = \frac{T_{DIS} \times I}{\Delta V}$$

where:

C_1	is the capacitor value, in Farads
T_{DIS}	is the worst-case discharge time, in seconds
I	is the discharge current, in amperes
ΔV	is the threshold voltage

NOTE

If Powerdown is re-entered and exited before C_1 charges to V_{CC}, it will take less time for the voltage to ramp down to the threshold (because ΔV is less). The device will take less time to exit Powerdown.

For example, assume that the oscillator needs at least 12.5 ms to stabilize (T_{DIS} = 12.5 ms), ΔV is 2.5 V, and the discharge current is 200 µA. The minimum C_1 capacitor size is 1 µF.

$$C_1 = \frac{.0125 \times .0002}{2.5} = 1\ \mu F$$

When using an external oscillator, the value of C1 can be very small, to allow rapid recovery from Powerdown. For example, a 100 pF capacitor discharges in 1.25 µs.

$$T_{DIS} = \frac{C_1 \times \Delta V}{I} = \frac{1.0e-10 \times 2.5}{.0002} = 1.25\ \mu s$$

12.3. ONCE MODE

ONCE mode is a test mode that electrically isolates the 8XC196KC/KD from the other devices on the Printed Circuit Board (PCB). It is the only test mode available to users. ONCE mode is typically used to isolate the 8XC196KC/KD while programming discrete EEPROMs on the circuit board.

All pins, except XTAL1 and XTAL2, have weak pull-ups or pull-downs and are not truly high impedance (see Table B-3 in Appendix B). RESET# must remain high during ONCE. If RESET# is asserted during ONCE, the device will exit ONCE mode and enter the reset state.

12.3.1. Entering ONCE Mode

The ONCE mode is entered if P2.0 is held low during the rising edge of RESET#. The DC specifications for I_{OH1} and I_{IL1} (see the data sheet) define the voltage levels required to place the device into ONCE mode or to ensure that ONCE is not inadvertently activated.

12.3.2. Exiting ONCE Mode

Exit the ONCE Mode by asserting the RESET# signal and allowing P2.0 to float or be pulled high. When RESET# rises, normal operation resumes.

12.4. ENTERING RESERVED TEST MODES

When held high in combination with other pins, PWM0 (P2.5) invokes reserved test modes. To avoid entering the reserved test modes, do not hold PWM0 high during reset.