8XC196KC/KD Signal Descriptions

B

APPENDIX B
8XC196KC/KD SIGNAL DESCRIPTIONS

This appendix provides reference information for the pin functions of the 8XC196KC and 8XC196KD. Table B-1 defines the columns used in Table B-2, which describes the pin functions. Table B-3 shows the reset status of I/O and control pins, and Table B-4 defines the pin status terminology. Tables B-5 and B-6 list package pin numbers along with their corresponding pin functions.

Table B-1. Description of Columns of Table B-2

Column Heading	Description
Function Name	Lists the pin functions, arranged alphabetically. Many pins have more than one function, so there are more entries in this column than there are pins. Every pin function is listed in this column; for each pin function, any additional functions that share the pin are listed in the "Additional Functions" column.
Additional Functions	Lists all other functions that the pin provides.
Selected by	Lists the register setting, pin state, or other condition that causes the function listed in the "Function Name" column to become active. A dash (—) indicates "none" or "not applicable."
Type	Identifies the pin function listed in the "Function Name" column as an input (I), output (O), bidirectional (I/O), quasi-bidirectional (QBD), power (PWR), or ground (GND). Note that all inputs, with the exception of RESET#, are *sampled inputs.* RESET# is a level-sensitive input. During Powerdown mode, the powerdown circuitry uses EXTINT as a level-sensitive input.
Description	Briefly describes the pin function listed in the "Function Name" column.

Table B-2. Signal Descriptions

Function Name	Additional Functions	Selected by	Type	Description
ACH0 ACH1 ACH2 ACH3 ACH4 ACH5 ACH6 ACH7	P0.0 P0.1 P0.2 P0.3 P0.4/PMODE.0 P0.5/PMODE.1 P0.6/PMODE.2 P0.7/PMODE.3	—	I	Analog Channels 0 through 7. ACH0–ACH7 are analog inputs to the A/D converter. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*x*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading Port 0 while a conversion is in process can produce unreliable conversion results. The ANGND and V_{REF} pins must be connected for the A/D converter and Port 0 to function.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
AD0–AD7 AD8–AD15	P3.0–P3.7 P4.0–P4.7	Bus access to external address	I/O	System Address/Data Bus. These pins provide a multiplexed address and data bus. During the address phase of the bus cycle, address bits 0–15 are presented on the bus and can be latched using ALE or ADV#. During the data phase, 8- or 16-bit data is transferred.
ADV#	ALE	CCR.3=0	O	Address Valid. This active-low output signal is asserted only during external memory accesses. ADV# indicates that valid address information is available on the system address/data bus. The signal remains low while a valid bus cycle is in progress and is returned high as soon as the bus cycle completes. The ADV# signal is used by an external latch to demultiplex the address from the address/data bus. ADV# can also be used with a decoder to generate chip-selects for external memory.
AINC#	P2.4/T2RST	EA# = V_{EA} (programming mode)	I	Auto Increment. In Slave Programming Mode, this active-low input signal enables the auto-increment mode. Auto increment allows reading from or writing to sequential EPROM locations without requiring address transactions across the programming bus for each read or write.
ALE	ADV#	CCR.3=1	O	Address Latch Enable. This active-high output signal is asserted only during external memory accesses. ALE indicates that valid address information is available on the system address/data bus and signals the start of a valid bus cycle. ALE differs from ADV# in that it is not returned high until a new bus cycle is to begin. ALE is used by an external latch to demultiplex the address from the address/data bus.
ANGND	—	—	GND	Reference ground for the A/D converter and the logic used to read Port 0. ANGND must be connected for the A/D converter and Port 0 to function.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
BHE#	WRH#	CCR.2=1	O	Byte High Enable. This active-low output signal is asserted only during **word** writes and **high byte** writes to external memory. BHE# indicates that valid data is being transferred (written) over the upper half of the system address/data bus. BHE#, in conjunction with A0, selects the memory byte to be written: **BHE# / A0 / Byte Written** 0 / 0 / both bytes 0 / 1 / high byte only 1 / 0 / low byte only
BREQ#	P1.5	WSR.7=1	O	Bus Request. This active-low output signal is asserted during a HOLD cycle when the bus controller has a pending external memory cycle. The earliest time in the HOLD cycle that the device can assert BREQ# is at the same time it asserts HLDA#. Once it is asserted, BREQ# remains asserted until HOLD# is removed. When this function is active, the pin acts as a standard output (not quasi-bidirectional). Once the alternate function is enabled, the pin functions as BREQ# until the device is reset.
BUSWIDTH	—	CCR.1=1	I	Bus Width. This active-high input signal dynamically selects the bus width. When high, BUSWIDTH selects a 16-bit bus width; when low, it selects an 8-bit bus width. BUSWIDTH is active during a CCR fetch. When CCR.1=0 the bus width is always 8 bits; the BUSWIDTH signal is ignored.
CLKOUT	—	IOC3.1=0 **8XC196KD and 8XC196KC (C-Step) only**	O	Clock Output. Output of the internal clock generator. The CLKOUT frequency is 1/2 the oscillator frequency input (XTAL1) and CLKOUT has a 50% duty cycle. On the 8XC196KD and the 8XC196KC (C-Step), clearing IOC3.1 enables CLKOUT; setting IOC3.1 disables the signal. On earlier versions of the 8XC196KC, CLKOUT cannot be disabled.
CPVER	P2.6/T2UP-DN	EA# = V_{EA} (programming mode)	O	Cumulative Program Verification. This active-high output signal indicates whether any verify errors have occurred since the device entered programming mode. CPVER remains high until a verify error occurs, at which time it is driven low. Once an error occurs, CPVER remains low until the device exits programming mode. When high, CPVER indicates that all locations have programmed correctly since the device entered programming mode.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
EA#	Programming mode select (EA# = V_{EA})	—	I	External Access. This active-low input signal directs memory accesses to on-chip or off-chip memory. When low, it selects off-chip memory; when high, it selects on-chip ROM or EPROM. EA# is sampled **only** on the rising edge of RESET#. EA# = V_{EA} on the rising edge of RESET# causes the device to enter the programming mode selected by PMODE.0–PMODE.3. For ROMless devices, EA# must be tied low.
EXTINT				External Interrupt. IOC1.1 assigns this input to either P2.2 or P0.7. EXTINT must be asserted for greater than two state times to guarantee that it is recognized. In Powerdown mode, EXTINT causes the chip to return to normal operating mode. EXTINT is normally a *sampled input*; however, the powerdown circuitry uses it as a level-sensitive input in Powerdown mode.
	P2.2/PROG#	IOC1.1=0	I	P2.2 always generates EXTINT1 (INT13, 203AH). When IOC1.1=0, a rising edge on the P2.2 pin also generates EXTINT (INT07, 200EH). EXTINT and EXTINT1 must be asserted for greater than two state times to guarantee that they are recognized.
	P0.7/PMODE.3 /ACH7	IOC1.1=1	I	When IOC1.1=1, a rising edge on the P0.7 pin generates external interrupt EXTINT (INT07, 200EH). EXTINT must be asserted for greater than two state times to guarantee that it is recognized.
HLDA#	P1.6	WSR.7=1	O	Bus Hold Acknowledge. This active-low output indicates that the 8XC196KC/KD has released the bus as a result of another device asserting HOLD#. When this function is active, the pin acts as a standard output (not quasi-bidirectional). Once the HLDA# function is enabled, the pin functions as HLDA# until the device is reset.
HOLD#	P1.7	WSR.7=1	I	Bus Hold. This active-low input is used to request control of the bus. When this function is active, the pin acts as a standard input (not quasi-bidirectional). Once the alternate function is enabled, the pin functions as HOLD# until the device is reset.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
HSI.0	INT04 interrupt /T2 reset source	IOC0.0=1	I	Input to the High-Speed Input module. The HSI.0 pin can also be used to generate an interrupt. A rising edge on HSI.0 generates the HSI.0 Pin interrupt (INT04, 2008H). HSI.0 must be asserted for greater than two state times to guarantee that it is recognized. In addition, when IOC0.5=1, a rising edge on HSI.0 resets Timer 2.
HSI.1	T2 clock source	IOC0.2=1	I	Input to the High-Speed Input module. When IOC0.7=0 and IOC3.0=0, the HSI.1 pin functions as the T2 clock source.
HSI.2	HSO.4	IOC0.4=1	I	Input to the High-Speed Input module. Note that HSI and HSO functions can be active at the same time, in which case the pin acts as an output that the HSO monitors.
HSI.3	HSO.5	IOC0.6=1	I	Input to the High-Speed Input module. Note that HSI and HSO functions can be active at the same time, in which case the pin acts as an output that the HSO monitors.
HSO.0 HSO.1 HSO.2 HSO.3	— — — —	— — — —	O	Outputs from the High-Speed Output module.
HSO.4	HSI.2	IOC1.4=1	O	Output from the High-Speed Output module. Note that the HSI and HSO functions can be active at the same time, in which case the pin acts as an output that the HSO monitors.
HSO.5	HSI.3	IOC1.6=1	O	Output from the High-Speed Output module. Note that the HSI and HSO functions can be active at the same time, in which case the pin acts as an output that the HSI monitors.
INST	—	—	O	Instruction Fetch. This signal is valid only during external memory read cycles. When high, INST indicates that an instruction is being fetched; when low, it indicates that data is being read. INST can be used in applications that require separate memory banks for instructions and data. (Note that CCB bytes and interrupt vectors are considered **data**.)
NMI	—	—	I	Nonmaskable Interrupt. A positive transition causes a vector through the NMI interrupt at location 203EH. NMI must be asserted for greater than one state time to guarantee that it is recognized. NMI is used by Intel tools that could conflict with user software. When NMI is not used, it should be tied low.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	ACH0 ACH1 ACH2 ACH3 ACH4/PMODE.0 ACH5/PMODE.1 ACH6/PMODE.2 ACH7/PMODE.3 /EXTINT	—	I	Port 0. This port is an 8-bit, high-impedance, input-only port. Port 0 is read (only) at location 0EH in HWindow 0. P0.0–P0.7 are digital inputs. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*x*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading Port 0 while a conversion is in process can produce unreliable conversion results. ANGND and V_{REF} must be connected for Port 0 and the A/D converter to function.
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	— — — PWM1 PWM2 BREQ# HLDA# HOLD#	— — — IOC3.2=0 IOC3.3=0 WSR.7=0 WSR.7=0 WSR.7=0	QBD	Port 1. This port is an 8-bit, quasi-bidirectional input/output port. Port 1 is read and written at location 0FH in HWindow 0. The additional functions act as standard I/O pins (not quasi-bidirectional).
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	TXD/PVER# RXD/PALE# EXTINT/PROG# T2CLK T2RST/AINC# PWM0 T2UP-DN/CPVER T2CAPTURE /PACT	IOC1.5=0 SPCON.3=0 — — — IOC1.0=0 — —	O I I I I O QBD QBD	Port 2. This port is an 8-bit, multifunctional port. Port 2 is read and written at location 10H in HWindow 0.
P3.0–P3.7 P4.0–P4.7	AD0–AD7 AD8–AD15	EA#=1	I/O	Ports 3 and 4. These are 8-bit, bidirectional, input/output ports with open-drain outputs. The pins are shared with the multiplexed address/data bus, which has strong internal pull-ups. Ports 3 and 4 can be read and written only as a word, at location 1FFEH. During Programming Modes, these ports function as the PBUS.
PACT#	P2.7 /T2CAPTURE	EA# = V_{EA} (programming mode)	O	Programming Active. In Auto Programming Mode, PACT# low indicates that programming activity is occurring.
PALE#	P2.1/RXD	EA# = V_{EA} (programming mode)	I	Programming ALE. When PALE# is asserted, data and commands on Ports 3 and 4 are read into the device.
PMODE.0 PMODE.1 PMODE.2 PMODE.3	P0.4/ACH4 P0.5/ACH5 P0.6/ACH6 P0.7/ACH7	EA# = V_{EA} (programming mode)	I	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a device reset when EA# = V_{EA} and must be stable while the device is operating.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
PROG#	P2.2/EXTINT	EA# = V_{EA} (programming mode)	I	Programming Start. This active-low input is valid only in Slave Programming Mode. When asserted, PROG# causes the data on the programming bus to be programmed into the EPROM. When PROG# is deasserted, the programming pulse is terminated.
PVER	P2.0/TXD	EA# = V_{EA} (programming mode)	O	Program Verification. In Programming Modes, this active-high output signal is asserted to indicate that the word has programmed correctly.
PWM0	P2.5	IOC1.0=1	O	Pulse Width Modulator (PWM) Output 0. If PWM0 is forced high on the rising edge of RESET#, the device enters Test Mode.
PWM1	P1.3	IOC3.2=1	O	PWM Output 1.
PWM2	P1.4	IOC3.3=1	O	PWM Output 2.
RD#	—	—	O	Read signal output to external memory. RD# is asserted only during external memory reads.
READY	—	—	I	Ready input. This signal is used to lengthen external memory cycles by generating "wait states" for interfacing to slow memory. When READY is high, CPU operation continues in a normal manner. If READY is low prior to the falling edge of CLKOUT, the memory controller inserts wait states until the next positive transition in CLKOUT occurs with READY high or until the number of wait states is equal to the number programmed into CCR.4 and CCR.5. READY is ignored for all internal memory accesses. READY is active during a CCR fetch.
RESET#	—	—	I/O	Reset input to and open-drain output from the chip. A falling edge on RESET# initiates the reset process. When RESET# is first asserted, the chip turns on a pull-down transistor connected to the RESET pin for 16 state times. This function can also be activated by a watchdog timer overflow or by execution of the RST instruction. In Powerdown mode, the reset process causes the chip to return to normal operating mode.
RXD	P2.1/PALE#	SPCON.3 = 1	I/O	Receive Serial Data. In modes 1, 2, and 3, RXD is used to receive serial port data. In mode 0, it functions as an input or an open-drain output for data.
T2CAPTURE	P2.7/PACT#	—	QBD	A rising edge on P2.7 captures the value of Timer 2 in the T2CAPTURE register and triggers a Timer 2 Capture interrupt (INT11, 2036H). T2CAPTURE must be asserted for greater than two state times to guarantee that it is recognized.

Table B-2. Signal Descriptions (Continued)

Function Name	Additional Functions	Selected by	Type	Description
T2CLK	P2.3	IOC0.7=0 and IOC3.0=0	I	Timer 2 clock input and
		BAUD_RATE. 15 = 0	I	Serial port baud rate generator input.
T2RST	P2.4/AINC#	IOC0.3=1 and IOC0.5=0	I	Timer 2 Reset. A rising edge on T2RST resets Timer 2.
T2UP-DN	P2.6 /CPVER	IOC2.1=1	I	Timer 2 Up/Down Control. This active-high input controls the direction of the Timer 2 counter. When T2UP-DN is high, Timer 2 counts down; when T2UP-DN is low, Timer 2 counts up.
TXD	P2.0/PVER	IOC1.5=1	O	Transmit Serial Data. In modes 1, 2, and 3, TXD is used to transmit serial port data. In mode 0, it is used as the serial clock output. Holding TXD low on the rising edge of RESET# causes the device to enter ONCE mode.
V_{CC}	—	—	PWR	Digital supply voltage (+5 volts).
V_{PP}	—	—	PWR	Programming voltage. Also the timing pin for the "return from power-down" circuit.
V_{REF}	—	—	PWR	Reference voltage for the A/D converter. V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. V_{REF} must be connected for the A/D and Port 0 to function.
V_{SS}	—	—	GND	Digital circuit ground (0 volts). There are multiple Vss pins, all of which must be connected.
WR#	WRL#	CCR.2=1	O	Write. This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes.
WRH#	BHE#	CCR.2=0	O	Write High. During 16-bit bus cycles, this active-low output signal is asserted during high byte writes and word writes. During 8-bit bus cycles, WRH# is asserted for all write operations.
WRL#	WR#	CCR.2=0	O	Write Low. During 16-bit bus cycles, this active-low output signal is asserted during low byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations.
XTAL1	—	—	I	Input of the on-chip oscillator inverter and of the internal clock generator. If an external oscillator is used, XTAL1 also serves as the 8XC196KC/KD clock input (the XTAL1 V_{IH} specification must be met.)
XTAL2	—	—	O	Output of the on-chip oscillator inverter.

Table B-3 lists the default functions of the 8XC196KC/KD I/O and control pins with their values during and after reset. Table B-4 defines the pin status terminology.

Table B-3. Pin Reset Status

Pin Name	Multiplexed Port Pins	Pin Status During Reset	Pin Status After Reset
ACH0–ACH7	P0.0–P0.7	Undefined Inputs (Note 1)	Undefined Inputs (Note 1)
PORT1	P1.0–P1.7	Weak Pull-ups (I_{IL} spec)	Weak Pull-ups (I_{IL} spec)
TXD	P2.0	Strong Pull-up (I_{LI1} spec)	Strongly Driven
RXD	P2.1	Undefined Input (Note 3)	Undefined Input (Note 3)
EXTINT	P2.2	Undefined Input (Note 3)	Undefined Input (Note 3)
T2CLK	P2.3	Undefined Input (Note 3)	Undefined Input (Note 3)
T2RST	P2.4	Undefined Input (Note 3)	Undefined Input (Note 3)
PWM0	P2.5	Medium Pull-down	Strongly Driven
—	P2.6–P2.7	Weak Pull-ups	Weak Pull-ups
AD0–AD15	P3.0–P4.7	Weak Pull-ups	Address/Data Bus or Open-Drain I/O (Note 2)
HSI.0, HSI.1	—	Undefined Input (Note 3)	Undefined Input (Note 3)
HSI.2/HSO.4	—	Undefined Input (Note 3)	Undefined Input (Note 3)
HSI.3/HSO.5	—	Undefined Input (Note 3)	Undefined Input (Note 3)
HSO.0–HSO.3	—	Weak Pull-down	Weak Pull-down
ALE	—	Weak Pull-up	Strongly Driven
BHE#	—	Weak Pull-up	Strongly Driven
BUSWIDTH	—	Undefined Input (Note 3)	Undefined Input (Note 3)
CLKOUT	—	CLKOUT (Strongly Driven)	CLKOUT (Strongly Driven)
EA#	—	Undefined Input (Note 3)	Undefined Input (Note 3)
INST	—	Weak Pull-down	Strongly Driven
NMI	—	Weak Pull-down (I_{IH1} spec)	Weak Pull-down (I_{IH1} spec)
RD#	—	Weak Pull-up	Strongly Driven
READY	—	Undefined Input (Note 3)	Undefined Input (Note 3)
RESET#	—	Medium Pull-up (R_{RST} spec)	Medium Pull-up (R_{RST} spec)
WR#	—	Weak Pull-up	Strongly Driven

NOTES:

1. These pins are allowed to float. However, it is recommended that unused pins be tied high or low.
2. The state of these pins depends on device configuration. If the address/data bus is active, the pins act as a strongly driven bus; otherwise, they act as an open-drain I/O port and are left floating.
3. These pins must be driven and not left floating. Input voltage must **not** exceed V_{CC} during power-up.
4. Consult the 8XC196KC/KD data sheet for specifications.

Table B-4. Pin Status Descriptions

Pin Status	Approximate Value
Weak Pull-up	70 µA
Medium Pull-up	1 mA
Strong Pull-up	12 mA
Weak Pull-down	200 µA
Medium Pull-down	1 mA
Strongly Driven High	see V_{OH} specification
Strongly Driven Low	see V_{OL} specification

NOTE:

These typical maximum values are approximate; they are provided for reference only and are not guaranteed.

Table B-5. 8XC196KC/KD 68-Lead PLCC Package Pin Assignments

Pin No.	Pin Function(s)
1	V_{CC}
2	EA#
3	NMI
4	P0.3/ACH3
5	P0.1/ACH1
6	P0.0/ACH0
7	P0.2/ACH2
8	P0.6/ACH6/PMODE.2
9	P0.7/ACH7/PMODE.3/EXTINT
10	P0.5/ACH5/PMODE.1
11	P0.4/ACH4/PMODE.0
12	ANGND
13	V_{REF}
14	V_{SS}
15	P2.2/EXTINT/PROG#
16	RESET#
17	P2.1/RXD/PALE#
18	P2.0/TXD/PVER
19	P1.0
20	P1.1
21	P1.2
22	P1.3/PWM1
23	P1.4/PWM2
24	HSI.0
25	HSI.1
26	HSI.2/HSO.4
27	HSI.3/HSO.5
28	HSO.0
29	HSO.1
30	P1.5/BREQ#
31	P1.6/HLDA#
32	P1.7/HOLD#
33	P2.6/T2UP-DN/CPVER
34	HSO.2

Pin No.	Pin Function(s)
35	HSO.3
36	V_{SS}
37	V_{PP}
38	P2.7/T2CAPTURE/PACT#
39	P2.5/PWM0
40	WR#/WRL#
41	BHE#/WRH#
42	P2.4/T2RST/AINC#
43	READY
44	P2.3/T2CLK
45	P4.7/AD15
46	P4.6/AD14
47	P4.5/AD13
48	P4.4/AD12
49	P4.3/AD11
50	P4.2/AD10
51	P4.1/AD9
52	P4.0/AD8
53	P3.7/AD7
54	P3.6/AD6
55	P3.5/AD5
56	P3.4/AD4
57	P3.3/AD3
58	P3.2/AD2
59	P3.1/AD1
60	P3.0/AD0
61	RD#
62	ALE/ADV#
63	INST
64	BUSWIDTH
65	CLKOUT
66	XTAL2
67	XTAL1
68	V_{SS}

Table B-6. 8XC196KC/KD 80-Lead QFP Package Pin Assignments

Pin No.	Pin Function(s)
1	P3.1/AD1
2	P3.0/AD0
3	RD#
4	ALE/ADV#
5	INST
6	BUSWIDTH
7	CLKOUT
8	XTAL2
9	XTAL1
10	V_{SS}
11	V_{SS}
12	V_{CC}
13	V_{CC}
14	EA#
15	NMI
16	P0.3/ACH3
17	P0.1/ACH1
18	P0.0/ACH0
19	P0.2/ACH2
20	P0.6/ACH6/PMODE.2
21	P0.7/ACH7/PMODE.3/EXTINT
22	No Connection
23	P0.5/ACH5/PMODE.1
24	P0.4/ACH4/PMODE.0
25	ANGND
26	V_{REF}
27	V_{SS}
28	P2.2/EXTINT/PROG#
29	V_{CC}
30	RESET#
31	P2.1/RXD/PALE#
32	P2.0/TXD/PVER
33	V_{SS}
34	P1.0
35	P1.1
36	P1.2
37	P1.3/PWM1
38	P1.4/PWM2
39	HSI.0
40	HSI.1

Pin No.	Pin Function(s)
41	HSI.2/HSO.4
42	V_{SS}
43	HSI.3/HSO.5
44	HSO.0
45	HSO.1
46	P1.5/BREQ#
47	P1.6/HLDA#
48	P1.7/HOLD#
49	P2.6/T2UP-DN/CPVER
50	HSO.2
51	V_{SS}
52	V_{CC}
53	HSO.3
54	V_{SS}
55	V_{SS}
56	V_{PP}
57	P2.7/T2CAPTURE/PACT#
58	P2.5/PWM0
59	WR#/WRL#
60	BHE#/WRH#
61	P2.4/T2RST/AINC#
62	READY
63	V_{SS}
64	P2.3/T2CLK
65	P4.7/AD15
66	P4.6/AD14
67	P4.5/AD13
68	P4.4/AD12
69	P4.3/AD11
70	P4.2/AD10
71	P4.1/AD9
72	P4.0/AD8
73	P3.7/AD7
74	P3.6/AD6
75	V_{CC}
76	P3.5/AD5
77	P3.4/AD4
78	P3.3/AD3
79	V_{SS}
80	P3.2/AD2