GLOSSARY

This glossary defines acronyms, abbreviations, and terms that have special meaning in this manual. (Chapter 1 discusses notational conventions and general terminology.)

Absolute Error — The maximum difference between corresponding actual and ideal code transitions. *Absolute error* accounts for all deviations of an actual A/D converter from an ideal converter.

Accumulator — A register or storage location that forms the result of an arithmetic or logic operations. The *RALU* performs most calculations, but it does not use an accumulator. Instead, it operates directly on the lower Register File, which essentially provides 256 accumulators. Because data does not flow through a single accumulator, code executes faster and more efficiently.

Actual Characteristic — A graph of output code versus input voltage of an actual A/D converter. An *actual characteristic* may vary with temperature, supply voltage, and frequency conditions.

A/D Converter — Analog-to-digital converter.

ALU — Arithmetic-Logic Unit. The part of the CPU that processes arithmetic and logical operations.

Assert — The term *assert* refers to the act of making a signal active (enabled). The polarity (high/low) is defined by the signal name. Active-low signals are designated by a pound symbol (#) suffix; active-high signals have no suffix. To *assert* RD# is to drive it low; to *assert* ALE is to drive it high.

Attenuation — A decrease in amplitude; voltage decay.

Bit — A binary digit.

BIT — A single-bit operand that can take on the Boolean values, "true" and "false."

Break-Before-Make — The property of a multiplexer which guarantees that a previously selected channel is deselected before a new channel is selected. (That is, *break-before-make* ensures that the A/D converter will not short inputs together.)

Byte	Any 8-bit unit of data.
BYTE	An unsigned, 8-bit variable with values from 0 through 255.
CAM	See *HSO CAM*.
CCB	Chip Configuration Byte, which is loaded into the Chip Configuration Register (CCR) unless the device is entering programming modes, in which case the *PCCB* is used.
Channel-to-Channel Matching Error	The difference between corresponding code transitions of *actual characteristics* taken from different channels under the same temperature, voltage, and frequency conditions. This error is caused by differences in DC leakage current and on-channel resistance from one multiplexer channel to another.
Characteristic	A graph of output code versus input voltage; the *transfer function* of the A/D converter.
Clear	The term *clear* refers to the value of a bit or the act of giving it a value. If a bit is *clear,* its value is "0"; *clearing* a bit gives it a "0" value.
Code	The digital value output by the A/D converter.
Code Center	The voltage corresponding to the midpoint between two adjacent code transitions on the A/D converter.
Code Transition	The point at which the A/D converter output code changes from "Q" to "Q+1." The input voltage corresponding to a code transition is defined as the voltage that is equally likely to produce either of two adjacent codes.
Code Width	The voltage change corresponding to the difference between two adjacent *code transitions*. Code width deviations cause *differential non-linearity* and *non-linearity* errors.
Crosstalk	See *Off-isolation*.
DC Input Leakage	Leakage current to ground from an analog input pin.

Deassert

The term *deassert* refers to the act of making a signal inactive (disabled). The polarity (high/low) is defined by the signal name. Active-low signals are designated by a pound symbol (#) suffix; active-high signals have no suffix. To *deassert* RD# is to drive it high; to *deassert* ALE is to drive it low.

Differential Non-Linearity

The difference between the actual *code width* and the ideal one-LSB code width of the *terminal-based characteristic* of an A/D converter. It provides a measure of how much the input voltage may have changed in order to produce a one-count change in the conversion result. *Differential non-linearity* is a measure of local code-width error; *non-linearity* is a measure of overall code-transition error.

Doping

The process of introducing a periodic table Group III or Group V element into a Group IV element (e.g., silicon). A Group III impurity (e.g., indium or gallium) results in a *p-type* material. A Group V impurity (e.g., arsenic or antimony) results in an *n-type* material.

Double-Word

Any 32-bit unit of data.

DOUBLE-WORD

An unsigned, 32-bit variable with values from 0 through 4,294,967,295.

ESD

Electrostatic discharge.

Event

See *HSI Event* and *HSO Event.*

Feedthrough

The attenuation from an input voltage on the selected channel to the A/D output after the *sample window* closes. The ability of the A/D converter to reject an input on its selected channel after the *sample window* closes.

FET

Field-effect transistor.

FIFO

See *HSI FIFO.*

Full-Scale Error

The difference between the ideal and actual input voltage corresponding to the final (full-scale) code transition.

Hold Latency

The time it takes the 8XC196KC/KD to assert HLDA# after the external device asserts HOLD#.

Horizontal Windowing — The mapping of a 24-byte window of RAM into the lowest 24 bytes of the lower Register File, allowing access to the Special Function Registers (SFRs). The RALU has direct control of all peripheral modules, except Ports 3 and 4, through the SFRs.

HSI — High-Speed Input module. The 8XC196KC/KD module that can record times of external events.

HSI Event — An occurrence on one of the HSI pins (HSI.0–HSI.3) that causes the HSI module to capture information and store it in the *HSI FIFO*. An *HSI event* can be eight positive transitions, each positive transition, each negative transition, or every positive and every negative transition.

HSI FIFO — The HSI's First-In-First-Out file. The portion of the HSI that stores the Timer 1 value and the associated event status bits when an *HSI event* occurs.

HSIO — High-Speed Input/Output unit. The timer/counter-based I/O system that consists of four individual modules: Timer 1, Timer 2, HSI, and HSO.

HSO — High-Speed Output module. The 8XC196KC/KD module that can trigger programmable events at specified times. The HSO can also be used to generate analog outputs, as can the three *PWM*s.

HSO CAM — The HSO's Content-Addressable Memory file. The portion of the HSO that stores commands to be executed and the associated time tags.

HSO Event — An occurrence that the HSO module is programmed to trigger at a specific time. Of the 15 programmable *HSO events*, the 9 that toggle one or more of the HSO pins are called *external events*, and the remaining 6 that program software timers 0–3, reset Timer 2, and start an A/D conversion are called *internal events*. The HSO module can be programmed to generate the High-Speed Output interrupt as the result of an *external event* and the Software Timer interrupt as the result of an *internal event*.

HWindow — Horizontal window. HWindows 0, 1, and 15 are implemented on the 8XC196KC/KD. Each HWindow provides access to a unique set of SFRs.

Ideal Characteristic

A graph of output code versus input voltage of an ideal A/D converter. The *ideal characteristic* possesses unique features: its first code transition occurs when the input voltage is 0.5 LSB; its full-scale (final) code transition occurs when the input voltage equals the full-scale reference minus 1.5 LSB; and its code widths are all exactly one LSB. These properties result in a conversion without zero offset, full-scale, or linearity errors. *Quantizing error* is the only error seen in an ideal A/D converter.

Input Leakage

Current leakage from an analog input pin to ground.

Input Series Resistance

The effective series resistance from the analog input pin to the sample capacitor.

Integer

Any member of the set consisting of the positive and negative whole numbers and zero.

INTEGER

A 16-bit, signed variable with values from –32,768 through +32,767.

Interrupt Controller

The module responsible for handling interrupts that are to be serviced by user-written interrupt service routines. Also called the *Programmable Interrupt Controller (PIC).*

Interrupt Latency

The total delay between the time that an interrupt is generated (not acknowledged) and the time that the 8XC196KC/KD begins executing the interrupt service routine or PTS cycle.

Interrupt Service Routine

The software routine that services a standard interrupt.

LONG-INTEGER

A 32-bit, signed variable with values from –2,147,483,648 through +2,147,483,647.

LSB

Least-significant bit of a byte or least-significant byte of a word.

For A/D conversions, the voltage value corresponding to the full-scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For a 10-bit converter with a reference voltage of 5.12 V, one LSB is 5.0 mV. Note that this differs from digital LSBs. When referring to an A/D converter, an uncertainty of two LSBs equals 10 mV. (This has

	been confused with an uncertainty of two digital bits, which would mean four counts, or 20 mV.)
Maskable Interrupts	All 8XC196KC/KD interrupts except Unimplemented Opcode, Software Trap, and NMI. *Maskable interrupts* can be disabled (masked) by the individual mask bits in the interrupt mask registers, and their servicing can be disabled by the global interrupt enable bit. Each *maskable interrupt* can be assigned to the PTS for processing.
Monotonic	The property of successive-approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value. (In other words, a converter is monotonic if every code change represents an input voltage change in the same direction.) Large *differential non-linearity* errors can cause the converter to exhibit non-monotonic behavior.
MSB	Most-significant bit of a byte or most-significant byte of a word.
***n*-Channel FET**	A field-effect transistor with an *n*-type conducting path (channel).
***n*-Type Material**	Semiconductor material with introduced impurities (*doping*) causing it to have an excess of negatively charged carriers.
No Missing Codes	An A/D converter has *no missing codes* if, for every output code, there exists a unique input voltage range which produces that code only. Large *differential non-linearity* errors can cause the converter to miss codes.
Non-Linearity	The maximum deviation of *code transitions* of the *terminal-based characteristic* from the corresponding code transitions of the *ideal characteristic*.
Nonmaskable Interrupts	Interrupts that cannot be masked (disabled) and cannot be assigned to the PTS for processing. The *nonmaskable interrupts* are Unimplemented Opcode, Software Trap, and NMI.
***npn* Transistor**	A transistor consisting of one part *p*-type material and two parts *n*-type material.

Off-Isolation	The attenuation from a deselected input to the A/D output. The ability of an A/D converter to reject (isolate) the signal on a deselected (off) input.
OTPROM	One-Time-Programmable Read-Only Memory, a version of EPROM.
***p*-Channel FET**	A field-effect transistor with a *p*-type conducting path.
***p*-Type Material**	Semiconductor material with introduced impurities (*doping*) causing it to have an excess of positively charged carriers.
PC	Program Counter.
PCCB	Programming Chip Configuration Byte, which is loaded into the Chip Configuration Register (CCR) when the device is entering programming modes; otherwise, the *CCB* is used.
PIC	Programmable Interrupt Controller. The module responsible for handling interrupts that are to be serviced by user-written interrupt service routines. Also called simply the *Interrupt Controller*.
Prioritized Interrupt	Any of the fifteen *maskable interrupts* or the *non-maskable* NMI. Two of the *nonmaskable interrupts* (Unimplemented Opcode and Software Trap) are not prioritized; they go directly to the Interrupt Controller for servicing.
PSW	Program Status Word. The PSW contains one bit that globally enables or disables servicing of all maskable interrupts, one bit that enables or disables the *PTS*, and six Boolean flags that reflect the state of the user's program.
PTS	Peripheral Transaction Server, the 8XC196KC/KD's microcoded hardware interrupt processor.
PTSCB	PTS Control Block. A block of data required for each PTS interrupt. The microcode executes the proper *PTS cycle* based on the contents of the PTSCB.

PTS Cycle

The PTS microcode equivalent of an interrupt service routine. It is the complete microcoded response to a *single* PTS interrupt. In Single Transfer mode, each byte or word transfer is a *PTS cycle*. In Block Transfer mode, each byte or word transfer is called a *PTS transfer*, while the entire block transfer is called a *PTS cycle*.

PTS Interrupt

Any *maskable interrupt* that is assigned to the PTS for interrupt processing.

PTS Mode

A microcoded response that enables the PTS to quickly complete a specific task. These tasks include single byte/word transfers, block byte/word transfers, multiple A/D conversions, HSI FIFO dumps, and HSO CAM loads.

PTS Transfer

The movement of a single byte or word from the source memory location to the destination memory location. In Single Transfer mode, a *PTS transfer* constitutes a *PTS cycle*, since only one transfer is to occur in the PTS cycle. In Block Transfer mode, the movement of each byte or word within the block is a *PTS transfer*; the movement of the entire block is a *PTS cycle*.

PWM

Pulse Width Modulator. The 8XC196KC/KD has three PWMs and an *HSO* module, all of which can be used to generate analog outputs.

Quantizing Error

An unavoidable A/D conversion error that results simply from the conversion of a continuous voltage to its integer digital representation. Quantizing error is always ± 0.5 LSB and is the only error present in an ideal converter.

RALU

Register Arithmetic-Logic Unit. A part of the CPU that consists of the *ALU*, the *PSW*, the master *PC*, the microcode engine, a loop counter, and six registers.

Repeatability Error

The difference between corresponding code transitions from different *actual characteristics* taken from the same converter on the same channel with the same temperature, voltage, and frequency conditions. The amount of *repeatability error* depends on the ability of the comparator to resolve very similar voltages and the extent to which random noise contributes to the error.

Sample Delay

The time period between the time that A/D converter receives the "start conversion" signal and the time that the sample capacitor is connected to the selected channel.

Sample Delay Uncertainty

The variation in the *sample delay*.

Sample Time

The period of time that the *sample window* is open. (That is, the length of time that the analog input channel is actually connected to the sample capacitor.)

Sample Time Uncertainty

The variation in the *sample time*.

Sample Window

The period of time that begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

Sampled Inputs

All input pins, with the exception of RESET#, are *sampled inputs*. The input pin is sampled one state time before the read buffer is enabled. Sampling occurs during PH1 (while CLKOUT is low) and resolves the value (high or low) of the pin before it is presented to the internal bus. If the pin value changes during the sample time, the new value may or may not be recorded during the read.

RESET# is a level-sensitive input. EXTINT is normally a sampled input; however, during Powerdown mode, the powerdown circuitry uses EXTINT as a level-sensitive input.

SAR

Successive approximation register; a component of the A/D converter.

Set

The term *set* refers to the value of a bit or the act of giving it a value. If a bit is *set*, its value is "1"; *setting* a bit gives it a "1" value.

SFR

Special Function Register.

SHORT-INTEGER

An 8-bit, signed variable with values from –128 through +127.

Sink Current

Current flowing **into** a device to ground. Always a positive value.

Source Current — Current flowing **out of** a device from V_{CC}. Always a negative value.

SP — Stack Pointer.

Special Interrupt — Any of the three *nonmaskable interrupts* (Unimplemented Opcode, Software Trap, or NMI).

Standard Interrupt — Any *maskable interrupt* that is assigned to the *Interrupt Controller* for processing by interrupt service routines.

State Time (or State) — The basic time unit of the 8XC196KC/KD; the combined period of the two internal timing signals, PH1 and PH2. (The internal clock generator produces PH1 and PH2 by halving the frequency of the signal on XTAL1. The rising edges of the active-high PH1 and PH2 signals generate CLKOUT, the output of the internal clock generator.) With a 20 MHz crystal, one *state time* equals 100 ns. Because the 8XC196KC/KD can operate at many frequencies, this manual defines time requirements in terms of *state times* rather than in specific units of time.

Successive Approximation — An A/D conversion method that uses a binary search to arrive at the best digital representation of an analog input.

Temperature Coefficients — Change in the stated variable per degree Centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of *temperature drift*.

Temperature Drift — The rate at which typical specifications change with respect to a change in temperature. These changes are reflected in the *temperature coefficients*.

Terminal-Based Characteristic — An *actual characteristic* that has been translated and scaled to remove *zero offset* error and *full-scale error*. A *terminal-based characteristic* resembles an *actual characteristic* with *zero offset* and *full-scale error* removed.

Transfer Function — A graph of output code versus input voltage; the *characteristic* of the A/D converter.

Transfer Function Errors

Errors inherent in an analog-to-digital conversion process: *quantizing error*, *zero offset error*, *full-scale error*, *differential non-linearity*, and *non-linearity*. Errors that are hardware-dependent, rather than being inherent in the process itself, include *feedthrough*, *repeatability*, *channel-to-channel matching*, *off-isolation*, and V_{CC} *rejection* errors.

UART

Universal Asynchronous Receiver and Transmitter. A part of the serial I/O port.

V_{CC} Rejection

The property of an A/D converter that causes it to ignore (reject) changes in V_{CC} so that the *actual characteristic* is unaffected by those changes. The effectiveness of V_{CC} *rejection* is measured by the ratio of the change in V_{CC} to the change in the *actual characteristic*.

Vertical Windowing

The mapping of sections of RAM into the upper section of the lower Register File in 32-, 64-, or 128-byte increments. *Vertical windowing* enables the RALU to use register-direct addressing to access the RAM in the upper Register File.

VWindow

Vertical window. The 8XC196KC has 512 bytes of internal RAM, which can be mapped into sixteen 32-byte VWindows, eight 64-byte VWindows, or four 128-byte VWindows. Since the 8XC196KD has twice as much RAM, it also has twice as many VWindows.

WDT

Watchdog timer, an internal timer that resets the device if the software fails to operate properly.

Word

Any 16-bit unit of data.

WORD

An unsigned, 16-bit variable with values from 0 through 65535.

Zero Offset

The difference between the ideal and actual input voltage corresponding to the first *code transition*.