8XC196KC/KD Registers

C

APPENDIX C
8XC196KC/KD REGISTERS

This appendix provides reference information about the registers of the 8XC196KC/KD. Table C-1 lists the modules and major components of the 8XC196KC/KD with their related configuration and status registers. Table C-2 lists the horizontal windows (HWindows) with the special function registers (SFRs) and functions available in each. Table C-3 lists the SFRs, arranged alphabetically by mnemonic, along with register names, addresses, and reset values. Table C-4 lists the interrupts of the 8XC196KC/KD, the vector locations for both normal and PTS interrupt vectors, and interrupt priorities. Table C-5 lists interrupt sources with their related interrupt vectors, the mask bits that enable the interrupts, and the register bits that select the sources. Following the tables, individual descriptions of the registers are arranged alphabetically.

Table C-1. Modules and Related Registers

A/D	HSI	HSO	PTS	PWM
AD_COMMAND	HSI_MODE	HSO_COMMAND	PTSBLOCK	PWM0_CONTROL
AD_RESULT	HSI_STATUS	HSO_TIME	PTSCON	PWM1_CONTROL
AD_TIME	HSI_TIME	IOC1	PTSCOUNT	PWM2_CONTROL
IOC2	IOC0	IOC2	PTSDST	IOC2
	IOS1	IOS0	PTS_REG	IOC3
		IOS1	PTS_S/D	
		IOS2	PTSSEL	
			PTSSRC	
			PTSSRV	
Interrupts	**I/O Ports**	**Serial Port**	**Timer 1**	**Timer 2**
INT_MASK	IOPORT0	BAUD_RATE	TIMER1	TIMER2
INT_MASK1	IOPORT1	SBUF (RX)	IOC1	T2CAPTURE
INT_PEND	IOPORT2	SBUF (TX)	IOS1	IOC0
INT_PEND1	IOPORT34	SP_CON		IOC1
		SP_STAT		IOC2
				IOC3
Chip Config.	**Stack**	**Watchdog**	**Window Select**	**Zero**
CCR	SP	WATCHDOG	WSR	ZERO_REG

Table C-2. Special Function Register (SFR) HWindows

Hex Addr.	Read/ Write	HWindow 0	HWindow 1	HWindow 15
00	Read	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)
	Write	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)
01	Read	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)
	Write	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)
02	Read	AD_RESULT (LO)	Reserved	AD_COMMAND
	Write	AD_COMMAND		AD_RESULT (LO)
03	Read	AD_RESULT (HI)	AD_TIME	HSI_MODE
	Write	HSI_MODE	AD_TIME	AD_RESULT (HI)
04	Read	HSI_TIME (LO)	PTSSEL (LO)	HSO_TIME (LO)
	Write	HSO_TIME (LO)	PTSSEL (LO)	HSI_TIME (LO)
05	Read	HSI_TIME (HI)	PTSSEL (HI)	HSO_TIME (HI)
	Write	HSO_TIME (HI)	PTSSEL (HI)	HSI_TIME (HI)
06	Read	HSI_STATUS	PTSSRV (LO)	HSO_COMMAND
	Write	HSO_COMMAND	PTSSRV (LO)	HSI_STATUS, bits 0, 2, 4, 6
07	Read	SBUF (RX)	PTSSRV (HI)	SBUF (TX)
	Write	SBUF (TX)	PTSSRV (HI)	SBUF(RX)
08	Read	INT_MASK	INT_MASK	INT_MASK
	Write	INT_MASK	INT_MASK	INT_MASK
09	Read	INT_PEND	INT_PEND	INT_PEND
	Write	INT_PEND	INT_PEND	INT_PEND
0A	Read	TIMER1 (LO)	Reserved	WATCHDOG
	Write	WATCHDOG		TIMER1 (LO)
0B	Read	TIMER1 (HI)	Reserved	IOC2, except bit 7 (Note 1)
	Write	IOC2		TIMER1 (HI)
0C	Read	TIMER2 (LO)	IOC3 (Note 2)	T2CAPTURE (LO)
	Write	TIMER2 (LO)	IOC3 (Note 2)	T2CAPTURE (LO)
0D	Read	TIMER2 (HI)	Reserved	T2CAPTURE (HI)
	Write	TIMER2 (HI)		T2CAPTURE (HI)

Table C-2. Special Function Register (SFR) HWindows (Continued)

Hex Addr.	Read/ Write	HWindow 0	HWindow 1	HWindow 15
0E	Read	IOPORT0	Reserved	Reserved
	Write	BAUD_RATE		
0F	Read	IOPORT1	Reserved	Reserved
	Write	IOPORT1		
10	Read	IOPORT2	Reserved	Reserved
	Write	IOPORT2		
11	Read	SP_STAT	Reserved	SP_CON
	Write	SP_CON		SP_STAT (Note 3)
12	Read	INT_PEND1	INT_PEND1	INT_PEND1
	Write	INT_PEND1	INT_PEND1	INT_PEND1
13	Read	INT_MASK1	INT_MASK1	INT_MASK1
	Write	INT_MASK1	INT_MASK1	INT_MASK1
14	Read	WSR	WSR	WSR
	Write	WSR	WSR	WSR
15	Read	IOS0	Reserved	IOC0, except bit 1 (Note 1)
	Write	IOC0		IOS0, except bits 6 and 7
16	Read	IOS1	PWM2_CONTROL	IOC1
	Write	IOC1	PWM2_CONTROL	IOS1, except bits 6 and 7 (Note 3)
17	Read	IOS2	PWM1_CONTROL	PWM0_CONTROL
	Write	PWM0_CONTROL	PWM1_CONTROL	IOS2 (Note 3)
18	Read	SP (LO)	SP (LO)	SP (LO)
	Write	SP (LO)	SP (LO)	SP (LO)
19	Read	SP (HI)	SP (HI)	SP (HI)
	Write	SP (HI)	SP (HI)	SP (HI)

NOTES:

1. IOC2.7 and IOC0.1 are not latched and will read as "1" (precharged bus).
2. The IOC3 register was previously called T2CONTROL or T2CNTC.
3. Writing to the SP_STAT, IOS1, and IOS2 registers in HWindow 15 sets the status bits, but does not cause interrupts.

Table C-3. SFR Name, Address, and Reset Status

Register Mnemonic	Register Name	Hex Addr.	Binary Reset Value
AD_COMMAND	A/D Command Register	02	XXXX XXXX
AD_RESULT	A/D Result Register	03, 02	0111 1111 1100 0000
AD_TIME	A/D Time Register	03	1111 1111
BAUD_RATE	Baud Rate Register	0E	0000 00X0
HSI_MODE	HSI Mode Register	03	1111 1111
HSI_STATUS	HSI Status Register	06	X0X0 X0X0
HSI_TIME	HSI Time Register	05, 04	XXXX XXXX XXXX XXXX
HSO_COMMAND	HSO Command Register	06	XXXX XXXX
HSO_TIME	HSO Time Register	05, 04	XXXX XXXX XXXX XXXX
INT_MASK	Interrupt Mask Register	08	0000 0000
INT_MASK1	Interrupt Mask Register 1	13	0000 0000
INT_PEND	Interrupt Pending Register	09	0000 0000
INT_PEND1	Interrupt Pending Register 1	12	0000 0000
IOC0	I/O Control Register 0	15	0000 00X0
IOC1	I/O Control Register 1	16	0010 0001
IOC2	I/O Control Register 2	0B	X000 0000
IOC3	I/O Control Register 3	0C	**KC-B** 1111 0010 **KC-C KD** 1111 0000
IOPORT0	Port 0 Register	0E	XXXX XXXX
IOPORT1	Port 1 Register	0F	1111 1111

Table C-3. SFR Name, Address, and Reset Status (Continued)

Register Mnemonic	Register Name	Hex Addr.	Binary Reset Value			
IOPORT2	Port 2 Register	10			1100	0001
IOPORT34	Port 3 and 4 Register	1FFE	1111	1111	1111	1111
IOS0	I/O Status Register 0	15			0000	0000
IOS1	I/O Status Register 1	16			0000	0000
IOS2	I/O Status Register 2	17			0000	0000
PTSSEL	PTS Select Register	05, 04	0000	0000	0000	0000
PTSSRV	PTS Service Register	07, 06	0000	0000	0000	0000
PWM0_CONTROL	PWM0 Control Register	17			0000	0000
PWM1_CONTROL	PWM1 Control Register	16			0000	0000
PWM2_CONTROL	PWM2 Control Register	17			0000	0000
SBUF (RX/TX)	Serial Port Buffer	07			0000	0000
SP	Stack Pointer	19, 18	0001	1101	0001	1000
SP_CON	Serial Port Control Register	11			0000	1011
SP_STAT	Serial Port Status Register	11			0000	1011
T2CAPTURE	Timer 2 Capture Register	0D, 0C	XXXX	XXXX	XXXX	XXXX
TIMER1	Timer 1 Value Register	0B, 0A	0000	0000	0000	0000
TIMER2	Timer 2 Value Register	0D, 0C	0000	0000	0000	0000
WATCHDOG	Watchdog Timer Register	0A			XXXX	XXXX
WSR	Window Select Register	14			XXXX	0000
ZERO_REG	Zero Register	01, 00	0000	0000	0000	0000

Table C-4. 8XC196KC/KD Interrupt Vector Sources, Locations, and Priorities

Number	Interrupt Vector	Source(s)	Interrupt Vector Location	PTS Vector Location	Priority (1)
Special	Unimplemented Opcode	Unimplemented Opcode	2012H	—	—
Special	Software Trap	TRAP Instruction	2010H	—	—
INT15	NMI (2)	NMI	203EH	—	15
Each of the following, maskable interrupts can be assigned to the PTS. Any PTS interrupt has priority over all other maskable interrupts.					
INT14	HSI FIFO Full	HSI FIFO Full	203CH	205CH	14
INT13	EXTINT1 (2)	P2.2	203AH	205AH	13
INT12	Timer 2 Overflow	Timer 2 Overflow	2038H	2058H	12
INT11	Timer 2 Capture (2)	Timer 2 Capture	2036H	2056H	11
INT10	HSI FIFO 4	HSI FIFO Fourth Entry	2034H	2054H	10
INT09	Receive	RI Flag (3)	2032H	2052H	9
INT08	Transmit	TI Flag (3)	2030H	2050H	8
INT07	EXTINT (2)	P2.2 or P0.7	200EH	204EH	7
INT06	Serial Port	RI Flag and TI Flag (4)	200CH	204CH	6
INT05	Software Timer	Software Timer 0–3 Timer 2 Reset A/D Conversion Start	200AH	204AH	5
INT04	HSI.0 Pin (2)	HSI.0	2008H	2048H	4
INT03	High Speed Outputs	HSO.0–HSO.5	2006H	2046H	3
INT02	HSI Data Available	HSI FIFO Full or HSI Holding Reg. Loaded	2004H	2044H	2
INT01	A/D Conversion Complete	A/D Conversion Complete	2002H	2042H	1
INT00	Timer Overflow	Timer 1 or Timer 2	2000H	2040H	0

NOTES:

1. The Unimplemented Opcode and Software Trap interrupts are not prioritized. They go directly to the Interrupt Controller for servicing. NMI has the highest priority of all prioritized interrupts. Any PTS interrupt has priority over all other maskable interrupts.
2. These interrupts can be configured to function as independent, external interrupts.
3. If the Serial interrupt is masked and the Receive and Transmit interrupts are enabled, the RI flag and TI flag generate separate Receive and Transmit interrupts. If 8096BH compatibility is not an issue, this configuration is preferred.
4. If the Receive and Transmit interrupts are masked and the Serial interrupt is enabled, both RI flag and TI flag generate a Serial Port interrupt. This configuration provides compatibility with the 8096BH.

Table C-5. 8XC196KC/KD Interrupt Sources, Vectors, and Register Bits

Interrupt Source	Interrupt Vector(s)	Number	Interrupt Enabled by Setting (1)	Source Selected by (2)
A/D Conversion Complete	A/D Conversion Complete	INT01	INT_MASK.1	—
A/D Conversion Start	Software Timer	INT05	INT_MASK.5	—
HSI FIFO Fourth Entry	HSI FIFO 4	INT10	INT_MASK1.2	—
HSI FIFO Full	HSI FIFO Full	INT14	INT_MASK1.6	—
	HSI Data Available	INT02	INT_MASK.2	IOC1.7 = 1
HSI Holding Register Loaded	HSI Data Available	INT02	INT_MASK.2	IOC1.7 = 0
HSI.0	HSI.0 Pin	INT04	INT_MASK.4	—
HSO.0–HSO.5	High-Speed Output	INT03	INT_MASK.3	—
NMI	NMI	INT15	—	—
P0.7	EXTINT	INT07	INT_MASK.7	IOC1.1 = 1
P2.2	EXTINT	INT07	INT_MASK.7	IOC1.1 = 0
	EXTINT1	INT13	INT_MASK1.5	—
RI Flag	Receive	INT09	INT_MASK1.1	—
	Serial Port	INT06	INT_MASK.6	—
Software Timers 0–3	Software Timer	INT05	INT_MASK.5	—
TI Flag	Transmit	INT08	INT_MASK1.0	—
	Serial Port	INT06	INT_MASK.6	—
Timer 1 Overflow	Timer Overflow	INT00	INT_MASK.0	IOC1.2 = 1
Timer 2 Capture	Timer 2 Capture	INT11	INT_MASK1.3	—
Timer 2 Overflow	Timer Overflow	INT00	INT_MASK.0	IOC1.3 = 1
	Timer 2 Overflow	INT12	INT_MASK1.4	—
Timer 2 Reset	Software Timer	INT05	INT_MASK.5	—
TRAP Instruction	Software Trap	Special	—	—
Unimplemented Opcode	Unimplemented Opcode	Special	—	—

NOTES:

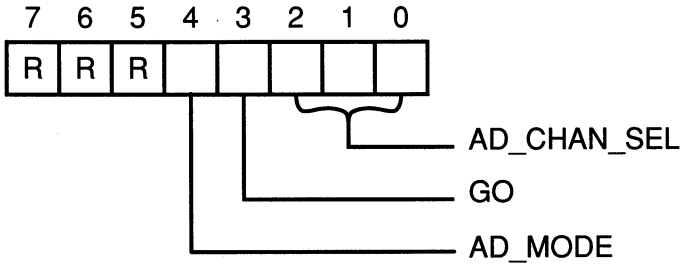
1. This column lists, for each interrupt source, the mask bit that must be set to enable the interrupt. Five interrupt sources can each generate two different interrupts — an 8096BH-compatible interrupt and a new, separate interrupt (HSI FIFO Full, EXTINT1, Receive, Transmit, Timer 2 Overflow). In all cases, only one interrupt should be enabled for each source. (That is, the mask bit should be set for only one of the two possible interrupts).
2. Three of the 8096BH-compatible interrupts (HSI Data Available, EXTINT, and Timer Overflow) can be generated by either of two sources. This column shows the IOC1 register bit and value that selects each source.

A/D Command Register

AD_COMMAND
02H
HWindow 0 (Write), HWindow 15 (Read)

The A/D Command Register selects the A/D channel number to be converted, controls whether the A/D converter starts immediately or with an HSO command, and selects either 8-bit or 10-bit conversion mode.

AD_COMMAND



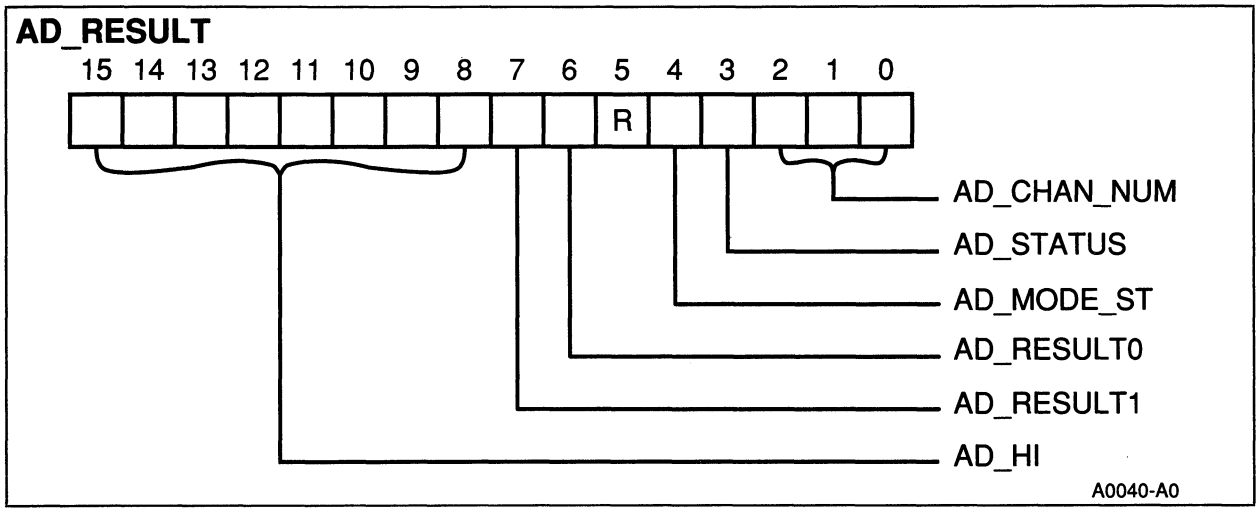
A0039-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–2	AD_CHAN_SEL	A/D Channel Selection	XXX	These three bits select the channel number for conversion: **Bit 2 1 0 Channel** 0 0 0 ACH0 0 0 1 ACH1 0 1 0 ACH2 0 1 1 ACH3 1 0 0 ACH4 1 0 1 ACH5 1 1 0 ACH6 1 1 1 ACH7
3	GO	A/D Conversion Source	X	This bit determines at what point a conversion is to start: 1= Start immediately 0= HSO initiates conversion
4	AD_MODE	A/D Conversion Mode	X	This bit determines whether an 8-bit or a 10-bit conversion is to be performed. 1= 8-bit conversion 0= 10-bit conversion
5–7	—	—	XXX	Reserved; always write as zero.

A/D Result Register

AD_RESULT
03/02H
HWindow 0 (Read), HWindow 15 (Write)

The AD_RESULT register consists of two bytes. The high byte contains the eight most-significant bits from the A/D converter. The low byte indicates the A/D channel number that was used for the conversion, indicates whether a conversion is currently in progress, and contains the two least-significant bits from a ten-bit A/D conversion. The AD_RESULT register is cleared when a new conversion is started; therefore, to prevent losing data, both bytes must be read before a new conversion starts.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–2	AD_CHAN_NUM	A/D Channel Number	000	The A/D channel number that was used for the conversion.
3	AD_STATUS	A/D Status	0	Indicates the status of the A/D converter. Up to 8 state times are required to set this bit following a start command. When testing this bit, wait at least the 8 state times. 1= A/D conversion is in progress 0= A/D is idle
4	AD_MODE_ST	A/D Conversion Mode	0	Indicates whether this is an 8-bit or a 10-bit conversion. 1= 8-bit conversion 0= 10-bit conversion
5	—	—	0	Reserved; always write as zero.

AD_RESULT

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
6	AD_RESULT0	Bit 0 of 10-Bit Conv.	1	Bit 0 (the LSB) of a 10-bit conversion.
7	AD_RESULT1	Bit 1 of 10-Bit Conv.	1	Bit 1 of a 10-bit conversion.
8–15	AD_HI	A/D High Result	1111 1110	The 8 most-significant bits of the result from the A/D converter.

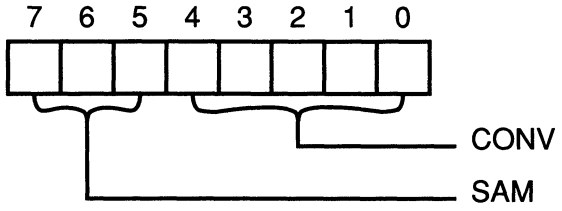
A/D Conversion Time Register

AD_TIME
03H
HWindow 1 (Read/Write)

The AD_TIME register programs the sample time and conversion time for the A/D converter. These values are used when IOC2.3 is set. When IOC2.3 is clear (80C196KB-compatible mode) IOC2.4 controls the sample and conversion times.

The sample time (SAM) is the length of time that the analog input channel is actually connected to the sample capacitor. Sample time must be long enough to allow the sample capacitor to charge properly, but not so long that the input will change and cause errors. The conversion time (CONV) determines the length of time required to convert the analog voltage on the sample capacitor to a digital value. Conversion time must be long enough to allow the comparator to settle and resolve the voltage, but not so long that the sample capacitor will discharge and lose accuracy.

AD_TIME



A0041-00

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–4	CONV	A/D Convert Time	11111	These bits specify the conversion time. CONV must be from 2 to 31, inclusive.
5–7	SAM	A/D Sample Time	111	These bits specify the sample time. SAM must be from 1 to 7, inclusive.

NOTES:

1. The register programs the speed at which the A/D can run — not the speed at which it can convert correctly. Consult the data sheet for recommended values.
2. Initialize the A/D registers in this order: AD_TIME, IOC2, and AD_COMMAND.
3. Do not start a conversion using the AD_TIME register (IOC2.3=1) when an 80C196KB-compatible conversion (IOC2.3=0) is in progress, and vice versa.

AD_TIME

The following formulas are used to compute sample and conversion times.

$$SAM = \frac{(T_{SAM} \times F_{OSC} - 2) / 4}{2}$$

$$CONV = \left[\frac{(T_{CONV} \times F_{OSC} - 3)}{2} / B\right] - 1$$

where:

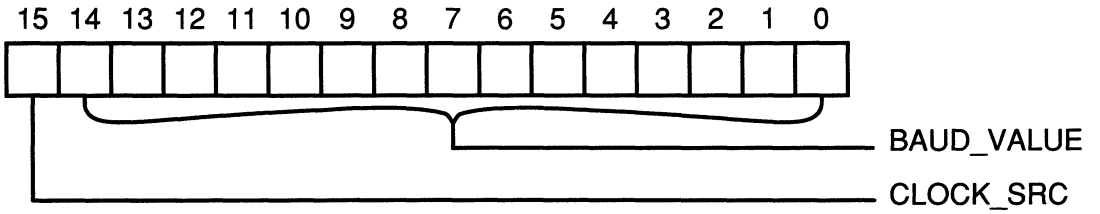
T_{SAM}	is the sample time, in µsec, from the data sheet
T_{CONV}	is the conversion time, in µsec, from the data sheet
F_{OSC}	is the XTAL1 frequency, in MHz
B	is the number of bits to be converted (8 or 10)

Baud Rate Register

BAUD_RATE
0EH
HWindow 0 (Write)

The Baud Rate register selects the serial port baud rate and clock source. It must be written with two bytes, the least-significant byte first. The most-significant bit selects the clock source. The lower 15 bits represent BAUD_VALUE, an unsigned integer that determines the baud rate. BAUD_VALUE has a maximum value of 32,767 and can equal zero only when using XTAL1 in asynchronous modes 1, 2, and 3.

BAUD_RATE



A0042-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–14	BAUD_VALUE	Baud Rate	0000 00X0 0000 00x	These bits constitute the BAUD_VALUE. Load the least-significant byte first.
15	CLOCK_SRC	Serial Port Clock Source	0	This bit determines whether the serial port is clocked from an internal or an external source. 1= XTAL1 (internal source) 0= T2CLK (external source)

BAUD_RATE

The following formulas are used in determining baud rates.

Synchronous Mode 0:

$$\text{BAUD\_VALUE} = \frac{F_{OSC}}{\text{Baud Rate} \times 8} - 1 \quad \text{or} \quad \frac{\text{T2CLK}}{\text{Baud Rate}}$$

Asynchronous Modes 1, 2, and 3:

$$\text{BAUD\_VALUE} = \frac{F_{OSC}}{\text{Baud Rate} \times 16} - 1 \quad \text{or} \quad \frac{\text{T2CLK}}{\text{Baud Rate} \times 8}$$

where:

F_{OSC} is the XTAL1 frequency, in MHz

Common baud rate values using XTAL1 at 16 MHz are shown below.

Baud Rate	BAUD_VALUE	
	Mode 0	Modes 1, 2, 3
9600	8340H	8067H
4800	8682H	80CFH
2400	8D04H	81A0H
1200	9A0AH	8340H
300	E82BH	8D04H

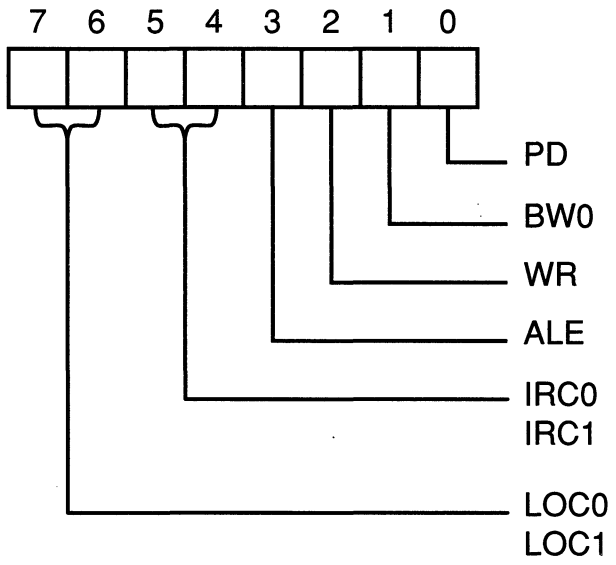
Chip Configuration Register — CCR

The Chip Configuration Register (CCR) controls Powerdown mode, bus width, bus control signals, internal READY mode, and internal memory protection.

In normal operating mode, the CCR is loaded from the Chip Configuration Byte (CCB) at location 2018H in either internal or external memory, depending on the state of the EA# pin. (EA# low selects external memory; EA# high selects internal memory.) In programming mode, the CCR is loaded from the Programming Chip Configuration Byte (PCCB). The CCB or PCCB is the first byte fetched from memory after a device reset. The CCR is loaded only once during the reset sequence; once it is loaded, the CCR cannot be changed until the next device reset.

If the READY pin is pulled low during the CCR fetch, the bus controller automatically inserts a maximum of three wait states into the CCR bus cycle. This allows a CCR fetch from slow memory. CCR.4 and CCR.5 control the number of wait states inserted into the bus cycle.

CCR



CCR

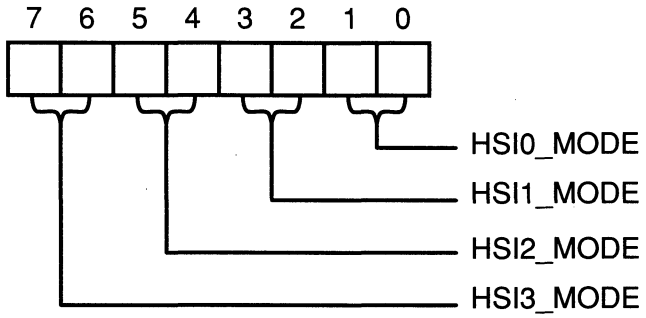
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	PD	Powerdown Enable	1	Controls whether the IDLPD #2 instruction causes the device to enter Powerdown mode. Clearing this bit at reset can prevent accidental entry into Powerdown mode. 1= enable Powerdown mode 0= disable Powerdown mode
1	BW0	Buswidth Control	1	Selects dynamic or 8-bit bus width. 1= dynamic bus width; bus width is controlled by the BUSWIDTH pin BUSWIDTH=1, 16-bit bus BUSWIDTH=0, 8-bit bus 0= the device is locked into 8-bit mode and the BUSWIDTH pin is ignored
2	WR	Select Write Strobe Mode	1	Selects the write strobe signals to be generated for 16-bit cycles: 1= WR# and BHE# are generated in Standard Bus and Address Valid Strobe modes. 0= WRL# and WRH# are generated in Write Strobe and Address Valid with Write Strobe modes.
3	ALE	Select Address Valid Strobe Mode	1	Selects the address valid signals to be generated. 1= ALE is generated to latch the valid address in Standard Bus and Write Strobe modes. 0= ADV# is generated in place of ALE and can be used as a simple chip select for external memory.
4–5	IRC0–IRC1	Internal Ready Control	10	Limit the number of wait states that can be inserted while the READY pin is held low. Wait states are inserted into the bus cycle either until the READY pin is pulled high or until this internal number is reached. **IRC1 IRC0 Max. Wait States** 0 0 1 0 1 2 1 0 3 1 1 READY pin controlled
6–7	LOC0–LOC1	Lock Bits	00	Determine the programming protection scheme for internal memory. **LOC1 LOC0 Protection** 0 0 read and write protect 0 1 read protect only 1 0 write protect only 1 1 no protection

HSI Mode Register

HSI_MODE
03H
HWindow 0 (Write), HWindow 15 (Read)

The HSI Mode register controls, for each HSI pin, which of four types of events trigger a capture into the HSI FIFO: each positive transition, each negative transition, every transition (both positive and negative), or a series of eight positive transitions. The pins must be individually enabled through the IOC0 register.

HSI_MODE



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–1	HSI0_MODE	HSI.0 Mode	11	HSI.0 transition mode
2–3	HSI1_MODE	HSI.1 Mode	11	HSI.1 transition mode
4–5	HSI2_MODE	HSI.2 Mode	11	HSI.2 transition mode
6–7	HSI3_MODE	HSI.3 Mode	11	HSI.3 transition mode

Each two-bit field defines the transition mode for the corresponding pin:

Transition Mode Encoding

Bit 1	Bit 0	Description
0	0	Eight positive transitions trigger a capture into the HSI FIFO.
0	1	Each positive transition triggers a capture into the HSI FIFO.
1	0	Each negative transition triggers a capture into the HSI FIFO.
1	1	Every transition (both positive and negative) triggers a capture into the HSI FIFO.

HSI Status Register

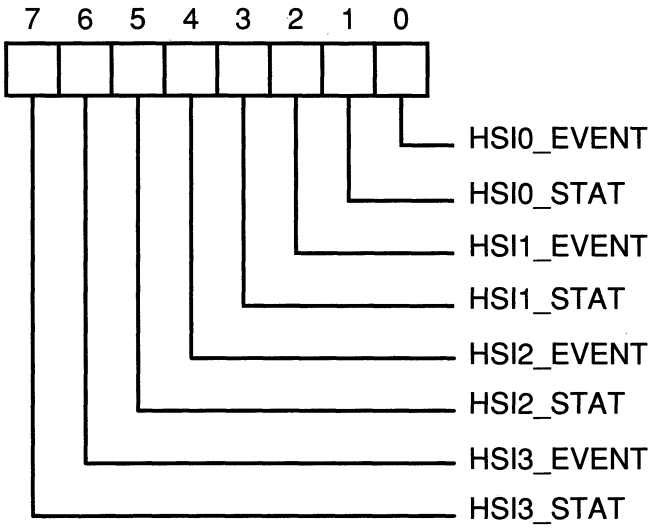
HSI_STATUS
06H
HWindow 0 (Read), HWindow 15 (Write bits 0, 2, 4, 6)

The HSI_STATUS register indicates HSI event status and current pin states. The HSI_TIME register contains the associated time tag. Reading HSI_TIME unloads the holding register. If you read HSI_TIME before HSI_STATUS, the status information associated with the HSI_TIME time tag is lost.

If the HSI holding register contains no events, the event status bits in this register are indeterminate; however, the pin state bits can be read at any time. This allows reading the HSI pins as inputs even when they are not enabled to the HSI unit. Writing to HSI_STATUS in HWindow 15 sets the event status bits but does not affect the pin state bits. Note that a current pin state is not necessarily related to the corresponding event status bit, since other events may have occurred since the pin state was last written.

The IOC0 register controls the alternate functions of HSI.0–HSI.3, and the HSI_MODE register controls the pin events that will trigger a capture into the HSI FIFO.

HSI_STATUS



A0044-A0

HSI_STATUS

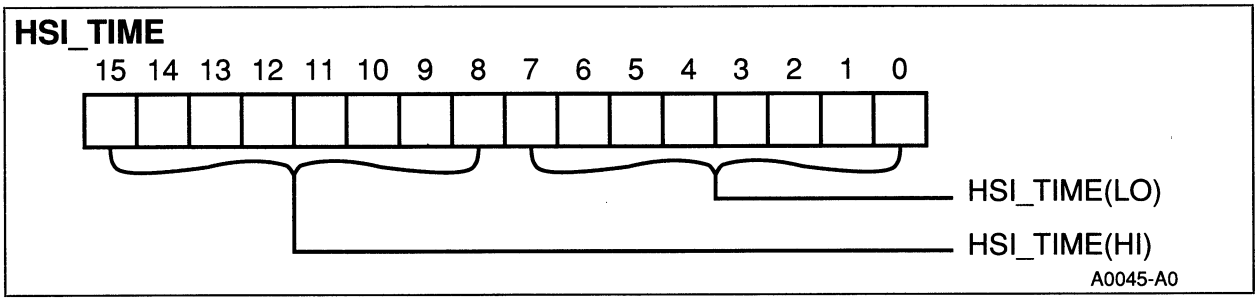
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	HSI0_EVENT	HSI.0 Pin Event	0	1= an event occurred on pin HSI.0 0= no event
1	HSI0_STAT	HSI.0 Pin Status	X	Current state of the HSI.0 pin.
2	HSI1_EVENT	HSI.1 Pin Event	0	1= an event occurred on pin HSI.1 0= no event
3	HSI1_STAT	HSI.1 Pin Status	X	Current state of the HSI.1 pin.
4	HSI2_EVENT	HSI.2 Pin Event	0	1= an event occurred on pin HSI.2 0= no event
5	HSI2_STAT	HSI.2 Pin Status	X	Current state of the HSI.2 pin.
6	HSI3_EVENT	HSI.3 Pin Event	0	1= an event occurred on pin HSI.3 0= no event
7	HSI3_STAT	HSI.3 Pin Status	X	Current state of the HSI.3 pin.

HSI Time Register

HSI_TIME
04, 05H
HWindow 0 (Read), HWindow 15 (Write)

The HSI Time register contains the time, with respect to the Timer 1 count value, at which an HSI event was triggered. When an event occurs on an HSI pin, the HSI_TIME register is loaded with the current 16-bit Timer 1 value. This time is stored into the HSI FIFO, along with the four event status bits in the HSI_STATUS register.

Reading the HSI_TIME register unloads the holding register. If you read HSI_TIME before HSI_STATUS, the status information associated with the HSI_TIME time tag is lost. If HSI holding register contains no events, HSI_TIME is indeterminate. Writing to HSI_TIME in HWindow 15 loads the holding register, overwriting any other data.



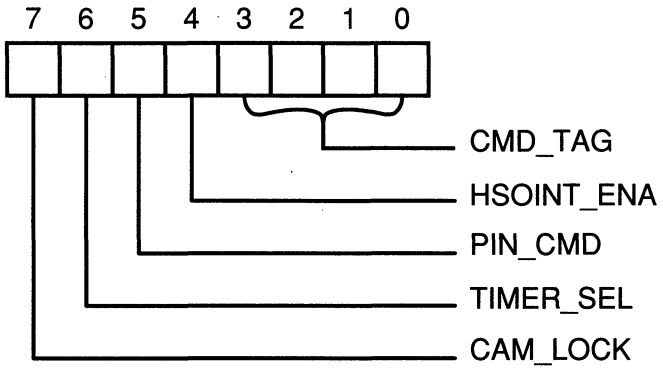
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	HSI_TIME (LO)	HSI Event Time	XXXX XXXX	The lower eight bits of the HSI event time.
8–15	HSI_TIME (HI)	HSI Event Time	XXXX XXXX	The upper eight bits of the HSI event time.

HSO Command Register

HSO_COMMAND
06H
HWindow 0 (Write), HWindow 15 (Read)

The HSO module can trigger events at specific times with minimal CPU overhead. The HSO Command Register determines what event or events will occur within the HSO module at the time specified in the HSO_TIME register.

HSO_COMMAND



A0046-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–3	CMD_TAG	HSO Commands	XXXX	Determines what event or events will occur at the time specified in HSO_TIME. (See the "CMD_TAG Encoding" table.)
4	HSOINT_ENA	Enable/ Disable HSO Interrupt	X	Determines whether an HSO event generates an interrupt. 1= generate an interrupt 0= no interrupt When this bit is set, programmed HSO pin events generate the High-Speed Output interrupt (INT03, 2006H) and internal events generate the Software Timer interrupt (INT05, 200AH). When an interrupt is generated, the HSO event status bits in the IOS1 and IOS2 registers must be interrogated to determine which event caused the interrupt.
5	PIN_CMD	Set/Clear Selected HSO Pin	X	Determines whether the effect of a CMD_TAG command sets or clears the specified pin or pins. 1= Set the pin(s) 0= Clear the pin(s)

HSO_COMMAND

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
6	TIMER_SEL	Select Timer 1/ Timer 2	X	Selects the timer reference for the HSO command. 1= Select Timer 2 0= Select Timer 1
7	CAM_LOCK	Lock Entry Into CAM	X	When IOC2.6 is set (command locking enabled), this bit controls whether the HSO command is locked into the CAM or cleared after execution. 1= Lock command into CAM 0= Clear command from CAM after execution Writing a "1" to IOC2.7 clears all entries (locked or not) from the CAM, as does a chip reset.

CMD_TAG Encoding

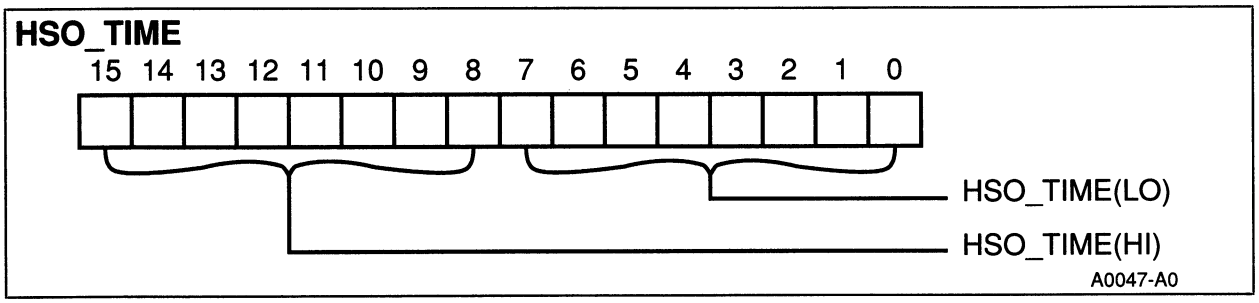
Bit 3	Bit 2	Bit 1	Bit 0	Command Mnemonic	Definition
0	0	0	0	HSO0	Switch High-Speed Output 0
0	0	0	1	HSO1	Switch High-Speed Output 1
0	0	1	0	HSO2	Switch High-Speed Output 2
0	0	1	1	HSO3	Switch High-Speed Output 3
0	1	0	0	HSO4	Switch High-Speed Output 4
0	1	0	1	HSO5	Switch High-Speed Output 5
0	1	1	0	HSO01 *	Switch High-Speed Outputs 0 and 1
0	1	1	1	HSO23 *	Switch High-Speed Outputs 2 and 3
1	0	0	0	SWT0	Program Software Timer 0
1	0	0	1	SWT1	Program Software Timer 1
1	0	1	0	SWT2	Program Software Timer 2
1	0	1	1	SWT3	Program Software Timer 3
1	1	0	0	HSOALL *	Switch High-Speed Outputs 0, 1, 2, 3, 4, 5
1	1	0	1	—	Reserved; do not use
1	1	1	0	T2RST	Reset Timer 2
1	1	1	1	A_D	Start an A/D Conversion

* In these configurations, two or more pins are set or cleared simultaneously.

HSO Time Register

HSO_TIME
05/04H
HWindow 0 (Write), HWindow 15 (Read)

The HSO Time register specifies the time at which an HSO command is to be executed. The command is specified by HSO_COMMAND.0–HSO_COMMAND.3, and the timer reference is selected by HSO_COMMAND.6. When loading events into the CAM, write to the HSO_COMMAND register first, then write to HSO_TIME.



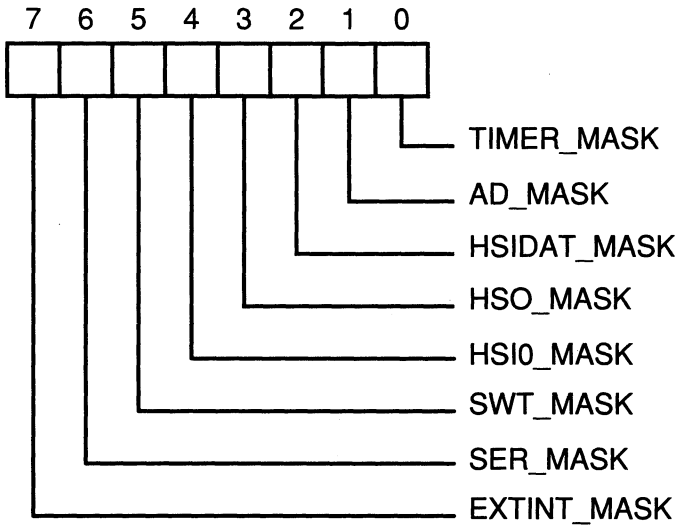
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	HSO_TIME (LO)	HSO Command Execution Time, Low Byte	XXXX	This is the low byte of HSO_TIME, which specifies the time at which an HSO command is to be executed.
8–15	HSO_TIME (HI)	HSO Command Execution Time, High Byte	XXXX	This is the high byte of HSO_TIME, which specifies the time at which an HSO command is to be executed.

Interrupt Mask Register

INT_MASK
08H
All HWindows (Read/Write)

The Interrupt Mask register enables or disables (masks) individual interrupts. (PSW.2 globally enables or disables servicing of all maskable interrupts.) INT_MASK can be read from or written to as a byte register in all HWindows. INT_MASK is the low byte of the Program Status Word (PSW); therefore, PUSHF or PUSHA saves this register on the stack and POPF or POPA restores it.

INT_MASK



INT_MASK

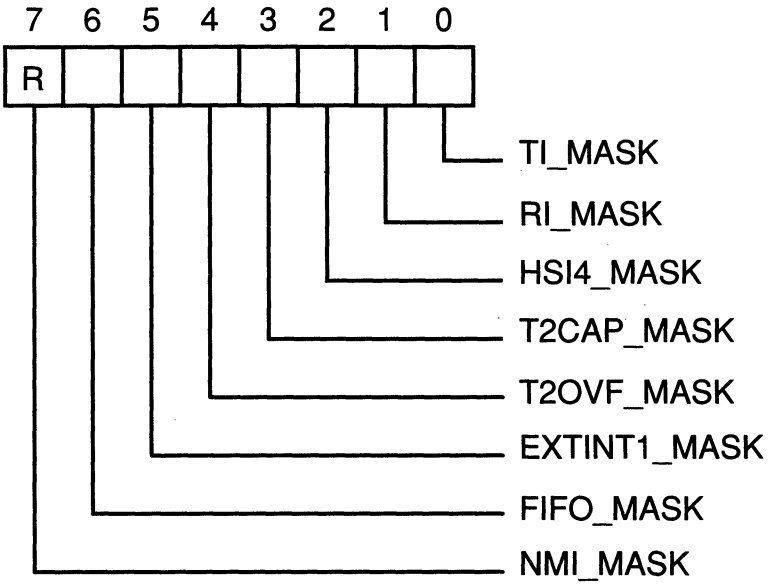
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	TIMER_MASK	Timer 1 or Timer 2 Overflow	0	Setting this bit enables the Timer Overflow interrupt (INT00, 2000H). Both Timer 1 and Timer 2 can generate the INT00 interrupt. Setting IOC1.2 selects Timer 1 as a source; setting IOC1.3 selects Timer 2 as a source. Timer 2 can generate either INT00 or INT12, but should not be configured for both.
1	AD_MASK	A/D Conversion Complete	0	Setting this bit enables the A/D Conversion Complete interrupt (INT01, 2002H).
2	HSIDAT_MASK	HSI Data Available/ FIFO Full	0	Setting this bit enables the HSI Data Available interrupt (INT02, 2004H). IOC1.7 selects the source of the interrupt.
3	HSO_MASK	HSO Output Event	0	Setting this bit enables the High-Speed Output interrupt (INT03, 2006H).
4	HSI0_MASK	HSI.0 External Interrupt	0	Setting this bit enables the HSI.0 Pin interrupt (INT04, 2008H).
5	SWT_MASK	Software Timer	0	Setting this bit enables the Software Timer interrupt (INT05, 200AH).
6	SER_MASK	Serial Port	0	Setting this bit enables the Serial Port interrupt (INT06, 200CH), which is the 8096BH-compatible configuration. If this bit is set, INTMASK1.0 and INTMASK1.1 should be cleared, disabling the Receive and Transmit interrupts.
7	EXTINT_MASK	EXTINT or P0.7 Interrupt	0	Setting this bit enables the EXTINT interrupt (INT07, 200EH). IOC1.1 selects the interrupt source (P0.7 or P2.2).

Interrupt Mask Register 1

INT_MASK1
13H
All HWindows (Read/Write)

The Interrupt Mask 1 register enables or disables (masks) individual interrupts. (PSW.2 globally enables or disables servicing of all maskable interrupts.) INT_MASK1 can be read from or written to as a byte register in all HWindows. PUSHA saves this register on the stack, and POPA restores it.

INT_MASK1



INT_MASK1

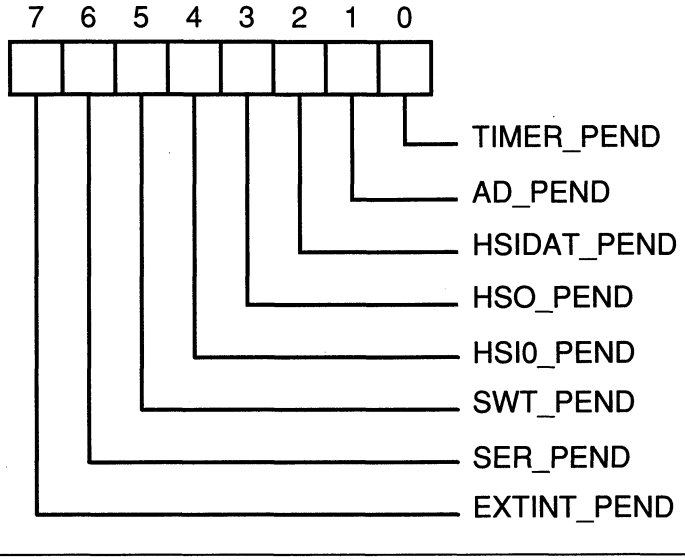
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	TI_MASK	Transmit Interrupt	0	Setting this bit enables the Transmit interrupt (INT08, 2030H). If this bit is set, INT_MASK1.1 should also be set and INT_MASK.6 should be cleared.
1	RI_MASK	Receive Interrupt	0	Setting this bit enables the Receive interrupt (INT09, 2032H). If this bit is set, INT_MASK1.0 should also be set and INT_MASK.6 should be cleared.
2	HSI4_MASK	HSI FIFO 4 Interrupt	0	Setting this bit enables the HSI FIFO 4 interrupt (INT10, 2034H).
3	T2CAP_MASK	Timer 2 Capture Interrupt	0	Setting this bit enables the Timer 2 Capture interrupt (INT11, 2036H).
4	T2OVF_MASK	Timer 2 Overflow Interrupt	0	Setting this bit enables the Timer 2 Overflow interrupt (INT12, 2038H). IOC2.5 selects the overflow boundary for INT12.
5	EXTINT1_MASK	EXTINT Pin Interrupt	0	Setting this bit enables the EXTINT1 interrupt (INT13, 203AH). P2.2 can generate either the EXTINT interrupt (INT07) or the EXTINT1 interrupt (INT13).
6	FIFO_MASK	HSI FIFO Full Interrupt	0	Setting this bit enables the HSI FIFO Full interrupt (INT14, 203CH).
7	NMI_MASK	NMI	0	This non-functional mask bit exists for design symmetry. The Nonmaskable Interrupt (NMI) is enabled for both 0 and 1. Always write zero to this bit.

Interrupt Pending Register

INT_PEND
09H
All HWindows (Read/Write)

When hardware detects a pending interrupt, it sets the corresponding bit in INT_PEND or INT_PEND1. When the vector is taken, the hardware clears the pending bit. The INT_PEND register can be read from or written to in all HWindows. Software can generate an interrupt by setting the corresponding interrupt pending bit.

INT_PEND



INT_PEND

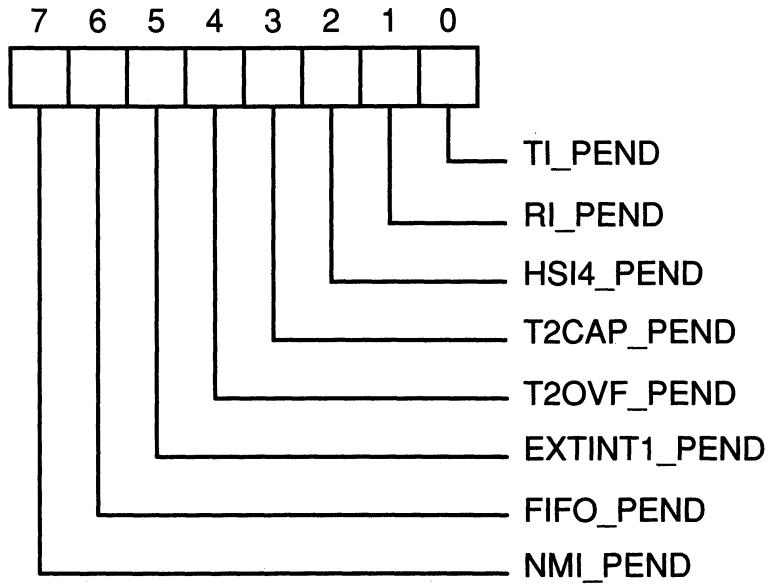
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	TIMER_PEND	Timer 1 or Timer 2 Overflow	0	When set, this bit indicates a pending Timer Overflow interrupt (INT00). It is cleared when the interrupt vectors to 2000H.
1	AD_PEND	A/D Conversion Complete	0	When set, this bit indicates a pending A/D Conversion Complete interrupt (INT01). It is cleared when the interrupt vectors to 2002H.
2	HSIDAT_PEND	HSI Data Available/ FIFO Full	0	When set, this bit indicates a pending HSI Data Available interrupt (INT02). It is cleared when the interrupt vectors to 2004H.
3	HSO_PEND	HSO Output Event	0	When set, this bit indicates a pending High-Speed Output interrupt (INT03). It is cleared when the interrupt vectors to 2006H.
4	HSI0_PEND	HSI.0 External Interrupt	0	When set, this bit indicates a pending HSI.0 Pin interrupt (INT04). It is cleared when the interrupt vectors to 2008H.
5	SWT_PEND	Software Timer	0	When set, this bit indicates a pending Software Timer interrupt (INT05). It is cleared when the interrupt vectors to 200AH.
6	SER_PEND	Serial Port	0	When set, this bit indicates a pending Serial Port interrupt (INT06). It is cleared when the interrupt vectors to 200CH.
7	EXTINT_PEND	EXTINT Pin or P0.7 Interrupt	0	When set, this bit indicates a pending EXTINT interrupt (INT07). It is cleared when the interrupt vectors to 200EH.

Interrupt Pending Register 1

INT_PEND1
12H
All HWindows (Read/Write)

When hardware detects a pending interrupt, it sets the corresponding bit in INT_PEND or INT_PEND1. When the vector is taken, the hardware clears the pending bit. The INT_PEND1 register can be read from or written to in all HWindows. Software can generate an interrupt by setting the corresponding interrupt pending bit.

INT_PEND1



A0051-A0

INT_PEND1

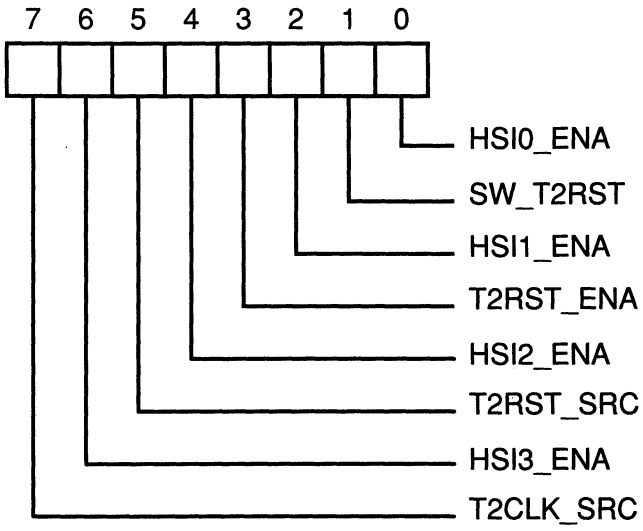
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	TI_PEND	Transmit Interrupt	0	When set, this bit indicates a pending Transmit interrupt (INT08). It is cleared when the interrupt vectors to 2030H.
1	RI_PEND	Receive Interrupt	0	When set, this bit indicates a pending Receive interrupt (INT09). It is cleared when the interrupt vectors to 2032H.
2	HSI4_PEND	HSI FIFO 4 Interrupt	0	When set, this bit indicates a pending HSI FIFO 4 interrupt (INT10). It is cleared when the interrupt vectors to 2034H.
3	T2CAP_PEND	Timer 2 Capture Interrupt	0	When set, this bit indicates a pending Timer 2 Capture interrupt (INT11). It is cleared when the interrupt vectors to 2036H.
4	T2OVF_PEND	Timer 2 Overflow Interrupt	0	When set, this bit indicates a pending Timer 2 Overflow interrupt (INT12). It is cleared when the interrupt vectors to 2038H.
5	EXTINT1_PEND	EXTINT Pin Interrupt	0	When set, this bit indicates a pending EXTINT1 interrupt (INT13). It is cleared when the interrupt vectors to 203AH.
6	FIFO_PEND	HSI FIFO Full Interrupt	0	When set, this bit indicates a pending HSI FIFO Full interrupt (INT14). It is cleared when the interrupt vectors to 203CH.
7	NMI_PEND	NMI	0	When set, this bit indicates a pending NMI interrupt (INT15). It is cleared when the interrupt vectors to 203EH.

Input/Output Control Register 0

IOC0
15H
HWindow 0 (Write), HWindow 15 (Read)

The IOC0 register selects the external clock and reset sources for Timer 2 and enables or disables the HSI input function of the four HSI pins. When IOC0 is read in HWindow 15, IOC0.1 will always read as "1" because its value is not latched.

IOC0



IOC0

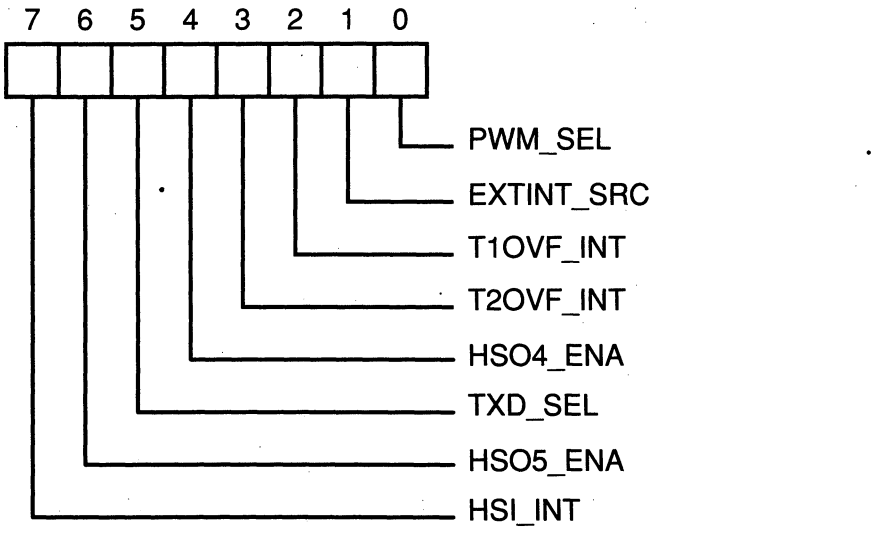
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	HSI0_ENA	Enable HSI.0 as HSI input	0	This bit controls whether events on the HSI.0 pin are loaded into the HSI FIFO. 1= enabled as HSI input 0= disabled as HSI input
1	SW_T2RST	Timer 2 Software Reset	X	Writing a "1" to this bit resets Timer 2. This bit will always read back as "1" in HWindow 15. 1= reset Timer 2 each write 0= no action
2	HSI1_ENA	Enable HSI.0 as HSI input	0	This bit controls whether events on the HSI.1 pin are loaded into the HSI FIFO. 1= enabled as HSI input 0= disabled as HSI input
3	T2RST_ENA	Timer 2 External Reset Source	0	This bit enables external reset of Timer 2. The external reset source is the rising edge of either T2RST or HSI.0, as selected by IOC0.5. 1= enable external reset 0= disable
4	HSI2_ENA	Enable HSI.0 as HSI input	0	This bit controls whether events on the HSI.2 pin are loaded into the HSI FIFO. 1= enabled as HSI input 0= disabled as HSI input
5	T2RST_SRC	Timer 2 Reset Source	0	This bit selects the external reset source for Timer 2. IOC0.3 must be set to enable the external reset. 1= HSI.0 pin rising edge 0= T2RST pin (P2.4) rising edge
6	HSI3_ENA	Enable HSI.0 as HSI input	0	This bit controls whether events on the HSI.3 pin are loaded into the HSI FIFO. 1= enabled as HSI input 0= disabled as HSI input
7	T2CLK_SRC	Timer 2 Clock Source	0	This bit selects the external clock source for Timer 2. IOC3.0 must be cleared to enable the external clock source. 1= HSI.1 pin 0= T2CLK pin (P2.3)

Input/Output Control Register 1

IOC1
16H
HWindow 0 (Write), HWindow 15 (Read)

The IOC1 register selects the output functions of P2.5 and P2.0; enables or disables HSO.4 and HSO.5 as outputs; and selects interrupt sources for EXTINT (INT07, 200EH), Timer Overflow (INT00, 2000H), and HSI Data Available (INT02, 2004H).

IOC1



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	PWM_SEL	Select P2.5/ PWM Output	1	This bit controls whether P2.5 functions as a PWM output pin or as a standard output port pin. 1= PWM output pin 0= standard output port pin

IOC1

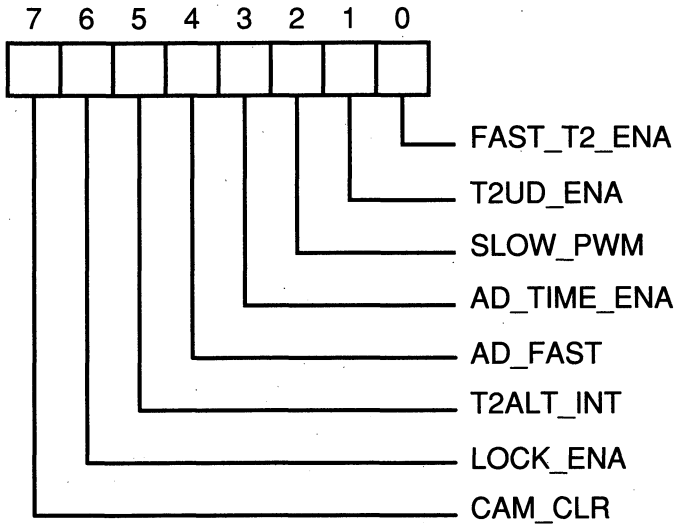
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
1	EXTINT_SRC	Select External Interrupt INT07 Source	0	This bit selects the EXTINT external interrupt source (INT07, 200EH). INT_MASK.7 must be set to enable the interrupt. 1= P0.7 0= P2.2
2	T1OVF_INT	Enable Timer 1 Overflow Interrupt	0	Both Timer 1 and Timer 2 can generate the Timer Overflow interrupt (INT00, 2000H). This bit controls whether an overflow on Timer 1 generates the interrupt. INT_MASK.0 must be set to enable the interrupt. IOS1.5 indicates the interrupt status. 1= enable Timer 1 as source 0= disable Timer 1 as source
3	T2OVF_INT	Enable Timer 2 Overflow Interrupt	0	Both Timer 1 and Timer 2 can generate the Timer Overflow interrupt (INT00, 2000H). This bit controls whether an overflow on Timer 2 generates the interrupt. INT_MASK.0 must be set to enable the interrupt. IOS1.4 indicates the interrupt status. 1= enable Timer 2 as source 0= disable Timer 2 as source
4	HSO4_ENA	Enable HSO.4 Pin as Output	0	HSO.4 is multiplexed with the HSI.2 input pin. This bit enables the output function of HSO.4. 1= enabled as output 0= disabled as output
5	TXD_SEL	Select P2.0/ TXD Output	1	This bits controls whether P2.0 functions as the TXD output of the serial port transmitter or as a standard output port pin. 1= serial port TXD output 0= standard output port pin
6	HSO5_ENA	Enable HSO.5 Pin as Output	0	HSO.5 is multiplexed with the HSI.3 input pin. This bit enables the output function of HSO.5. 1= enabled as output 0= disabled as output
7	HSI_INT	Select HSI Interrupt Source	0	This bit selects the source of the HSI Data Available interrupt (INT02, 2004H). INT_MASK.2 must be set to enable the interrupt. 1= HSI FIFO full 0= HSI Holding Register loaded

Input/Output Control Register 2

IOC2
0BH
HWindow 0 (Write), HWindow 15 (Read)

The IOC2 register controls three Timer 2 options, the clock prescalers for the PWM and the A/D converter, and the source for A/D conversion time determination. IOC2 also enables and disables locking commands into the HSO CAM, and it can clear all entries from the HSO CAM.

IOC2



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	FAST_T2_ENA	Enable Timer 2 Fast Increment	0	This bit controls whether Timer 2 operates in fast increment or normal mode. 1= fast increment mode; count every state 0= normal mode; count every eight states When fast increment mode is enabled, do not use Timer 2 as the HSO reference and do not reset Timer 2.
1	T2UD_ENA	Enable Timer 2 Up/Down Count	0	This bit controls whether Timer 2 functions as an up counter or as an up/down counter 1= if P2.6 = 1, count down if P2.6 = 0, count up 0= count up only

IOC2

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
2	SLOW_PWM	Enable PWM Clock Prescaler	0	This bit controls the PWM output period by enabling or disabling a clock prescaler (divide-by-two) on PWM.1, PWM.2, and PWM.3. 1= enable; PWM output period is 512 state times 0= disable; PWM output period is 256 state times
3	AD_TIME_ENA	Enable AD_TIME Register	0	This bit selects whether the A/D conversion times are controlled by the AD_TIME register or by the fast and normal conversion modes of the 80C196KB. 1= AD_TIME register 0= 80C196KB-compatible mode When this bit is clear, IOC2.4 enables or disables the A/D clock prescaler for complete 80C196KB compatibility.
4	AD_FAST	Disable A/D Clock Prescaler	0	In 80C196KB-compatible mode (IOC2.3 cleared), this bit controls the A/D conversion time period by enabling or disabling the A/D clock prescaler (divide-by-two). 1= disable; conversion time is 89.5 state times, 80C196KB normal mode 0= enable; conversion time is 156.5 state times, 80C196KB fast mode If IOC2.3 is set, this bit is ignored.
5	T2ALT_INT	Select Timer 2 Overflow Boundary	0	This bit selects the overflow boundary for the Timer 2 Overflow interrupt (INT12, 2038H). INT_MASK1.4 must be set to enable the interrupt. 1=7FFFH/8000H boundary 0=0FFFFH/0000H boundary
6	LOCK_ENA	Enable Locked CAM Entries	0	This bit enables and disables command locking. When this bit is set, HSO_COMMAND.7 controls whether individual commands are locked into the CAM or cleared after execution. 1= Enable command locking 0= Disable command locking Writing a "1" to IOC2.7 clears all entries (locked or not) from the CAM, as does a chip reset.
7	CAM_CLR	Clear All CAM Entries	X	Setting this bit clears all entries (even locked entries) from the HSO CAM. This bit is not latched; it will always read as "1" in HWindow 15.

Input/Output Control Register 3

IOC3
0CH
HWindow 1 (Read/Write)

The IOC3 register selects either an internal or an external clock source for Timer 2 and selects the function of pin P1.2 and pin P1.3. (This register was previously called T2CONTROL or T2CNTC.)

IOC3

7	6	5	4	3	2	1	0
R	R	R	R				

- 0: T2_ENA
- 1: Reserved (8XC196KC , earlier versions) / CLKOUT_DIS (8XC196KD and 8XC196KC (C-Step))
- 2: PWM1_SEL
- 3: PWM2_SEL

A0055-B0

IOC3

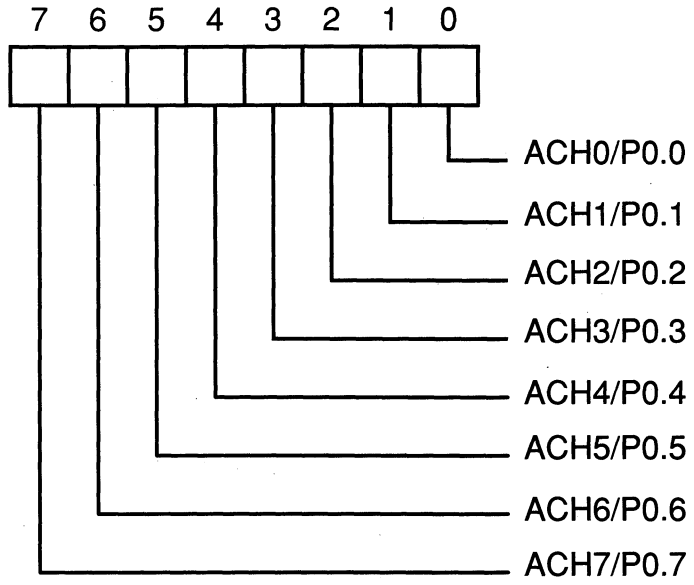
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	T2_ENA	Timer 2 Internal Clock Enable	0	This bit controls whether Timer 2 is clocked internally or externally. 1= internal source 0= external source: if IOC0.7=1, HSI.1 if IOC0.7=0, T2CLK (P2.3) IOC2.0 controls whether Timer 2 counts every clock (fast increment mode) or every eight clocks (normal mode).
1	Reserved	Reserved	0	On earlier versions of the 8XC196KC, this bit is reserved; always write as zero. On the 8XC196KC (B-Step), this bit will always read back as "1" in HWindow 1 (precharged bus).
	CLKOUT_DIS	CLKOUT Disable	0	This bit has been implemented on the 8XC196KC (C-Step) and 8XC196KD to enable or disable the CLKOUT signal. This can be used to reduce noise in systems that do not require the CLKOUT signal. The actual value of the bit will read back in HWindow 1. 1= disable CLKOUT 0= enable CLKOUT
2	PWM1_SEL	PWM1 Select	0	This bit selects the P1.3 pin function. 1= PWM1 output 0= quasi-bidirectional port pin When this bit is set, P1.3 has strong pull-ups and pull-downs. This pin can be switched between functions without a device reset.
3	PWM2_SEL	PWM2 Select	0	This bit selects the P1.4 pin function. 1= PWM2 output 0= quasi-bidirectional port pin When this bit is set, P1.4 has strong pull-ups and pull-downs. This pin can be switched between functions without a device reset.
4–7	—	—	1111	Reserved; always write as zero.

Input/Output Port 0 Register

IOPORT0
0EH
HWindow 0 (Read)

Port 0 is an input-only port. To reduce noise, Port 0 is monitored only when a read occurs. The pins can be used as analog inputs to the A/D converter (ACH*x*) and digital inputs (P0.*x*) at the same time, but this is not recommended. Pin P0.7 can also be configured as an external interrupt.

IOPORT0



A0056-0A

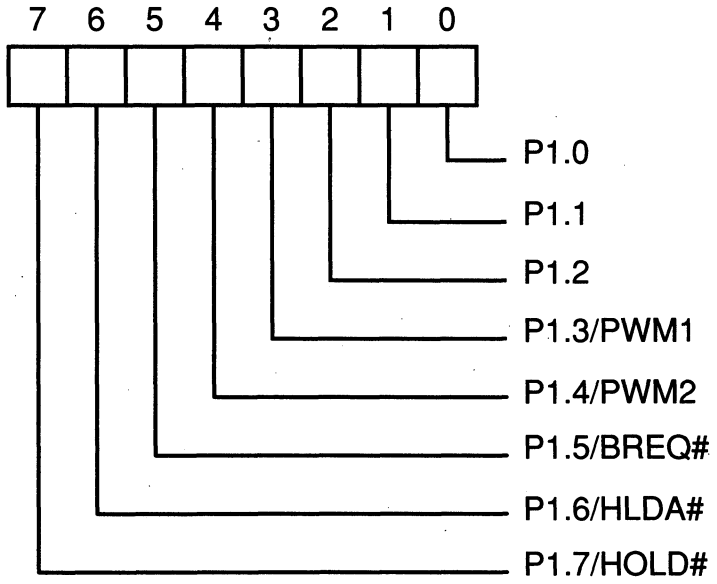
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	ACH0/P0.0	ACH0/P0.0	X	Analog Channel 0/Input Pin P0.0
1	ACH1/P0.1	ACH1/P0.1	X	Analog Channel 1/Input Pin P0.1
2	ACH2/P0.2	ACH2/P0.2	X	Analog Channel 2/Input Pin P0.2
3	ACH3/P0.3	ACH3/P0.3	X	Analog Channel 3/Input Pin P0.3
4	ACH4/P0.4	ACH4/P0.4	X	Analog Channel 4/Input Pin P0.4
5	ACH5/P0.5	ACH5/P0.5	X	Analog Channel 5/Input Pin P0.5
6	ACH6/P0.6	ACH6/P0.6	X	Analog Channel 6/Input Pin P0.6
7	ACH7/P0.7	ACH7/P0.7	X	Analog Channel 7/Input Pin P0.7

Input/Output Port 1 Register

IOPORT1
0FH
HWindow 0 (Read/Write)

All Port 1 pins are quasi-bidirectional unless the alternate function is selected. Three pins share functions with the bus-hold signals; two pins share functions with PWM outputs. When the pins are configured as I/O pins, they can be read or written. When the pins are configured for their alternate functions, they can be read but not written.

IOPORT1



IOPORT1

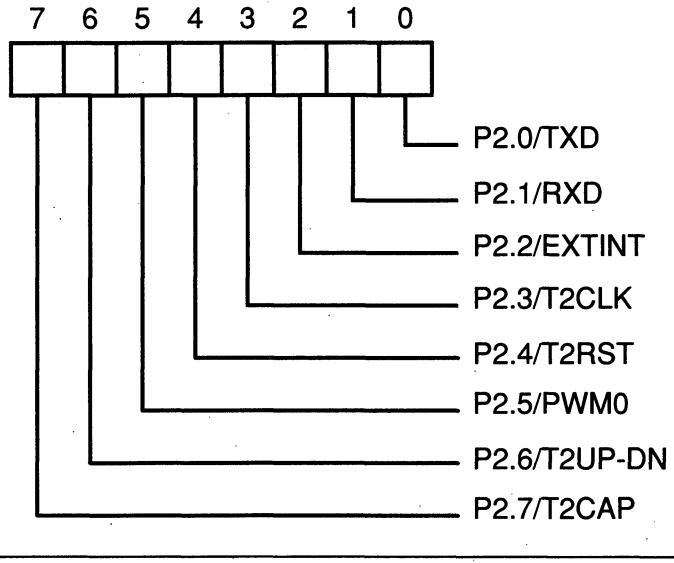
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	P1.0	P1.0	1	I/O Pin P1.0
1	P1.1	P1.1	1	I/O Pin P1.1
2	P1.2	P1.2	1	I/O Pin P1.2
3	P1.3/PWM1	P1.3/PWM1	1	I/O Pin P1.3/PWM1 Output Setting IOC3.2 enables P1.3 as the PWM1 output pin.
4	P1.4/PWM2	P1.4/PWM2	1	I/O Pin P1.4/PWM2 Output Setting IOC3.3 enables P1.4 as the PWM2 output pin.
5	P1.5/BREQ#	P1.5/ BREQ#	1	I/O Pin P1.5/Bus Request Setting WSR.7 enables P1.5 as BREQ#. Once the HOLD protocol is enabled, the pin functions as BREQ# until the device is reset. BREQ# is activated as an output when the bus controller has a pending external memory cycle. Once BREQ# is asserted, it remains asserted until the HOLD# is removed.
6	P1.6/HLDA#	P1.6/ HLDA#	1	I/O Pin P1.6/Hold Acknowledge Setting WSR.7 enables P1.6 as HLDA#. Once the HOLD protocol is enabled, the pin functions as HLDA# until the device is reset. HLDA# is activated as an output when the 8XC196KC/KD releases the bus in response to another device asserting HOLD#.
7	P1.7/HOLD#	P1.7/ HOLD#	1	I/O Pin P1.7/Hold Input Setting WSR.7 enables P1.7 as HOLD#. Once the HOLD protocol is enabled, the pin functions as HOLD# until the device is reset. HOLD# is activated as an input by a device to request control of the bus.

Input/Output Port 2 Register

IOPORT2
10H
HWindow 0 (Read/Write)

Port 2 contains input-only, output-only, and quasi-bidirectional port pins. The alternate functions must be enabled through the appropriate control registers.

IOPORT2



IOPORT2

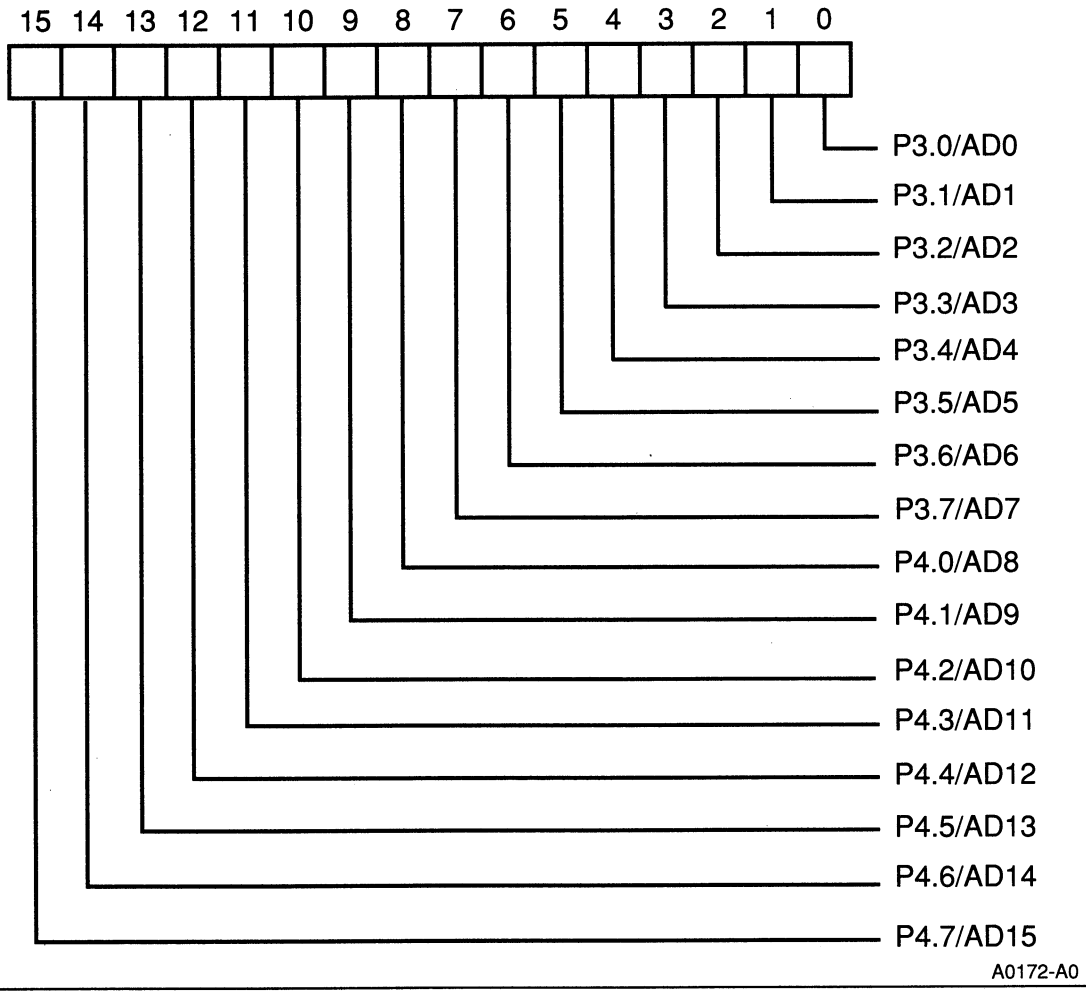
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	P2.0/TXD	P2.0/TXD	1	Output Pin P2.0 Setting IOC1.5 enables the pin as TXD, which serves as the transmit pin for serial port modes 1, 2, and 3 and the shift clock for mode 0.
1	P2.1/RXD	P2.1/RXD	0	Input Pin P2.1 Setting SP_CON.3 enables the pin as RXD. In modes 1, 2, and 3, RXD is used to receive serial port data. In mode 0, it functions as an input or an open-drain output for data
2	P2.2/EXTINT	P2.2/EXTINT	0	Input Pin 2.2. Clearing IOC1.1 selects P2.2 as the source for the EXTINT interrupt (INT07, 200EH). P2.2 can generate either EXTINT (INT07) or EXTINT1 (INT13, 203AH).
3	P2.3/T2CLK	P2.3/T2CLK	0	Input Pin P2.3 Clearing IOC0.7 enables the pin as the external clock input for Timer 2.
4	P2.4/T2RST	P2.4/T2RST	0	Input Pin P2.4 Clearing IOC0.5 enables the pin as the external reset to Timer 2. IOC0.3 must be set to enable the external reset.
5	P2.5/PWM0	P2.5/PWM0	0	Output Pin P2.5 Setting IOC1.0 enables this pin as the PWM0 output.
6	P2.6/T2UP-DN	P2.6/ T2UP-DN	1	Quasi-bidirectional pin P2.6. Setting IOC2.1 enables the pin as the direction control for Timer 2. Timer 2 counts up when the pin is low and counts down when the pin is high.
7	P2.7/T2CAP	P2.7/T2CAP	1	Quasi-bidirectional pin P2.7 A rising edge on P2.7 captures the value of Timer 2 in the T2CAPTURE register and generates a Timer 2 Capture interrupt (INT11, 2036H).

Input/Output Ports 3 and 4 Register

IOPORT34
1FFEH

Ports 3 and 4 contain bidirectional port pins with open-drain outputs. The pins are shared with the multiplexed address/data bus. The pins automatically switch to their system bus functions when EA# is low and to their open-drain port functions when EA# is high. Ports 3 and 4 can be read and written only as a word, at location 1FFEH.

IOPORT34



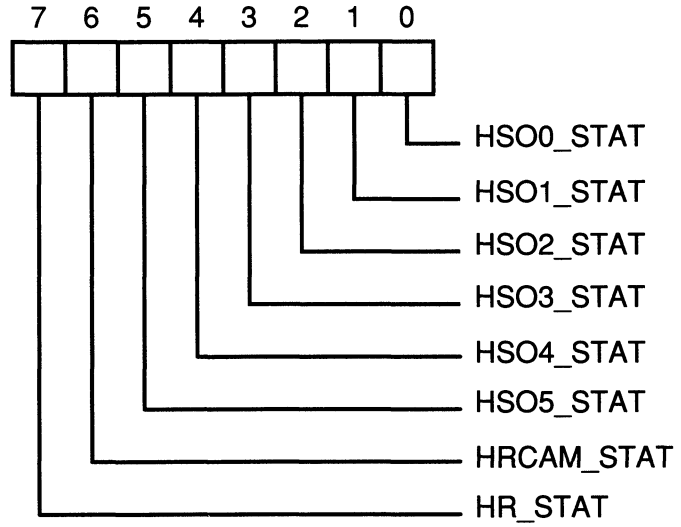
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	P3.0–P3.7 /AD0–AD7	P3.0–P3.7 /AD0–AD7	1111 1111	Bidirectional port pins P3.0–P3.7 during external accesses (EA# = 0); otherwise, AD0–AD7.
8–15	P4.0–P4.7 /AD8–AD15	P4.0–P4.7 /AD8–AD15	1111 1111	Bidirectional port pins P4.0–P4.7 during external accesses (EA# = 0); otherwise, AD8–AD15.

Input/Output Status Register 0

IOS0
15H
HWindow 0 (Read), HWindow 15 (Write)

The IOS0 register indicates the current state of the HSO pins. Writing to the corresponding bits (IOS0.0–IOS0.5) in HWindow 15 can set or clear the HSO pins. IOS0.6 and IOS0.7 indicate the current state of the HSO CAM file and the HSO holding register. (IOS0.6 and IOS0.7 cannot be written.)

IOS0



IOS0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	HSO0_STAT	HSO.0 State	0	Current state of the HSO.0 pin.
1	HSO1_STAT	HSO.1 State	0	Current state of the HSO.1 pin.
2	HSO2_STAT	HSO.2 State	0	Current state of the HSO.2 pin.
3	HSO3_STAT	HSO.3 State	0	Current state of the HSO.3 pin.
4	HSO4_STAT	HSO.4 State	0	Current state of the HSO.4 pin. HSO.4 is a bidirectional port pin and is multiplexed with the HSI.2 pin. Setting IOC1.4 enables the output function of HSO.4.
5	HSO5_STAT	HSO.5 State	0	Current state of the HSO.5 pin. HSO.5 is a bidirectional port pin and is multiplexed with the HSI.3 pin. Setting IOC1.6 enables the output function of HSO.5.
6	HRCAM_STAT	HSO CAM and Holding Register State	0	Current state of the HSO holding register and CAM. 0= HSO holding register is empty and at least one CAM slot is empty 1= HSO holding register is full To avoid overwriting a current value, do not write to the holding register until either this bit or IOS0.7 is cleared.
7	HR_STAT	HSO Holding Register State	0	Current state of the HSO holding register. 0= HSO holding register is empty 1= HSO holding register is full To avoid overwriting a current value, do not write to the holding register until either this bit or IOS0.6 is cleared.

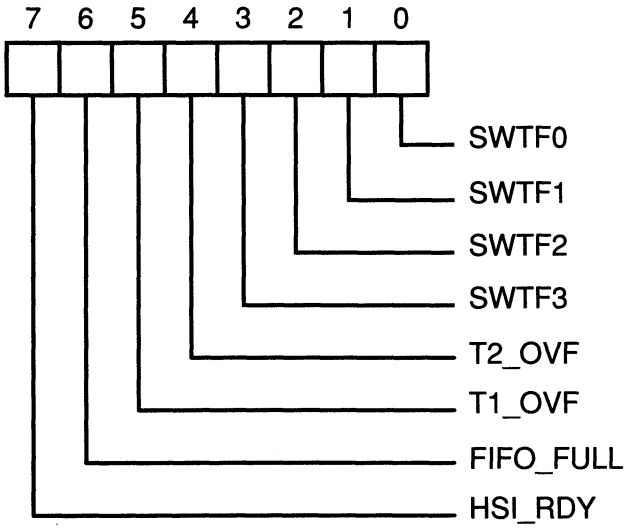
Input/Output Status Register 1

IOS1
16H
HWindow 0 (Read), HWindow 15 (Write)

The IOS1 register contains flags that indicate which events triggered interrupts. IOS1.0 through IOS1.5 indicate the status of software timers, Timer 2, and Timer 1. Reading IOS1 clears bits IOS1.0–IOS1.5. Writing to IOS1.0–IOS1.5 sets or clears the bits, but does not trigger interrupts.

IOS1.6 and IOC1.7 indicate the status of the HSI FIFO register and the HSI holding register. IOS1.6 and IOS1.7 cannot be written.

IOS1



IOS1

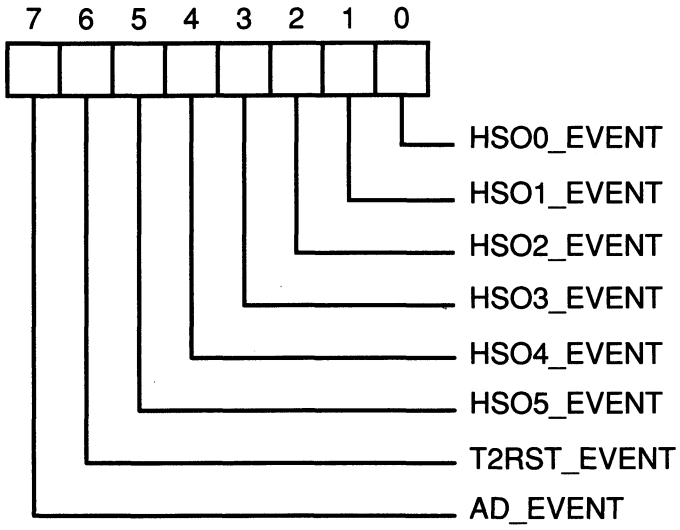
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	SWTF0	Software Timer 0 Flag	0	This bit, when set, indicates that Software Timer 0 has expired, triggering INT05 (200AH). INT_MASK.5 must be set to enable the interrupt.
1	SWTF1	Software Timer 1 Flag	0	This bit, when set, indicates that Software Timer 1 has expired, triggering INT05 (200AH). INT_MASK.5 must be set to enable the interrupt.
2	SWTF2	Software Timer 2 Flag	0	This bit, when set, indicates that Software Timer 2 has expired, triggering INT05 (200AH). INT_MASK.5 must be set to enable the interrupt.
3	SWTF3	Software Timer 3 Flag	0	This bit, when set, indicates that Software Timer3 has expired, triggering INT05 (200AH). INT_MASK.5 must be set to enable the interrupt.
4	T2_OVF	Timer 2 Overflow Flag	0	Both Timer 1 and Timer 2 can generate a Timer Overflow interrupt (INT00, 2000H). This bit, when set, indicates that Timer 2 triggered the interrupt. INT_MASK.0 must be set to enable the interrupt.
5	T1_OVF	Timer 1 Overflow Flag	0	Both Timer 1 and Timer 2 can generate a Timer Overflow interrupt (INT00, 2000H). This bit, when set, indicates that Timer 1 triggered the interrupt. INT_MASK.0 must be set to enable the interrupt.
6	FIFO_FULL	Sixth FIFO Entry Flag	0	This bit, when set, indicates that the HSI FIFO has six or more entries, independent of the holding register. This event can generate either an HSI Data Available interrupt (INT02, 2004H) or an HSI FIFO Full interrupt (INT14, 203CH), but should not be configured for both.
7	HSI_RDY	HSI Holding Register Data Ready	0	This bit, when set, indicates that the HSI holding register has been loaded. When IOC1.7 is clear, this event generates an HSI Data Available interrupt (INT02, 2004H). INT_MASK.2 must be set to enable the interrupt.

Input/Output Status Register 2

IOS2
17H
HWindow 0 (Read), HWindow 15 (Write)

The IOS2 register contains flags that indicate which HSO events have occurred. Writing to IOS2 sets or clears the status bits, but does not trigger interrupts. Reading IOS2 clears all bits.

IOS2



A0061-A0

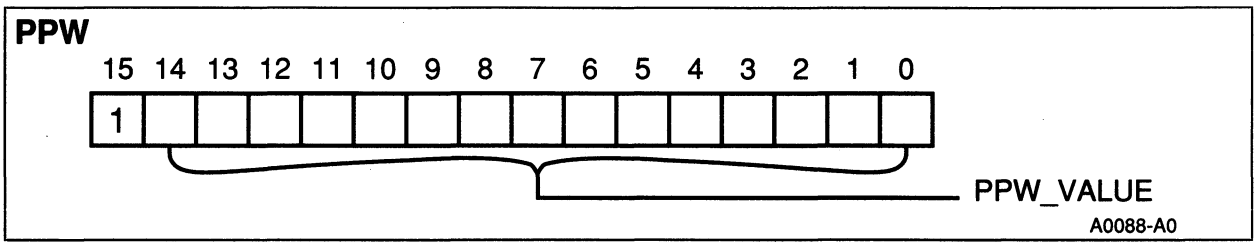
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	HSO0_EVENT	HSO.0 Pin Event	0	This bit, when set, indicates that an HSO command toggled the HSO.0 pin.
1	HSO1_EVENT	HSO.1 Pin Event	0	This bit, when set, indicates that an HSO command toggled the HSO.1 pin.
2	HSO2_EVENT	HSO.2 Pin Event	0	This bit, when set, indicates that an HSO command toggled the HSO.2 pin.
3	HSO3_EVENT	HSO.3 Pin Event	0	This bit, when set, indicates that an HSO command toggled the HSO.3 pin.
4	HSO4_EVENT	HSO.4 Pin Event	0	This bit, when set, indicates that an HSO command toggled the HSO.4 pin.
5	HSO5_EVENT	HSO.5 Pin Event	0	This bit, when set, indicates that an HSO command toggled the HSO.5 pin.
6	T2RST_EVENT	Timer 2 Reset Event	0	This bit, when set, indicates that an HSO command reset Timer 2.
7	AD_EVENT	A/D Conversion Start Event	0	This bit, when set, indicates that an HSO command started an A/D conversion.

Programming Pulse Width Register

PPW
(no direct access)

The Programming Pulse Width register is accessible only during Auto Programming mode. It is loaded from external address 4015/4014H.

The value in the PPW register determines the programming pulse width. The programming pulse width must be at least 100µs for programming to function correctly. The most-significant bit (PPW.15) must always be set. The high byte of PPW usually contains 80H and the low byte usually contains 05H, although they can hold other values.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–14	PPW_VALUE	Programming Pulse Width	0000 0101 0000 000	These bits usually equal 05H, the correct value for XTAL1 = 8 MHz. Write the desired PPW_VALUE to these bits.
15	PPW_MSB	PPW Most-Significant Bit	1	This bit must always equal "1."

Use the following formula and round the result to the next higher integer value to determine the proper PPW_VALUE.

$$PPW\_VALUE = (0.6944 \times F_{OSC}) - 1$$

where:

PPW_VALUE is a 15-bit word

F_{OSC} is the XTAL1 frequency, in MHz

For example, assume XTAL1 is 8 MHz:

$$\begin{aligned} PPW\_VALUE &= (0.6944 \times 8) - 1 \\ &= 5.5552 - 1 \\ &= 4.5552 \\ &\equiv 5 \end{aligned}$$

Program Status Word

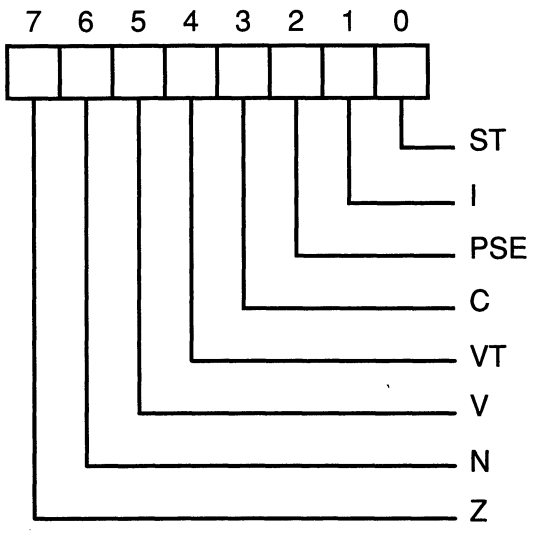
PSW
(no direct access)

The PSW actually consists of two bytes. The high byte is the status word, which is described here; the low byte is the INT_MASK register. The status word contains one bit (PSW.1) that globally enables or disables servicing of all maskable interrupts, one bit (PSW.2) that enables or disables the Peripheral Transaction Server (PTS), and six Boolean flags that reflect the state of a user's program.

The status word portion of the PSW cannot be accessed directly. To access the status word, push the value onto the stack (PUSHF), then pop the value to a register (POP *test_reg*). The PUSHF and PUSHA instructions save the PSW in the system stack; POPF and POPA restore it.

The EI and DI instructions set and clear PSW.1; the EPTS and DPTS instructions set and clear PSW.2. Various instructions test, set, and clear the Boolean flags. (Appendix B contains one table that shows the effect of instructions on the PSW flags and one that shows the effect of PSW flags on conditional jump instructions.)

PSW



A0038-A0

PSW

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	ST	Sticky Bit Flag		This flag is set to indicate that, during a right shift, a "1" has been shifted into the Carry flag and then shifted out. This bit is undefined after a multiply operation. The Sticky Bit flag can be used with the Carry flag to allow finer resolution in rounding decisions. (See the description of the Carry flag for details.)
1	I	Interrupt Disable (Global)		This bit globally enables or disables the servicing of all maskable interrupts (that is, all interrupts except NMI, TRAP, and Unimplemented Opcode). The bits in INT_MASK and INT_MASK1 individually enable or disable the interrupts. The EI instruction sets this bit; DI clears it. 1= enable interrupt servicing 0= disable interrupt servicing
2	PSE	PTS Enable		This bit globally enables or disables the Peripheral Transaction Server (PTS). The EPTS instruction sets this bit; DPTS clears it. 1= enable PTS 0= disable PTS
3	C	Carry Flag		This flag is set to indicate the state of an arithmetic carry from the most-significant bit of the ALU or the state of the last bit shifted out of an operand. If a subtraction operation generates a borrow, the Carry flag is cleared. **C — Value of Bits Shifted Off** 0 — <½LSB 1 — ≥½LSB Normally, the result is rounded up if the Carry flag is set. The Sticky Bit flag allows a finer resolution in the rounding decision. **C ST — Value of Bits Shifted Off** 0 0 — = 0 0 1 — > 0 and < ½ LSB 1 0 — =½LSB 1 1 — > ½ LSB and < 1 LSB

PSW

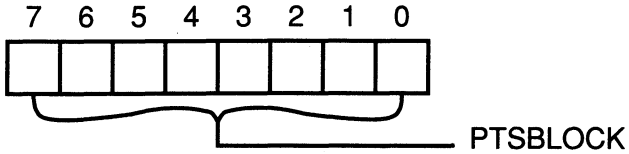
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
4	VT	Overflow-Trap Flag		This flag is set when the Overflow flag is set, but it is cleared only by the CLRVT, JVT, and JNVT instructions. This allows testing for a possible overflow condition at the end of a sequence of related arithmetic operations, which is generally more efficient than testing the Overflow flag after each operation.
5	V	Overflow Flag		This flag is set to indicate that an operation generated a result outside the range for the destination data type. For shift operations (SHL, SHLB, and SHLL), the flag is set if the most-significant bit of the operand changes during the shift. For divide operations, the flag is set under the following conditions: **Instruction** **Result** DIVU > 255 (0FFH) DIVUB > 65535 (0FFFFH) DIV < –127 (81H) or > +127 (7FH) DIVB < –32767 (8001H) or > +32767 (7FFFH)
6	N	Negative Flag		This flag is set to indicate that an operation generated a negative result. The flag is correct even if an overflow occurs. For all shift operations and the NORML instruction, the flag is set to equal the most-significant bit of the result, even if the shift count is zero.
7	Z	Zero Flag		This flag is set to indicate that the result of an operation was zero. For add-with-carry and subtract-with-borrow operations, the flag is never set, but it is cleared if the result is non-zero. This way, the Zero flag indicates the correct zero or non-zero result for multiple-precision calculations.

PTS Block Register

PTSBLOCK
Offset 7 from PTS Control Block

The PTSBLOCK register is used during block transfer, HSO, and HSI modes. PTSBLOCK controls the number of transfers that will take place.

PTSBLOCK



A0143-A0

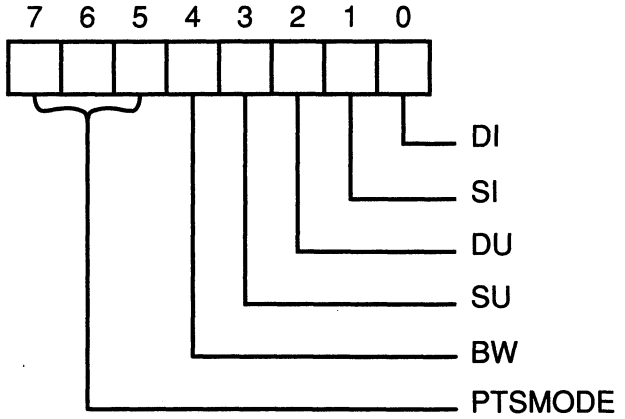
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	PTSBLOCK	PTS Block Count	XXXX XXXX	Controls the number of transfers that will take place. Values depend on the PTS mode: **Mode** **Values** Block transfer 1–32 HSI 1–7 HSO 1–8 In all modes, writing zero to this register causes the maximum number of transfers to take place (32 for block transfer mode, 7 for HSI mode, and 8 for HSO mode).

PTS Control Register

PTSCON
Offset 1 from PTS Control Block

Three bits of the PTSCON register determine the PTS mode: single transfer, block transfer, A/D, HSO, or HSI. The PTS mode defines the functions of the remaining five bits. PTSCON has one configuration for the single and block transfer modes and one for the AD, HSO, and HSI modes. The configurations are described separately here. (PSW.2, controlled by the DPTS and EPTS instructions, globally enables or disables the PTS.)

PTSCON (Single and Block Transfer Modes)

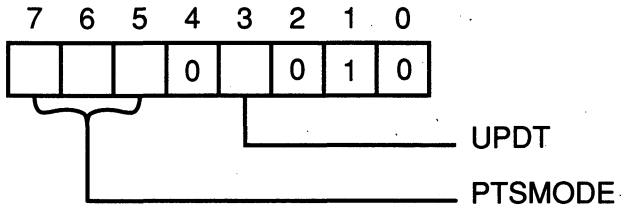


A0036-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	DI	PTSDST Auto-Increment	0	Setting this bit causes the PTS destination register to increment at the end of each PTS cycle.
1	SI	PTSSRC Auto-Increment	0	Setting this bit causes the PTS source register to increment at the end of each PTS cycle.
2	DU	Update PTSDST	0	Setting this bit causes the PTSDST register to retain its final value at the end of a PTS cycle. Clearing it causes the register revert to the value that existed at the beginning of the PTS cycle.
3	SU	Update PTSSRC	0	Setting this bit causes the PTSSRC register to retain its final value at the end of a PTS cycle. Clearing it causes the register to revert to the value that existed at the beginning of the PTS cycle.
4	BW	Byte/Word Transfer	0	Setting this bit specifies a byte transfer. Clearing it specifies a word transfer.
5–7	PTSMODE	PTS Mode	000	These bits specify the PTS mode: **Bit 7 6 5** 0 0 0 Single Transfer 1 0 0 Block Transfer

PTSCON

PTSCON (A/D, HSO, and HSI Modes)



A0037-A0

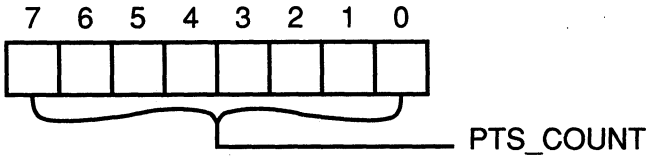
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	—	—	0	Always zero.
1	—	—	1	Always one.
2	—	—	0	Always zero.
3	UPDT	Update Register	0	Setting this bit causes the associated register to be loaded with the value that exists at the end of a PTS cycle. Clearing it causes the register to be loaded with the value that existed at the beginning of the PTS cycle. **Mode Register** A/D PTS_S/D HSI PTSDST HSO PTSSRC
4	—	—	0	Always zero.
5–7	PTSMODE	PTS Mode	000	These bits specify the PTS mode: **Bit 7 6 5** 1 1 0 A/D 0 1 1 HSO 0 0 1 HSI

PTS Count Register

PTSCOUNT
Offset 0 from PTS Control Block

The PTSCOUNT register is used in all PTS modes. PTSCOUNT defines the number of PTS cycles to be executed consecutively without CPU intervention. Since PTSCOUNT is an 8-bit value, the maximum number of cycles is 256. PTSCOUNT is decremented at the end of each PTS cycle. When PTSCOUNT reaches zero, hardware clears the corresponding PTSSEL bit and sets the PTSSRV bit, which requests the end-of-PTS interrupt. When the end-of-PTS interrupt is called, hardware clears the PTSSRV bit. The PTSSEL bit must be set manually to re-enable the PTS channel.

PTSCOUNT



A0144-A0

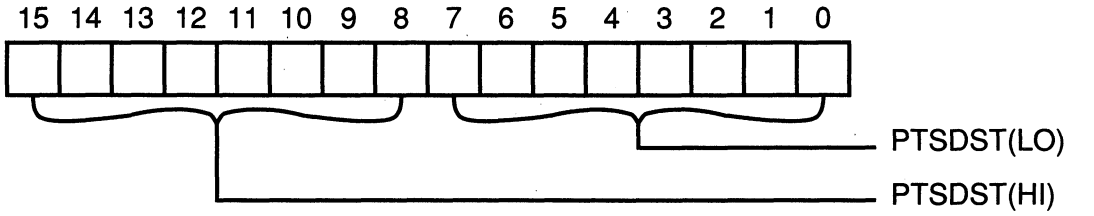
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	PTS_COUNT	Consecutive PTS Cycles	XXXX XXXX	Defines the number of PTS cycles to be executed consecutively without CPU intervention. Maximum value is 256.

PTS Destination Register

PTSDST
Offset 4 from PTS Control Block

The PTSDST register is used in single transfer, block transfer, and HSI modes. PTSDST points to the destination memory location. PTSDST is optionally incremented at the end of a PTS cycle. In single transfer mode, PTSCON.0 and PTSCON.2 control whether PTSDST is incremented. In block transfer mode, PTSCON.0 controls whether PTSDST is incremented after each transfer and PTSCON.2 controls whether PTSDST retains its final value or reverts to its original value. In HSI mode, PTSCON.3 determines whether PTSDST is updated at the end of the PTS cycle.

PTSDST



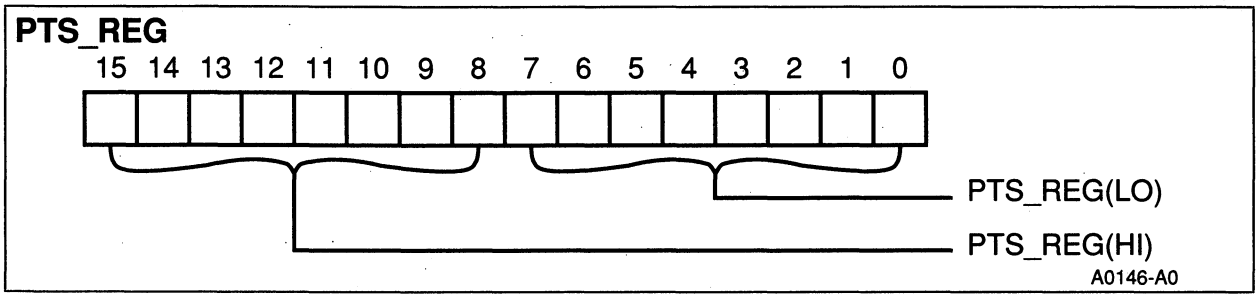
A0145-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	PTSDST (LO)	PTS Destination Address, Low Byte	XXXX XXXX	Low byte of the PTS destination address.
8–15	PTSDST (HI)	PTS Destination Address, High Byte	XXXX XXXX	High byte of the PTS destination address.

PTS AD Register

PTS_REG
Offset 3 from PTS Control Block

The PTS_REG register is used in A/D mode. PTS_REG points to address 02H. When read, this location contains the AD_RESULT register; when written, it contains the AD_COMMAND register.

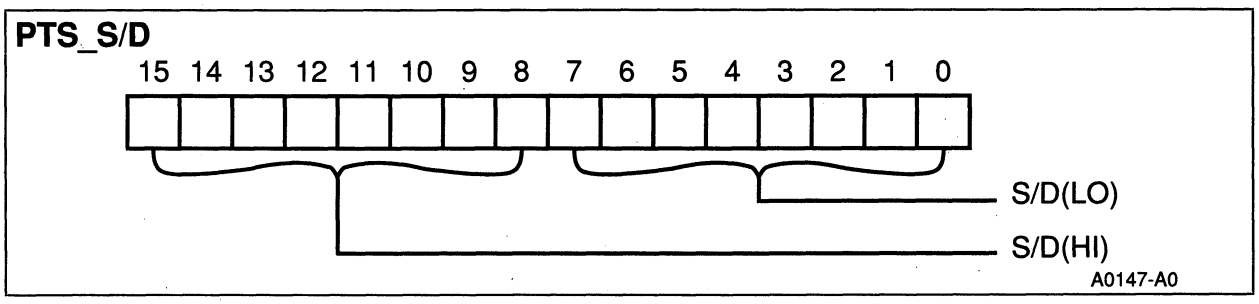


Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	PTS_REG (LO)	Register Address, Low Byte	XXXX XXXX	Low byte of the AD_RESULT register address.
8–15	PTS_REG (HI)	Register Address, High Byte	XXXX XXXX	High byte of the AD_RESULT register address.

PTS Source/Destination Register

PTS_S/D
Offset 3 from PTS Control Block

The PTS_S/D register is used in A/D mode. PTS_S/D points to the memory location that contains the A/D command/data table. In a PTS A/D cycle, the word that PTS_S/D points to is loaded into a temporary internal register, PTS_S/D is incremented by 2, then the AD_RESULT register is stored at the updated PTS_S/D address. PTSCON.3 controls whether PTS_S/D is updated at the end of a PTS cycle, to point to the next word in the A/D table.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	S/D (LO)	Source/ Destination Address, Low Byte	XXXX XXXX	Low byte of the source/destination address.
8–15	S/D (HI)	Source/ Destination Address, High Byte	XXXX XXXX	High byte of the source/destination address.

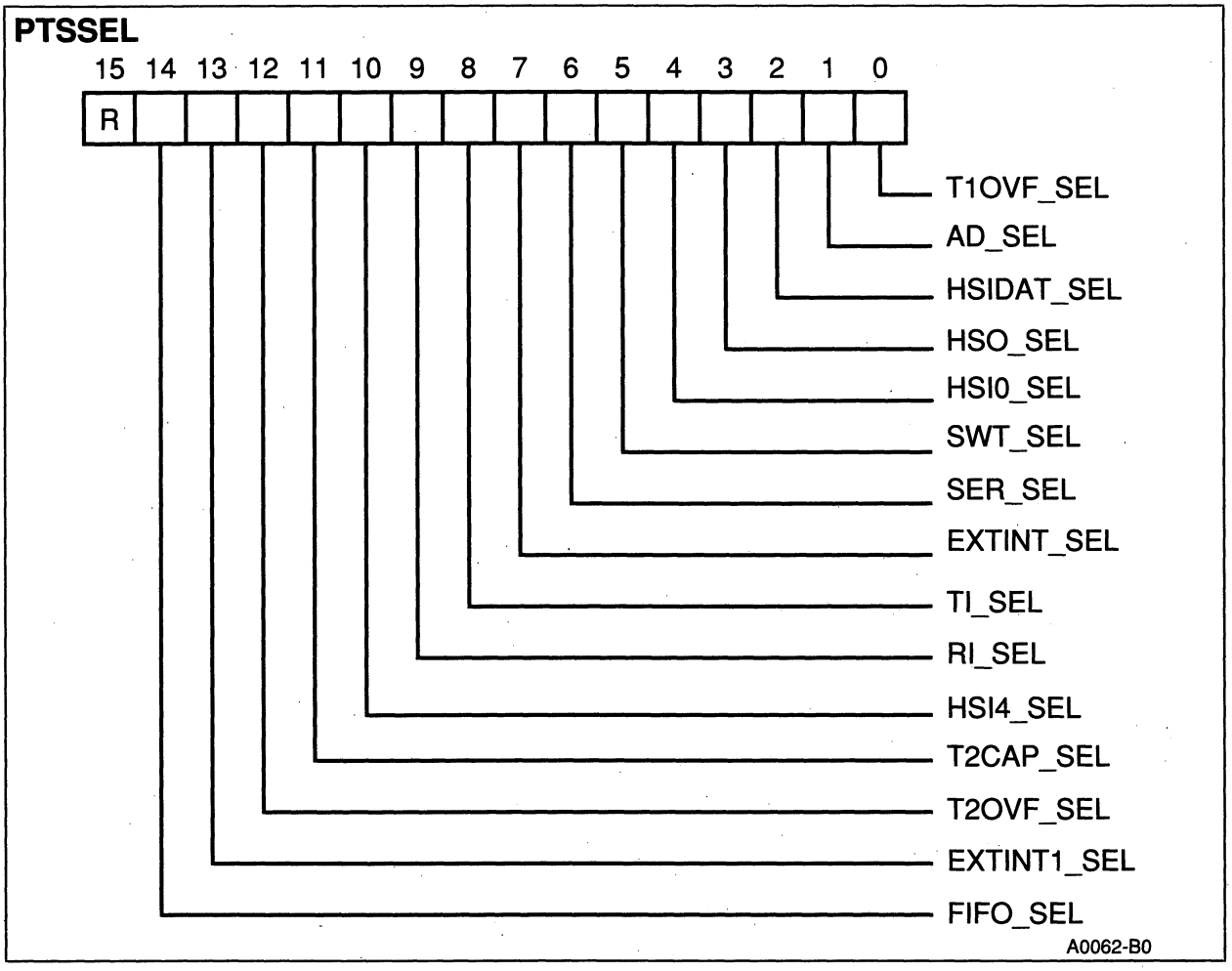
PTS Select Register (HI/LO)

PTSSEL
05/04H
HWindow 1 (Read/Write)

The PTSSEL register consists of two bytes. PTSSEL selects either a PTS cycle or a normal interrupt service routine for each of fifteen interrupt requests. Setting a bit selects a PTS cycle; clearing a bit selects a normal interrupt service routine.

When PTSCOUNT reaches zero, hardware clears the corresponding PTSSEL bit and sets the PTSSRV bit, which requests the end-of-PTS interrupt. When the end-of-PTS interrupt is called, hardware clears the PTSSRV bit. The PTSSEL bit must be set manually to re-enable the PTS channel.

Each interrupt can be masked by the corresponding bit in the INT_MASK or INT_MASK1 register. The PTS is globally enabled or disabled by PSW.2.



PTSSEL

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	T1OVF_SEL	Timer Overflow Interrupt Select	0	Setting this bit causes a Timer Overflow interrupt (INT00) to be handled by a PTS cycle.
1	AD_SEL	A/D Conversion Complete Interrupt Select	0	Setting this bit causes an A/D Conversion Complete interrupt (INT01) to be handled by a PTS cycle.
2	HSIDAT_SEL	HSI Data Available/ FIFO Full Interrupt Select	0	Setting this bit causes an HSI Data Available interrupt (INT02) to be handled by a PTS cycle.
3	HSO_SEL	HSO Output Event Interrupt Select	0	Setting this bit causes a High-Speed Output interrupt (INT03) to be handled by a PTS cycle.
4	HSI0_SEL	HSI.0 External Interrupt Select	0	Setting this bit causes an HSI.0 Pin interrupt (INT04) to be handled by a PTS cycle.
5	SWT_SEL	Software Timer Interrupt Select	0	Setting this bit causes a Software Timer interrupt (INT05) to be handled by a PTS cycle.
6	SER_SEL	Serial Port Interrupt Select	0	Setting this bit causes a Serial Port interrupt (INT06) to be handled by a PTS cycle.
7	EXTINT_SEL	EXTINT Pin or P0.7 Interrupt Select	0	Setting this bit causes an EXTINT pin or P0.7 interrupt (INT07) to be handled by a PTS cycle.

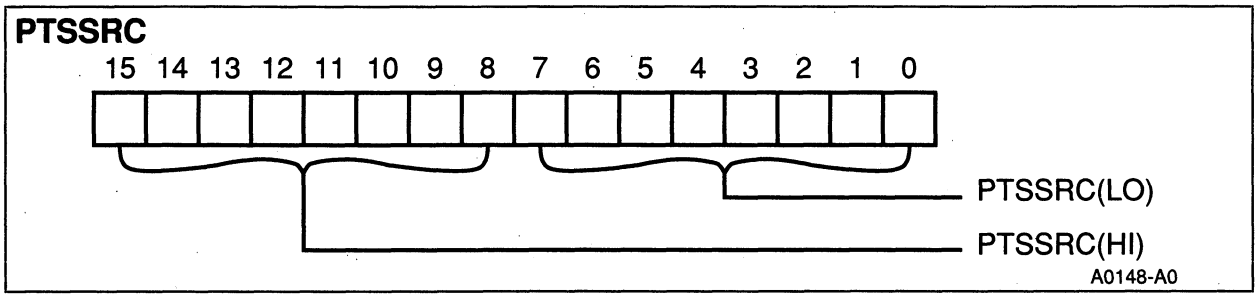
PTSSEL

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
8	TI_SEL	Transmit Interrupt Select	0	Setting this bit causes a TI interrupt (INT08) to be handled by a PTS cycle.
9	RI_SEL	Receive Interrupt Select	0	Setting this bit causes an RI interrupt (INT09) to be handled by a PTS cycle.
10	HSI4_SEL	HSI FIFO 4 Interrupt Select	0	Setting this bit causes an HSI FIFO 4 interrupt (INT10) to be handled by a PTS cycle.
11	T2CAP_SEL	Timer 2 Capture Interrupt Select	0	Setting this bit causes a Timer 2 Capture interrupt (INT11) to be handled by a PTS cycle.
12	T2OVF_SEL	Timer 2 Overflow Interrupt Select	0	Setting this bit causes a Timer 2 Overflow interrupt (INT12) to be handled by a PTS cycle.
13	EXTINT1_SEL	EXTINT Pin Interrupt Select	0	Setting this bit causes an EXTINT1 interrupt (INT13) to be handled by a PTS cycle.
14	FIFO_SEL	HSI FIFO Full Interrupt Select	0	Setting this bit causes an HSI FIFO Full interrupt (INT14) to be handled by a PTS cycle.
15	—	—	0	Reserved; always write as zero.

PTS Source Register

PTSSRC
Offset 2 from PTS Control Block

The PTSSRC register is used in single transfer, block transfer, and HSO modes. PTSSRC points to the source memory location. PTSSRC is optionally incremented at the end of a PTS cycle. In single transfer mode, PTSCON.1 and PTSCON.3 control whether PTSDST is incremented. In block transfer mode, PTSCON.1 controls whether PTSDST is incremented after each transfer and PTSCON.3 controls whether PTSDST retains its final value or reverts to its original value. In HSO mode, PTSCON.3 determines whether PTSSRC is updated at the end of the PTS cycle.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	PTSSRC (LO)	PTS Source Address, Low Byte	XXXX XXXX	Low byte of the PTS source address.
8–15	PTSSRC (HI)	PTS Source Address, High Byte	XXXX XXXX	High byte of the PTS source address.

PTS Service Register

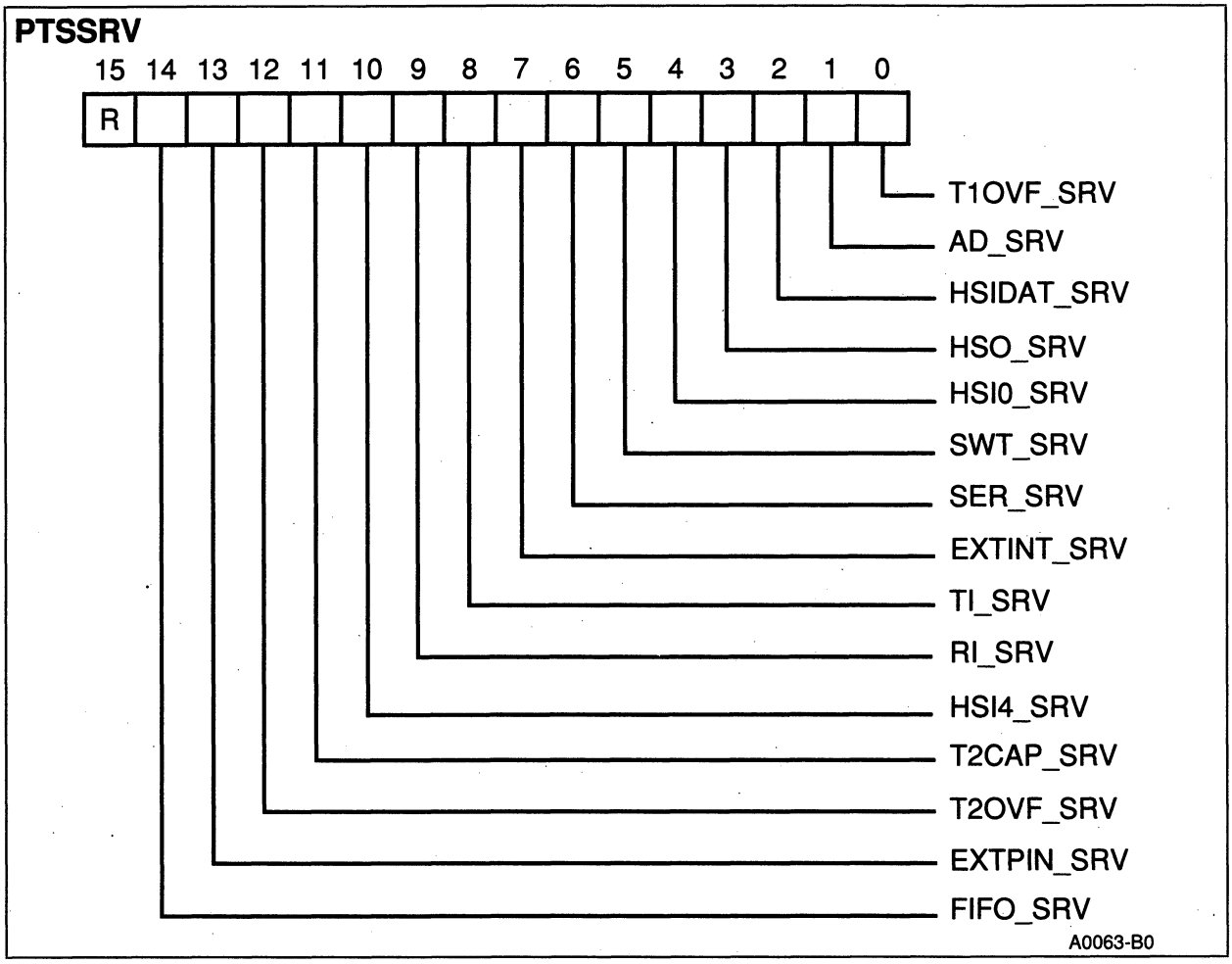
PTSSRV
07/06H
HWindow 1 (Read/Write)

The PTSSRV register consists of two bytes. PTSSRV is used by the hardware to indicate that the final PTS cycle has been serviced. When PTSCOUNT reaches zero, hardware clears the corresponding PTSSEL bit and sets the PTSSRV bit, which requests the end-of-PTS interrupt. When the end-of-PTS interrupt is called, hardware clears the PTSSRV bit. The PTSSEL bit must be set manually to re-enable the PTS channel.

The PTS is globally enabled or disabled by PSW.2, which is set with the EPTS instruction and cleared with the DPTS instruction. Interrupts are enabled or disabled (masked) by the corresponding bits in the INT_MASK and INT_MASK1 registers. Individual interrupts are enabled as PTS cycles by the corresponding bits in the PTSSEL register.

The end-of-PTS interrupt vectors through the same location that the corresponding normal interrupt vector would. For example, if PTSSEL.8 is set, the TI interrupt is handled by its PTS vector at 2050H with its end-of-PTS vector at 2030H. (Refer to Table C-4 for interrupt vector locations.)

PTSSRV


PTSSRV
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
R
T1OVF_SRV
AD_SRV
HSIDAT_SRV
HSO_SRV
HSI0_SRV
SWT_SRV
SER_SRV
EXTINT_SRV
TI_SRV
RI_SRV
HSI4_SRV
T2CAP_SRV
T2OVF_SRV
EXTPIN_SRV
FIFO_SRV
A0063-B0

PTSSRV

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0	T1OVF_SRV	Timer 1 Overflow Interrupt Serve	0	This bit is set when PTSCOUNT for the Timer 1 Overflow PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2000H.
1	AD_SRV	A/D Conversion Complete Interrupt Serve	0	This bit is set when PTSCOUNT for the A/D Complete PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2002H.
2	HSIDAT_SRV	HSI Data Available/ FIFO Full Interrupt Serve	0	This bit is set when PTSCOUNT for the HSI PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2004H.
3	HSO_SRV	HSO Output Event Interrupt Serve	0	This bit is set when PTSCOUNT for the HSO PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2006H.
4	HSI0_SRV	HSI.0 External Interrupt Serve	0	This bit is set when PTSCOUNT for the HSI.0 PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2008H.
5	SWT_SRV	Software Timer Interrupt Serve	0	This bit is set when PTSCOUNT for the Software Timer PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 200AH.
6	SER_SRV	Serial Port Interrupt Serve	0	This bit is set when PTSCOUNT for the Serial Port PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 200CH.
7	EXTINT_SRV	EXTINT Pin or P0.7 Interrupt Serve	0	This bit is set when PTSCOUNT for the EXTINT PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 200EH.

PTSSRV

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
8	TI_SRV	Transmit Interrupt Serve	0	This bit is set when PTSCOUNT for the TI PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2030H.
9	RI_SRV	Receive Interrupt Serve	0	This bit is set when PTSCOUNT for the RI PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2032H.
10	HSI4_SRV	HSI FIFO 4 Interrupt Serve	0	This bit is set when PTSCOUNT for the HSI4 PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2034H.
11	T2CAP_SRV	Timer 2 Capture Interrupt Serve	0	This bit is set when PTSCOUNT for the T2 Capture PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2036H.
12	T2OVF_SRV	Timer 2 Overflow Interrupt Serve	0	This bit is set when PTSCOUNT for the Timer 2 Overflow PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 2038H.
13	EXTPIN_SRV	EXTINT Pin Interrupt Serve	0	This bit is set when PTSCOUNT for the EXTPIN PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 203AH.
14	FIFO_SRV	HSI FIFO Full Interrupt Serve	0	This bit is set when PTSCOUNT for the FIFO PTS channel reaches zero, which initiates an end-of-PTS interrupt through location 203CH.
15	—	—	0	Reserved; always write as zero.

PWM0 Control Register

PWM0_CONTROL
17H
HWindow 0 (Write), HWindow 15 (Read)

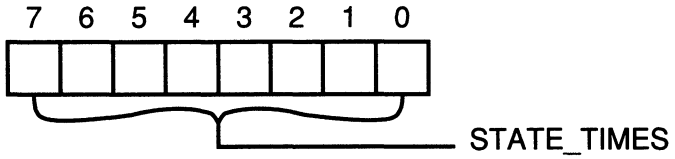
PWM0 is multiplexed with P2.5. IOC1.0 must be set to enable the PWM0 output function.

The PWM's eight-bit counter is incremented every state time (with the PWM prescaler disabled) or every two state times (with the PWM prescaler enabled). When the counter is equal to zero, the PWM0 output is driven high. It remains high until the counter value matches the value in this register, at which time the output is pulled low. When the counter overflows, the output is again switched high. When PWM0_CONTROL equals zero, the output is always low.

The PWM0_CONTROL register, in conjunction with IOC2.2, determines how long the PWM0 output is held high during the pulse, effectively controlling the duty cycle. The value written to PWM0_CONTROL register can be from 0 to 255 state times (0% to 99.6% duty cycle).

Setting IOC2.2 enables the PWM's divide-by-two clock prescaler; clearing IOC2.2 disables it. When the prescaler is enabled, the total length of the pulse is 512 state times and the PWM0_CONTROL value is multiplied by 4. When it is disabled, the total pulse length is 256 state times and the PWM0_CONTROL value is multiplied by 2.

PWM0_CONTROL



A0064-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	STATE_TIMES	PWM0 High State Times	0000 0000	These bits determine the number of state times that the PWM0 output is held high during the pulse. Write a hexadecimal value (00H – FFH) to this register.

PWM0_CONTROL

The following formulas are used to determine the PWM period and the time that the output is held high:

	Clock Prescaler Disabled (IOC2.2=0)	Clock Prescaler Enabled (IOC2.2=1)
PWM Period (in µsec.) =	$\frac{512}{F_{OSC}}$	$\frac{1024}{F_{OSC}}$
PWM*x* High (in µsec.) =	$\frac{PWMx\_CONTROL \times 2}{F_{OSC}}$	$\frac{PWMx\_CONTROL \times 4}{F_{OSC}}$

where:

F_{OSC} is the XTAL1 frequency, in MHz

For example, if F_{OSC} equals 16 MHz, then the period of the PWM output waveform is 32 µs. If IOC2.2 is clear and PWM0_CONTROL equals 8AH (138 decimal), PWM0 is held high for 17.25 µs (and low for 14.8 µs) of the total 32 µs, resulting in a duty cycle of approximately 54%. When IOC2.2 is set, the same values would produce a period of 64 µs and PWM0 would be held high for 34.5 µs (and low for 29.5 µs), for the same duty cycle, approximately 54%.

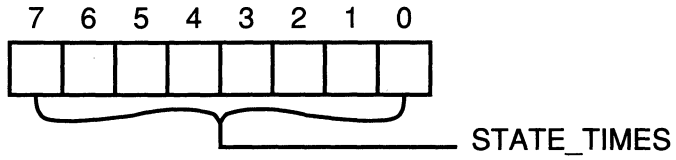
PWM1 Control Register

PWM1_CONTROL
16H
HWindow 1 (Read/Write)

PWM1 is multiplexed with P1.3. IOC3.2 must be set to enable the PWM1 output function.

The PWM1_CONTROL register, in conjunction with IOC2.2, determines how long the PWM1 output is held high during the pulse, effectively controlling the duty cycle. The value written to PWM1_CONTROL register can be from 0 to 255 state times (0% to 99.6% duty cycle). Please refer to the PWM0_CONTROL register description for additional information.

PWM1_CONTROL



A0064-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	STATE_TIMES	PWM1 High State Times	0000 0000	These bits determine the number of state times that the PWM1 output is held high during the pulse. Write a hexadecimal value (00H – FFH) to this register.

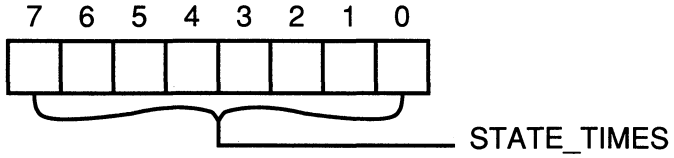
PWM2 Control Register

PWM2_CONTROL
17H
HWindow 1 (Read/Write)

PWM2 is multiplexed with P1.4. IOC3.3 must be set to enable the PWM2 output function.

The PWM2_CONTROL register, in conjunction with IOC2.2, determines how long the PWM2 output is held high during the pulse, effectively controlling the duty cycle. The value written to PWM2_CONTROL register can be from 0 to 255 state times (0% to 99.6% duty cycle). Please refer to the PWM0_CONTROL register description for additional information.

PWM2_CONTROL



A0064-A0

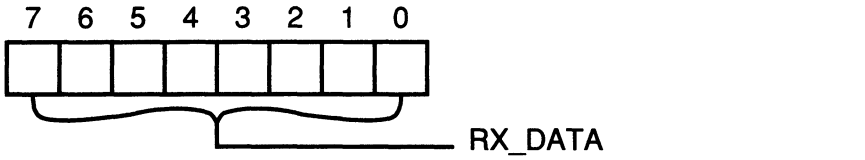
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	STATE_TIMES	PWM2 High State Times	0000 0000	These bits determine the number of state times that the PWM2 output is held high during the pulse. Write a hexadecimal value (00H – FFH) to this register.

Serial Port Receive Buffer Register

SBUF (RX)
07H
HWindow 0 (Read), HWindow 15 (Write)

The Serial Port Receive Buffer register contains data received from the serial port. The serial port receiver is double-buffered and can begin receiving a second data byte before the first byte is read. Data is held in the receive shift register until the last data bit is received, then the data byte is loaded into SBUF (RX). If data in the shift register is loaded into SBUF (RX) before the previous byte is read, the overflow error bit is set (SP_STAT.2). The data in SBUF (RX) will always be the last byte received, never a combination of the last two bytes.

SBUF (RX)



A0086-A0

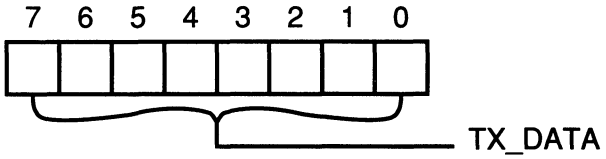
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	RX_DATA	Data Received	0000 0000	These bits contain the last byte of data received from the serial port.

Serial Port Transmit Buffer Register

SBUF (TX)
07H
HWindow 0 (Write), HWindow 15 (Read)

The Serial Port Transmit Buffer register contains data that is ready for transmission. In modes 1, 2, and 3, writing to SBUF (TX) starts a transmission. In mode 0, writing to SBUF (TX) starts a transmission only if the receiver is disabled (SP_CON.3=0).

SBUF (TX)



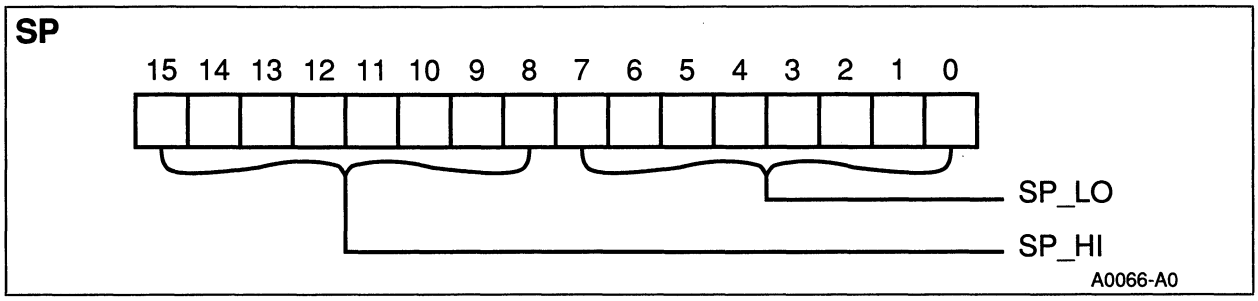
A0065-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	TX_DATA	Data to Transmit	0000 0000	These bits contain a byte of data to be transmitted by the serial port.

Stack Pointer

SP
19/18H
All HWindows (Read/Write)

The system's stack pointer may point anywhere in the 64K internal or external memory; it must be word aligned and must always be initialized before use. The stack pointer is decremented before a PUSH and incremented after a POP, so the stack pointer should be initialized to two bytes above the highest stack location. If stack operations are not being performed, locations 18H and 19H may be used as standard RAM.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	SP_LO	Stack Pointer (LO)	XXXX XXXX	The low byte of the system's stack pointer.
8–15	SP_HI	Stack Pointer (HI)	XXXX XXXX	The high byte of the system's stack pointer.

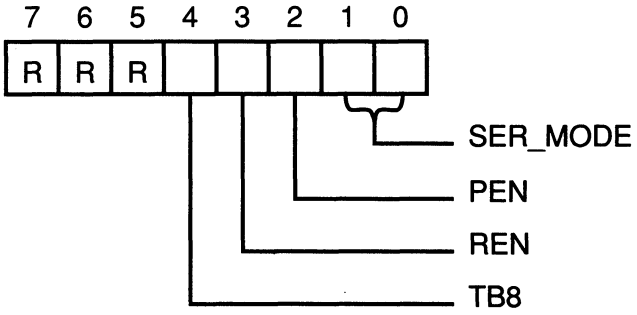
Serial Port Control Register

SP_CON
11H
HWindow 0 (Write), HWindow 15 (Read)

The Serial Port Control register selects the communications mode and enables or disables the receiver, even parity checking, and nine-bit data transmission.

TXD shares a pin with P2.0. IOC1.5 must be set to enable the TXD function. TXD serves as the transmit pin for serial port modes 1, 2, and 3 and the shift clock for mode 0. RXD shares a pin with P2.1. SP_CON.3 must be set to enable the RXD function. RXD receives serial port data in modes 1, 2, and 3 and functions as an input or an open-drain output for data in mode 0.

SP_CON



SP_CON

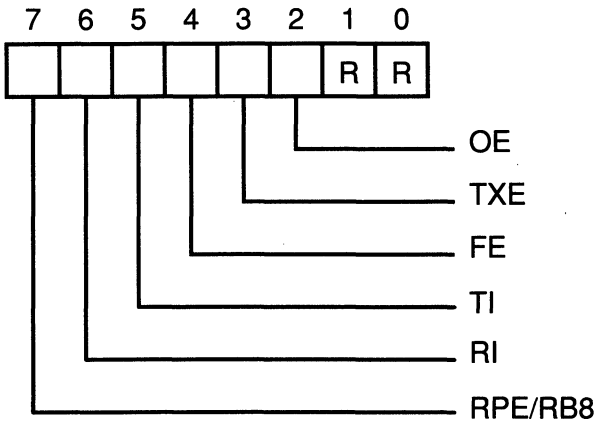
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–1	SER_MODE	Mode Selection	11	These two bits select the communications mode. **Bit 1 Bit 0** 0 0 Mode 0 0 1 Mode 1 1 0 Mode 2 1 1 Mode 3
2	PEN	Even Parity Enable	0	In modes 1 and 3, setting this bit enables the parity function. This bit must be cleared if mode 2 is used. When this bit is set, TB8 takes the even parity value on transmissions. With parity enabled, SP_STAT.7 becomes the Receive Parity Error bit.
3	REN	Receive Enable	1	Setting this bit enables the RXD function of the P2.1/RXD pin. When this bit is set, a high-to-low transition on the pin starts a reception in mode 1, 2, or 3. In mode 0, this bit must be clear for transmission to begin and must be set for reception to begin. Clearing this bit stops a reception in progress and inhibits further receptions.
4	TB8	Transmit Ninth Data Bit	0	This is the ninth data bit that will be transmitted in mode 2 or 3. This bit is cleared after each transmission, so it must be set before SBUF (TX) is written. When SPCON.2 is set, this bit takes on the even parity value.
5–7	—	—	000	Reserved; always write as zeros.

Serial Port Status Register

SP_STAT
11H
HWindow 0 (Read), HWindow 15 (Write)

The Serial Port Status register contains bits that indicate the status of the serial port.

SP_STAT



SP_STAT

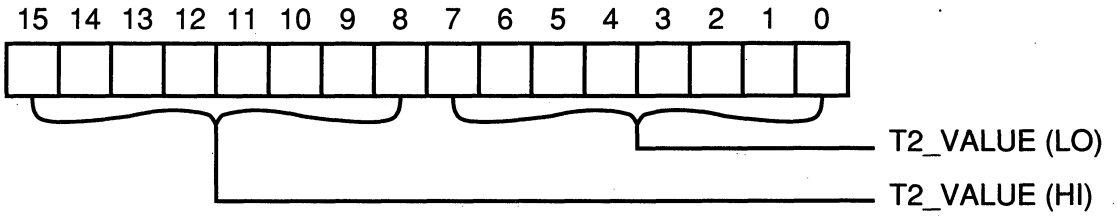
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–1	—	—	11	Reserved; always write as zero.
2	OE	Overrun Error	0	This bit is set if data in the receive shift register is loaded into SBUF (RX) before the previous bit is read. Reading SP_STAT clears this bit.
3	TXE	SBUF (TX) Empty	0	This bit is set if the transmit buffer is empty and ready to accept up to two characters. It is cleared when a byte is written to SBUF (TX).
4	FE	Framing Error	1	This bit is set if a stop bit is not found within the appropriate period of time. Reading SP_STAT clears this bit.
5	TI	Transmit Interrupt	0	This bit is set at the beginning of the stop bit transmission. Reading SP_STAT clears this bit.
6	RI	Receive Interrupt	0	This bit is set when the last data bit is sampled. Reading SP_STAT clears this bit. This bit need **not** be clear for the serial port to receive data.
7	RPE/RB8	Received Parity Error/ Received Bit 8	0	RPE is set if parity is disabled (SP_CON.2=0) and the ninth data bit received is high. RB8 is set if parity is enabled (SP_CON.2=1) and a parity error occurred. Reading SP_STAT clears this bit.

Timer 2 Capture Register

T2CAPTURE
0D/0CH
HWindow 15 (Read/Write)

A rising edge on P2.7 causes the value of Timer 2 to be captured into the T2CAPTURE register and generates a Timer 2 Capture interrupt (INT11, 2036H). INT_MASK1.3 must be set to enable the interrupt.

T2CAPTURE



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	T2_VALUE (LO)	Timer 2 Low Byte	XXXX XXXX	These bits contain the low byte of the captured value of Timer 2.
8–15	T2_VALUE (HI)	Timer 2 High Byte	XXXX XXXX	These bits contain the high byte of the captured value of Timer 2.

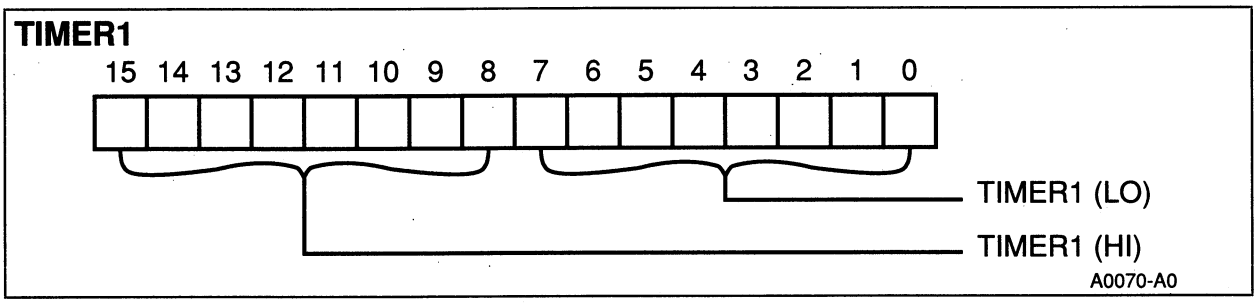
Timer 1 Register

TIMER1
0B/0AH
HWindow 0 (Read), HWindow 15 (Write)

The two bytes of the TIMER1 register contain the value of Timer 1. This register can be written, allowing Timer 1 to be initialized to a value other than zero.

Timer 1 is a 16-bit, free-running timer that is incremented every eight state times. Setting IOC1.2 causes an overflow to generate a Timer Overflow interrupt (INT00, 2000H) if INT_MASK.0 is also set, enabling the interrupt.

Use caution when writing to Timer 1 if the HSI and HSO modules are in use. HSO time entries in the CAM depend on exact matches with Timer 1. Also, changing Timer 1 between incoming events on the HSI lines will corrupt relative references between events.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	TIMER1 (LO)	Timer 1 Value, High Byte	0000 0000	These bits constitute the low byte of the Timer 1 value.
8–15	TIMER1 (HI)	Timer 1 Value, Low Byte	0000 0000	These bits constitute the high byte of the Timer 1 value.

Timer 2 Register

TIMER2
0D/0CH
HWindow 0 (Read/Write)

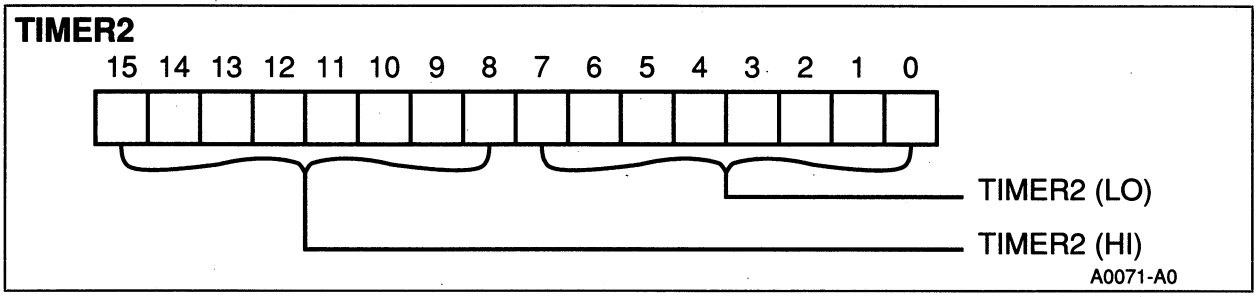
The two bytes of the TIMER2 register contain the value of Timer 2. This register can be written, allowing Timer 2 to be initialized to a value other than zero.

Timer 2 is a 16-bit counter that can be clocked either internally or externally, depending on the state of IOC3.0. If an external clock source is selected, IOC0.7 controls which of two external sources is used. Depending on the state of IOC2.0, Timer 2 counts every eight clocks (normal mode) or every clock (fast increment mode).

IOC2.1 controls the direction of Timer 2. With IOC2.1 clear, Timer 2 counts up. With IOC2.1 set, Timer 2 counts up or down, depending on the state of P2.6. Use caution when this feature is enabled and working with the HSO. If Timer 2 does not count through all 64K values, events in the CAM may never match the timer.

A Timer 2 overflow can generate either a Timer Overflow interrupt (INT00, 2000H) or a Timer 2 Overflow interrupt (INT12, 2038H). Set or clear IOC1.3, INT_MASK.0, and INT_MASK1.4 to configure Timer 2 for the desired interrupt.

This register can be cleared by hardware, software, or an HSO command, depending on the states of IOC0.3, IOC0.1, and HSO_COMMAND.0–HSO_COMMAND.3, respectively.



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	TIMER2 (LO)	Timer 2 Value, Low Byte	0000 0000	These bits constitute the low byte of the Timer 2 value.
8–15	TIMER2 (HI)	Timer 2 Value, High Byte	0000 0000	These bits constitute the high byte of the Timer 2 value.

UPROM Special Function Register

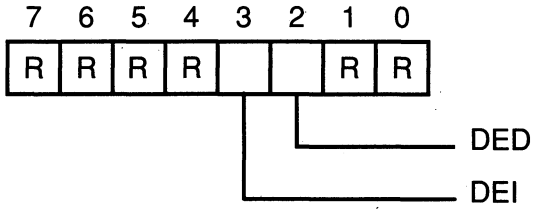
USFR
1FF6H (Read)

The UPROM (Uneraseable PROM) SFR contains two bits that disable external fetches of data and instructions. These bits can be programmed, but cannot be erased. (Refer to Chapter 14, "Programming the Non-Volatile Memory," for details.) The remaining bits are reserved.

WARNING

These bits can be programmed, but can never be erased. Programming these bits makes dynamic failure analysis impossible. For this reason, devices with programmed UPROM bits cannot be returned to Intel for failure analysis.

USFR



A0087-A0

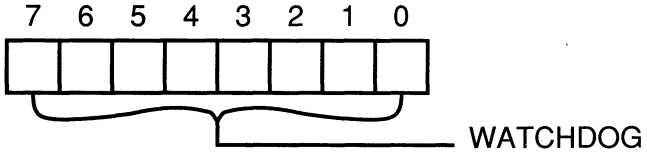
Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–1	—	—	00	Reserved; always write as zero.
2	DED	Disable External Data fetch	—	Setting this bit prevents the bus controller from executing external data reads and writes. Any attempt to access data through the bus controller initiates a reset.
3	DEI	Disable External Instruction fetch	—	Setting this bit prevents the bus controller from executing external instruction fetches. Any attempt to load an external address initiates a reset.
4–7	—	—	0000	Reserved; always write as zero.

Watchdog Timer Register

WATCHDOG
0AH
HWindow 0 (Clear/Enable), HWindow 15 (Read)

Unless it is cleared every 64K state times, the watchdog timer resets the 8XC196KC/KD. To clear the watchdog timer, send a "1EH" followed immediately by an "E1H" to location 0AH in HWindow 0. Clearing this register the first time enables the watchdog with an initial value of 0000H, which is incremented once every state time. After it is enabled, the watchdog can be disabled only by a reset. The eight most-significant bits of the watchdog value can be read in HWindow 15.

WATCHDOG



A0072-A0

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	WATCHDOG	Watchdog Timer Value	XXXX XXXX	This byte contains the 8 most-significant bits of the current value of the Watchdog timer.

Window Select Register

WSR
14H
All HWindows (Read/Write)

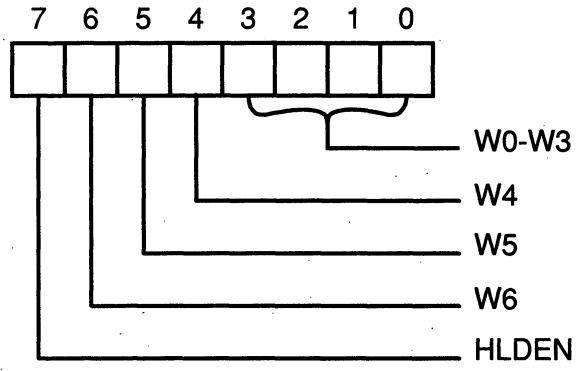
The WSR has two functions. One bit enables and disables the bus-hold protocol. The remaining bits select horizontal windows (HWindows) and vertical windows (VWindows). PUSHA saves this register on the stack, and POPA restores it.

Horizontal windows (HWindows) allow access to the Special Function Registers (SFRs) by mapping a 24-byte window into the lowest 24 bytes of the Lower Register File. HWindows 0, 1, and 15 are implemented on the 8XC196KC/KD. All other HWindows are reserved.

Vertical windows (VWindows) map sections of RAM into the upper section of the Lower Register File, in 32-, 64-, or 128-byte increments. The 8XC196KC has 512 bytes of internal RAM, which can be mapped into sixteen 32-byte VWindows, eight 64-byte VWindows, or four 128-byte VWindows. The 8XC196KD has 1024 bytes of internal RAM, which can be mapped into thirty-two 32-byte VWindows, sixteen 64-byte VWindows, or eight 128-byte VWindows.

HWindows and VWindows cannot be active at the same time. To switch between windows, write the window number into bits 0–3 and set or clear bits 4–6, as appropriate. See the window selection tables for clarification and refer to the "Memory Space Partitioning" chapter for additional information.

WSR



A0073-A0

WSR

Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–3	W0–W3	Window Select Bits 0–3	0000	Write the number of the desired HWindow or VWindow into these four bits and select the window size by setting either WSR.4, WSR.5, or WSR.6. Valid HWindows are 0, 1, and 15. Valid VWindows are 0–15 for the 8XC196KC and 0–31 for the 8XC196KD. To select VWindows 16–31, you must also set both WSR.4 and WSR.6.
4	W4	Window Select Bit 4	X	Set this bit to specify a 128-byte VWindow or, for the 8XC196KD only, to specify a 32-byte VWindow from 16–31. Otherwise, clear it. On the 8XC196KC, setting this bit selects a 128-byte VWindow. On the 8XC196KD, if WSR.6 is clear, setting this bit selects a 128-byte VWindow. If WSR.6 is set, this bit functions as the high bit of the VWindow number for 32-byte VWindows 16–31.
5	W5	Window Select Bit 5	X	Set this bit to specify a 64-byte VWindow. Otherwise, clear it.
6	W6	Window Select Bit 6	X	Set this bit to specify a 32-byte VWindow. Otherwise, clear it.
7	HLDEN	HOLD#/ HLDA# Protocol Enable	0	This bit enables or disables the bus-hold protocol. 1= enable 0= disable

HWindow Selections

Desired HWindow	Device	WSR Bits								Hex Value
		7	6	5	4	3	2	1	0	
HWindow 0	8XC196KC/KD	X	0	0	0	0	0	0	0	00H
HWindow 1	8XC196KC/KD	X	0	0	0	0	0	0	1	01H
HWindow 15	8XC196KC/KD	X	0	0	0	1	1	1	1	15H

WSR

128-Byte VWindow Selections

Desired VWindow	Address to Remap	Device	WSR Bits 7	6	5	4	3	2	1	0	Hex Value
0	0000H	8XC196KC/KD	X	0	0	1	0	0	0	0	10H
1	0080H	8XC196KC/KD	X	0	0	1	0	0	0	1	11H
2	0100H	8XC196KC/KD	X	0	0	1	0	0	1	0	12H
3	0180H	8XC196KC/KD	X	0	0	1	0	0	1	1	13H
4	0200H	8XC196KD	X	0	0	1	0	1	0	0	14H
5	0280H	8XC196KD	X	0	0	1	0	1	0	1	15H
6	0300H	8XC196KD	X	0	0	1	0	1	1	0	16H
7	0380H	8XC196KD	X	0	0	1	0	1	1	1	17H

64-Byte VWindow Selections

Desired VWindow	Address to Remap	Device	WSR Bits 7	6	5	4	3	2	1	0	Hex Value
0	0000H	8XC196KC/KD	X	0	1	0	0	0	0	0	20H
1	0040H	8XC196KC/KD	X	0	1	0	0	0	0	1	21H
2	0080H	8XC196KC/KD	X	0	1	0	0	0	1	0	22H
3	00C0H	8XC196KC/KD	X	0	1	0	0	0	1	1	23H
4	0100H	8XC196KC/KD	X	0	1	0	0	1	0	0	24H
5	0140H	8XC196KC/KD	X	0	1	0	0	1	0	1	25H
6	0180H	8XC196KC/KD	X	0	1	0	0	1	1	0	26H
7	01C0H	8XC196KC/KD	X	0	1	0	0	1	1	1	27H
8	0200H	8XC196KD	X	0	1	0	1	0	0	0	28H
9	0240H	8XC196KD	X	0	1	0	1	0	0	1	29H
10	0280H	8XC196KD	X	0	1	0	1	0	1	0	2AH
11	02C0H	8XC196KD	X	0	1	0	1	0	1	1	2BH
12	0300H	8XC196KD	X	0	1	0	1	1	0	0	2CH
13	0340H	8XC196KD	X	0	1	0	1	1	0	1	2DH
14	0380H	8XC196KD	X	0	1	0	1	1	1	0	2EH
15	03C0H	8XC196KD	X	0	1	0	1	1	1	1	2FH

WSR

32-Byte VWindow Selections

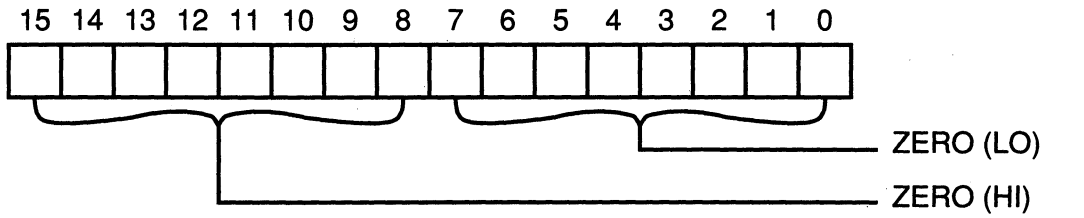
Desired VWindow	Address to Remap	Device	WSR Bits								Hex Value
			7	6	5	4	3	2	1	0	
0	0000H	8XC196KC/KD	X	1	0	0	0	0	0	0	40H
1	0020H	8XC196KC/KD	X	1	0	0	0	0	0	1	41H
2	0040H	8XC196KC/KD	X	1	0	0	0	0	1	0	42H
3	0060H	8XC196KC/KD	X	1	0	0	0	0	1	1	43H
4	0080H	8XC196KC/KD	X	1	0	0	0	1	0	0	44H
5	00A0H	8XC196KC/KD	X	1	0	0	0	1	0	1	45H
6	00C0H	8XC196KC/KD	X	1	0	0	0	1	1	0	46H
7	00E0H	8XC196KC/KD	X	1	0	0	0	1	1	1	47H
8	0100H	8XC196KC/KD	X	1	0	0	1	0	0	0	48H
9	0120H	8XC196KC/KD	X	1	0	0	1	0	0	1	49H
10	0140H	8XC196KC/KD	X	1	0	0	1	0	1	0	4AH
11	0160H	8XC196KC/KD	X	1	0	0	1	0	1	1	4BH
12	0180H	8XC196KC/KD	X	1	0	0	1	1	0	0	4CH
13	01A0H	8XC196KC/KD	X	1	0	0	1	1	0	1	4DH
14	01C0H	8XC196KC/KD	X	1	0	0	1	1	1	0	4EH
15	01E0H	8XC196KC/KD	X	1	0	0	1	1	1	1	4FH
16	0200H	8XC196KD	X	1	0	1	0	0	0	0	50H
17	0220H	8XC196KD	X	1	0	1	0	0	0	1	51H
18	0240H	8XC196KD	X	1	0	1	0	0	1	0	52H
19	0260H	8XC196KD	X	1	0	1	0	0	1	1	53H
20	0280H	8XC196KD	X	1	0	1	0	1	0	0	54H
21	02A0H	8XC196KD	X	1	0	1	0	1	0	1	55H
22	02C0H	8XC196KD	X	1	0	1	0	1	1	0	56H
23	02E0H	8XC196KD	X	1	0	1	0	1	1	1	57H
24	0300H	8XC196KD	X	1	0	1	1	0	0	0	58H
25	0320H	8XC196KD	X	1	0	1	1	0	0	1	59H
26	0340H	8XC196KD	X	1	0	1	1	0	1	0	5AH
27	0360H	8XC196KD	X	1	0	1	1	0	1	1	5BH
28	0380H	8XC196KD	X	1	0	1	1	1	0	0	5CH
29	03A0H	8XC196KD	X	1	0	1	1	1	0	1	5DH
30	03C0H	8XC196KD	X	1	0	1	1	1	1	0	5EH
31	03E0H	8XC196KD	X	1	0	1	1	1	1	1	5FH

Zero Register

ZERO_REG
01/00H
All HWindows (Read/Write)

The two-byte Zero register is always equal to zero. It is useful as a fixed source of the constant zero for comparisons and calculations. ZERO_REG can also be used as the WORD variable in a long-indexed reference. This combination of register selection and address mode enables direct addressing of any location in memory. A CMPL (compare long) instruction with ZERO_REG forces a compare with a "generated" 32-bit zero value.

ZERO_REG



Bit Number(s)	Bit Mnemonic	Bit Name	Reset State	Description
0–7	ZERO (LO)	Zero Register Low Byte	0000 0000	This is the low byte of the zero register.
8–15	ZERO (HI)	Zero Register High Byte	0000 0000	This is the high byte of the zero register.