STEREO
IMPACT

SWEA UCB to CESR
Interface Control Document (ICD)

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Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2001-Feb-22	Preliminary Draft	-
B	2001-Mar-27	- Change ripple spec to 20mV - Change SWEA Operational temp range - Add LVPS current consumption - Add SWEA HVPS requirements - Adjust housekeeping gain to correspond to HV range	
C	2001-Jun-5	- Change analog housekeeping to be bipolar - Change deflector HVPS gain - Add information on sweep waveforms	
D	2001-Nov-7	- Modify SWEA analyzer waveforms to add a pause after each step for settling time - Add operational heater	

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1. Introduction

The SWEA (Solar Wind Electron Analyzer) instrument is part of the STEREO IMPACT instrument suite. It is being built at CESR, France and the U.C.Berkeley Space Science Lab. This document shall describe the interface between the part of SWEA built in CESR and the part built at UCB.

1.1. *SWEA Description*

SWEA measures the distribution function of the solar wind core and halo electrons from ~1 to ~5000 eV with high spectral and angular resolution. SWEA consists of a top-hat electrostatic analyzer (ESA) that provides a 360° field of view in a plane combined with electrostatic deflectors to provide +/- 65° coverage in elevation out of the plane. The electrostatic optics focuses electrons from a selected energy and elevation angle onto a Micro-Channel Plate (MCP) detector. The MCP output is collected by 16 sector anodes to provide ~22° resolution in azimuth. The electronics is divided into two parts; the front-end electronics and the common SWEA/STE Interface electronics. The former includes the high voltage supplies and preamps, and is provided with the analyzer by CESR. The latter includes the logic to run the analyzer sweeps, event counters, the serial interface to the Instrument Data Processing Unit (IDPU), and the Low Voltage power converter. This part is provided by UCB to simplify the interface to the CESR section, and save resources by sharing with STE.

The MCP, Analyzer, and Deflector programmable High Voltage Power Supplies shall be provided by CESR. The Outer Hemisphere bias supply is also provided by CESR. All are programmed by voltage levels provided from DACs on the SWEA/STE interface electronics board. These supplies must have a wide dynamic range to cover the energy range accurately, and must track together well (especially the outer hemisphere and analyzer supplies) to avoid small differentials that may change with time or temperature. The anodes and preamps are closely coupled to prevent electronic noise problems.

The Interface logic is contained in an Actel FPGA. This will contain the event counters, and the logic required to generate the sweep waveforms. It contains the serial interface to the IDPU, and also the STE digital electronics. The FPGA interfaces with Digital-to-Analog Converters (DACs) to generate the programming voltages for the CESR supplies, and an ADC to measure housekeeping voltages and temperatures.

1.2. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by UCB and / or CESR indicating who is responsible for providing the data, and a unique reference number.

1.3. *Applicable Documents*

The following documents include drawings and STEREO Project policies, and are part of the Interface Requirements. In the event of a conflict between this ICD and the following

documents, this ICD takes precedence. All ICD documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

1. IMPACT_ICD_revc_31_oct 2001 (IMPACT/Spacecraft ICD on APL website)
2. ICD/IMPACTResources (Mass & Power)
3. ICD/IMPACTSetialInterface_D
4. ICD/IMPACTHarnessSpec_D
5. Phase A Report/C2.2-SWEA
6. Plans/STEREO-IMPACT-PAIP_B (Performance Assurance Implementation Plan)
7. Project/ContaminationControlPlan_7381-9006e (Cleanliness requirements)
8. Project/EnvironmentSpec7381-9003d (Environmental Requirements)
9. Project/EMC_7381-9030d (EMC requirements)

2. Mechanical Interface

2.1. *Interface Drawing*

The mechanical configuration of SWEA is shown in the IMPACT/Spacecraft ICD (Reference 1). A drawing showing the mechanical interface between the UCB and CESR parts of SWEA is TBD-CESR-002.   The CESR part of the SWEA includes all of the enclosure up to the UCB electronics enclosure at the boom end of SWEA. The UCB electronics and interface and enable connectors (SWEA-J1, SWEA-J2, and SWEA-J3; see reference 4) mount to this UCB enclosure. The UCB enclosure completes the close-out of the SWEA enclosure.

2.2. *Mass Properties*

Reference 2 includes the SWEA mass allocations. These are current best estimates, without margin. Margin is currently held by STEREO Project. The part of SWEA provided by CESR has a separate mass and power allocation as shown.

3. Thermal Interface

3.1. *Thermal Design*

The SWEA shall be largely thermally isolated from the spacecraft, and as isolated as possible from the boom. SWEA shall be designed to operate at a reasonable temperature with a minimal operational heater in addition to the normal operating power dissipation indicated in reference 2.   The operational heater shall be located near the MCP, and shall be controlled by software in the IDPU using the temperature sensor. A thermostatically controlled replacement heater shall be powered when the instrument is powered off. The instrument will be in the shade during normal operations, but may be in sunlight during early maneuvers, when it will be powered off.

3.2. *Thermal Design Responsibilities*

The thermal design of SWEA shall be the joint responsibility of CESR and UCB. CESR shall be responsible for the internal thermal design, minimizing the heat transfer out of the aperture and maintaining the electronics and MCP warm. CESR shall provide sufficient information to UCB to thermally model the instrument. UCB shall merge this information with the boom thermal model, and shall use this model to provide thermal predicts for SWEA.   UCB shall also provide this model to the spacecraft thermal engineer who will perform top-level thermal analysis (but given how isolated SWEA is from the spacecraft, this is not expected to differ much from the stand-alone thermal predicts generated by UCB). UCB/APL shall design and fabricate the thermal blankets, and shall provide the thermostat, replacement heater, and spacecraft-monitored thermistor (which will be located in the UCB part of the instrument). The replacement heater thermostat set-point shall be TBD-UCB-004. An operational heater and second temperature sensor shall be mounted near the MCP mount by. This sensor and heater shall be wired to the UCB-provided Interface circuit. UCB shall provide the thermistor to CESR.

3.3. *SWEA Temperature Requirements*

The Non-Op temperature limits apply when the instrument power is off. The instrument will not be in calibration unless in the Operational Limits.   The "Analyzer" section includes the more exposed parts of the instrument, which may be thermally isolated from the rest.

Table 3.3-1 Thermal Limits

	Temperatures, °C		
Range	Electronics	MCP	Analyzer
Non-Op Limits	-30 - +50	-30 - +50	-30 - +50
Operational Limits	-25 - +30	-25 - +30	-25 - +30

4. Electrical Interface

The UCB-provided SWEA/STE Interface electronics will be the single-point electrical interface between SWEA and the IDPU/Boom/Spacecraft.

4.1. *Low Voltage Power*

The UCB-provided SWEA/STE Low Voltage Power Supply (LVPS) shall provide power to the CESR-provided front-end electronics and High Voltage Power Supplies. The voltages to be provided and nominal currents are shown in table 4.1-1.

Table 4.1-1 CESR LVPS Requirements (TBR-CESR-006)

Voltage	Nominal Current	Max Current
+5	21mA	32mA
+12	5mA	8mA
-12	3mA	6mA
+28	13mA	

Max Current is the maximum expected current required over the operating conditions, including such things as high count rates and high voltage sweeping peaks. It does not include in-rush due to charging by-pass capacitors.

These supplies shall be regulated to +/-5% (including some variation in voltage with load, since the regulation feedback is common to all secondaries). High frequency (supply-generated) ripple on the secondaries shall be less than 20mV peak to peak at Max Current.

The +/-12V and +28V supplies are all considered "analog" supplies and have a common return to the LVPS. The +5V supply (for the preamps) is digital and has a separate return. These returns may be connected in the preamp/HVPS, but should be connected with a jumper; during ETU testing we will determine the best location(s) to connect these grounds to minimize noise in both SWEA and STE.

4.2. *SWEA Cover Actuator Power*

SWEA has a 1-time opening cover (manually reclosable), opened by providing power to an actuator. The Actuator Power shall be based on the spacecraft primary 28V supply followed by a FET switch and series current-limiting resistor in the UCB-provided interface circuitry. The supply voltage will range from 22-35V, and shall have a separate return that shall be isolated from other grounds. The circuit shall take a maximum of 750mA for a maximum of 100ms (TBR-CESR-008). The actuator shall be designed to open-circuit when the cover opens to avoid over-heating the actuator. A cover status signal shall also be incorporated, which shall be pulled-up and monitored in the interface circuitry (TBR-CESR-009; The TiNi P5-403-10 actuator can be purchased with this option).

4.3. *Enable Plug*

SWEA-J3 will mate with a green-tag enable connector. This enable connector will enable high voltage and the cover actuator. It will be part of the UCB-provided hardware (mounted with the other connectors to the SWEA end-plate).

The 28V secondary supply shall be routed via the enable plug. When the enable plug is removed, 28V will not be supplied to the HV supplies, preventing accidental application of HV. The HV supplies shall generate no significant output when 28V is not present, but should not otherwise be damaged by its absence. Separate enable bridges will be provided for the MCP 28V and for the HV supply for the analyzer and deflectors. This means that there will be two 28V signals provided to the CESR hardware: MCPHV28V and NRHV28V.

The Actuator circuit shall also run through the enable connector. This will prevent actuation when the enable plug is absent. It will also allow testing of the actuation circuit by monitoring the actuator voltage at the enable plug.

4.4. *Preamp Pulses*

The Outputs of the 16 A111F preamps shall be provided to the UCB interface circuit where they will be counted and then shipped to the IMPACT IDPU. These pulses are 0 to about +5V positive-going pulses lasting about 400ns. The signals are labeled OUTPUT1 through OUTPUT16. These correspond to the 16 anodes, numbered counter-clockwise when looking down on the top of the analyzer, starting with Anode 1 looking in direction TBD-CESR-010.

4.5. *Test Pulser*

The SWEA Interface shall provide a test pulser input to the CESR preamp electronics. This shall be a logic level signal (0-5V) with a programmable frequency up to 1MHz, and a square waveform. During normal operation, this signal shall be off (0V).

4.6. *High Voltage Enable*

The SWEA Interface shall provide signals that enable the MCP and NR supplies (MCPHVEBL and NRHVEBL). These signals shall be zero to turn the supply off, +5V (1mA max) to turn the supply On.

4.7. *Control Voltages*

The Interface Electronics shall provide analog voltages to control the programmable power supplies for the analyzer in the CESR electronics. These voltages will be generated by DACs, using a common +5.0V (+/-6mV) reference supply (AD584). CMD_ANAL shall be generated using a 16-bit DAC. CMD_DEFL1 and CMD_DEFL2 will be generated using 8 (or more)-bit multiplying DACs based on the CMD_ANAL value. CMD_MCP and CMD_VO will be generated using 8-bit DACs. Note that CMD_VO, CMD_DEFL1, and CMD_DEFL2 will require extra inversion amplifiers in the interface circuitry to generate the required polarity to the CESR HVPS.

For the analyzer and deflector supplies (ANAL, DEFL1, DEFL2), the output voltage should be equal to the HV supply gain times the control voltage, plus VO. The accuracy requirement is based on the difference between the HV output and VO.

Table 4.7-1 HV Controls

Control	Range	HV Gain	Max HV	HV Accuracy /Stability	Comments
CMD_ANAL	0 - -5.0V	-150	750	8mV or 1%	
CMD_DEFL1	0 - -2.0V	-750	1500	40mV or 1%	
CMD_DEFL2	0 - -2.0V	-750	1500	40mV or 1%	
CMD_VO	0 - +5.0V	-5	-25V	10mV	
CMD_MCP	0 - -5.0V	-700	+3500V	10V	Gain/Max TBR-CESR-012

- Assumes maximum energy is 5keV, but maximum energy at which 65 degree deflection is possible is 2keV.
- Accuracy/Stability is at the output of the HVPS. It represents the thermal stability and repeatability. Resolution from the DACs may be worse. The 1% number refers

to V-VO, and allows larger uncertainties at the high end of the output. The error
number includes any error in adding in VO.

4.8. *Sweep Waveforms*

CMD_ANAL, CMD_DEFL1, and CMD_DEFL2 shall sweep with a repetitive pattern
with an over-all 2 second period. The nominal waveform shall be as follows, but shall be
programmable. The supply settling times shall be at least sufficient to meet the
requirements of this sweep waveform.

The analyzer sweep shall cover 48 steps in 2 seconds. The time between steps shall be
40.6ms, except for the first step (between the minimum and maximum values), which
shall be 51.2ms + 40.6ms (51.2ms for the analyzer voltage to settle, plus a normal 40.6ms
deflector sweep at the first analyzer step). The sweep shall be approximately logarithmic,
sweeping from maximum to minimum value covering a dynamic range of 5000, so the
steps are about 19.4%. The output voltage should settle to within 5% of its final value in
the first 5ms after the change in the control voltage. The first step where it jumps back
from minimum back to maximum should settle to within 5% in 50ms.

The deflectors shall ramp alternately from zero to max and back to zero linearly (see
figure 4.8-1). While one supply is ramping up and down the other stays at zero. The
deflector supplies shall pause for 5.8ms while the analyzer supply settles at the start of
each step. One half cycle of both deflectors (covering the full deflector range one time,
and including the pause) shall take 28 steps of 1.45ms each. The 28 step cycle occurs
during a single step of the analyzer supply. The deflector supply shall settle to within 5%
of its final value in the first 0.5ms after a change in the control voltage. The maximum
value of the deflector voltage shall be proportional to the analyzer voltage. At the high
end of the analyzer sweep, the deflector voltage control shall be modified not to exceed
the maximum capability of the deflector high voltage supply.

The counters shall accumulate for 5.8ms intervals. The 5.8ms interval while the analyzer
voltage settles and the deflector voltages pause shall be discarded, as well as the 51.2ms
while the analyzer voltage returns to the first step. The remaining 6 5.8ms intervals shall
per analyzer step divides the deflection angle range into six 21 degree intervals.
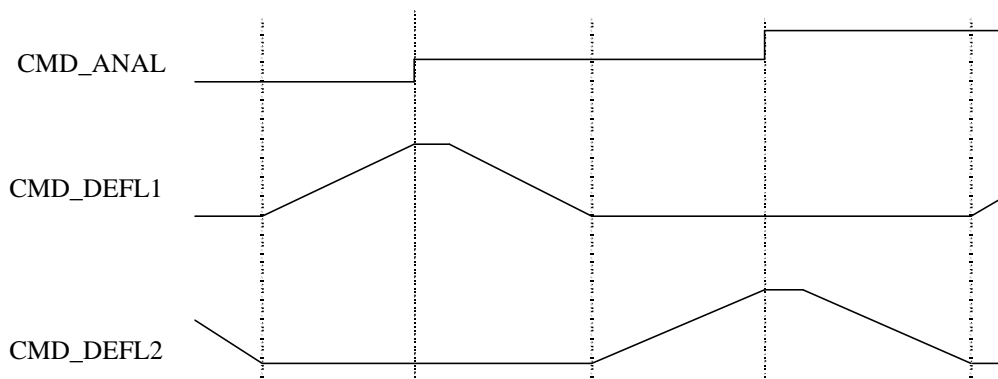

Figure 4.8-1 Sweep Waveforms

4.9. *Analog Housekeeping*

The high voltage power supplies shall provide an analog monitor proportional to their output voltages. These analog voltages shall be digitized by the SWEA Interface electronics and used for Instrument Health monitoring. The gain of the flight unit shall be calibrated by CESR, and the gain shall not drift by more than 1% over the operating temperature range. The voltages shall be in the range -5V - +5V.

Table 4.8-1 Housekeeping Monitors

Supply	Signal	Nominal Gain
MCP HV	HK_MCP	0.00100
NR HV +5VNR Monitor	HK_HV	0.75
Analyzer HV	HK_ANAL	0.0050
Deflector #1 HV	HK_DEF1	0.0020
Deflector #2 HV	HK_DEF2	0.0020
Vo (Bias) voltage	HV_VO	-0.200

4.10. *Thermistor*

A thermistor, type YSI44908 (311P18-08S7R6), shall be installed at a location near the microchannel plates mount to provide an estimate of the MCP temperature. This sensor shall be wired directly to the connector to the Interface circuit, where it shall be conditioned and digitized.

4.11. *Connector*

The signals between the CESR and UCB parts of SWEA shall be routed to a connector on the UCB-provided interface board. A CESR-provided harness will mate to this connector. Sufficient service loop shall be provided in this harness to allow it to be mated just before the UCB electronics (attached to the end-plate) are inserted into the CESR-provided SWEA housing. The connector location is TBD-UCB-012.

The connector on the Interface Board shall be a Micro-D 51 pin connector, type M83513/23-G01NP (available screened to NASA Grade 2 from Glenair)

Table 4.10-1 SWEA Interface Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal
1	OUTPUT1	19	OUTPUT2		
2	OUTPUT4	20	OUTPUT5	36	OUTPUT3
3	OUTPUT7	21	OUTPUT8	37	OUTPUT6
4	OUTPUT10	22	OUTPUT11	38	OUTPUT9
5	OUTPUT13	23	OUTPUT14	39	OUTPUT12
6	OUTPUT16	24	TEST	40	OUTPUT15
7	NRHVEBL	25	MCPHVEBL	41	DIGGND
8	OPHTR	26	OPHTRRET	42	+5V
9	COVER28V	27	COVERRET	43	Spare
10	MCPHV28V	28	NRHV28V	44	Spare
11	+12V	29	-12V	45	ANALGND
12	Spare	30	Spare	46	Spare
13	CMD_MCP	31	Spare	47	CMD_ANAL
14	CMD_DEF1	32	CMD_DEF2	48	CMD_VO
15	HK_MCP	33	HK_HV	49	HK_ANAL
16	HK_DEF1	34	HK_DEF2	50	HK_VO
17	Spare	35	Thermistor Ret	51	Spare
18	Thermistor				

4.12. *EMI/EMC/ESC Issues*

The EMC requirements for the STEREO Project are called out in Reference 9.