

# STEREO *IMPACT*

## IMPACT/PLASTIC Power Converter Requirements

LVPSRequirements\_F.doc  
Version F – 2003-Mar-05

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## Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2002-July-15	Preliminary Draft	-
B	2002-July-29	<ul style="list-style-type: none"> <li>• Small changes to the SEP supply requirements from Caltech</li> <li>• Add PLASTIC currents &amp; mechanical</li> <li>• Add SEP mechanical</li> </ul>	-
C	2002-Oct-17	<ul style="list-style-type: none"> <li>• Update SEP LVPS voltages/currents</li> <li>• Update IDPU LVPS currents</li> <li>• Add IDPU LVPS Form Factor</li> <li>• Add SWEA connector pinout</li> </ul>	-
D	2002-Dec-9	<ul style="list-style-type: none"> <li>• Add SEP connector pinouts</li> <li>• Fix SWEA Pinouts</li> <li>• Add SWEA, IDPU load capacitance</li> <li>• Add reference to HVPS requirements document</li> <li>• Remove SEPT -5.1V supply</li> <li>• Update SEP loads per the CDR values</li> <li>• Add SEP capacitive load</li> <li>• Update SEP form factor</li> </ul>	-
E	2003-Feb-25	<ul style="list-style-type: none"> <li>• PLASTIC +/-5V -&gt; +/-5.5V</li> <li>• PLASTIC loads change</li> <li>• Split PLASTIC 2.5V Load, change connector</li> <li>• Update SEP power consumption &amp; add distribution &amp; min/max figures</li> <li>• Update SEP power connector</li> </ul>	
F	2003-Mar-5	<ul style="list-style-type: none"> <li>• Update SEP loads &amp; capacitance (figures 2-1, 2-2a-c). Fig 2-1 contains has max case.</li> <li>• Update PLASTIC LVPS form factor (fig 2-4)</li> </ul>	

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## 1. Introduction

This document describes the requirements on the low voltage and high voltage power converters being built at UCB for STEREO. This includes low voltage converters for the IMPACT IDPU, SEP, and SWEA/STE, a low voltage converter for PLASTIC, and a high voltage converter for SIT. UCB will design, build, and test these supplies according to these requirements prior to providing them to the instrument teams.

### 1.1. Document Conventions

In this document, **TBD** (To Be Determined) means that no data currently exists. A value followed by **TBR** (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by a code such as UCB indicating who is responsible for providing the data, and a unique reference number.

### 1.2. Applicable Documents

The following reference documents include drawings and STEREO Project policies. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

<http://sprg.ssl.berkeley.edu/impact/dwc/>

Or on the APL STEREO web site at:

<https://sd-forum.jhuapl.edu/stereo/>

1. Project/EMC\_7881-9030\_RevA - EMC requirements
2. Project/EnvSpec7381-9003RevA - Environmental specifications
3. Specifications/IDPUDesign\_C - IDPU form factors & internal connectors
4. IMPACT\_ICD\_RevA - Spacecraft to IMPACT ICD (APL)
5. hvps\_requirements\_rev1 – SIT HVPS requirements

## 2. LVPS Requirements

The 4 low voltage power converters shall convert primary spacecraft 28V into secondary voltages as indicated in Figure 2-1.

### 2.1. Primary Characteristics

Each of the 4 supplies shall have a separate switched spacecraft service, as indicated in reference 4. The characteristics of the spacecraft 28V supply are indicated in reference 2 (including ground isolation requirements).

### 2.2. EMC

The supplies shall meet the EMC requirements called out in reference 1, in particular the conducted emissions and susceptibility requirements. Reference 4 includes a typical front end (filter) circuit for the LVPS.

### 2.3. **Secondary Characteristics**

The supplies shall provide the voltages listed in Figure 2-1. These supplies shall be regulated to +/-5% (half load to full load). High frequency (supply-generated) ripple on the secondaries shall be less than 10mV peak to peak at Max Current.

#### 2.3.1. Digital / Analog Ground

The digital supplies (highlighted in figure 2-1) shall have a separate return from the analog supplies (not highlighted). These returns will be tied together in the instrument.

#### 2.3.2. SEPT Supplies

The SEPT supplies are part of the SEP supply. These supplies shall have separate secondaries with separate isolated returns (both analog and digital). There are two such SEPT supplies (one for SEPT-E and one for SEPT-NS).

#### 2.3.3. Peak Current

Figure 2-1 lists the nominal and surge current requirements. The supply shall perform within specs for loads up to at least 50% above the nominal current indicated.

### 2.4. **Form Factor and Connector Definitions**

#### 2.4.1. IDPU LVPS

The IDPU LVPS form factor is shown in Figure 2-7. The LVPS shall have an MDM connector between the LVPS half of the tray and the other side. The mating connector shall be wired from there to the power input connector (IDPU-J1; pinout as called out in Reference 4) and the internal connector to the other boards (pinout in reference 3). Mass estimate is 400g (excluding box).

#### 2.4.2. SWEA LVPS

The SWEA LVPS form factor is shown in figure 2-2 and 2-3. The supply shall be harnessed to a connector type MM-222-021-261-41WC (M83513/04-C11N) that mates with the DAC board via a pig-tail. This connector pinout is shown in Figure 2.8.

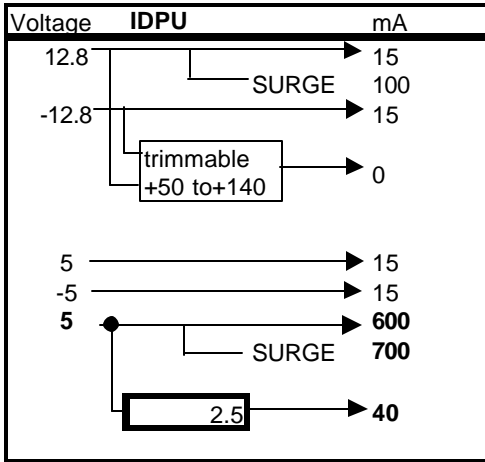
#### 2.4.3. SEP LVPS

The SEP LVPS form factor is shown in figure 2-6. Secondary connector pinouts are shown in Figure 2-9. Primary power connector pinout is defined in reference 4. Mass estimate is 480g (including box). Figure 2.1a/b shows the SEP power flow to the various subsystems. Figure 2.1c shows the min/max power consumption for SEP. At SEP turn-on loads are at the absolute minimum: in the worst case it can take up to 4 minutes to boot; nominally it takes 1 minute. Following the turn-on boot process SEP will operate in the low-power state indefinitely.

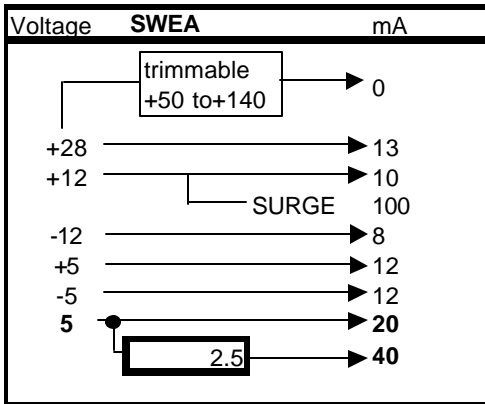
#### 2.4.4. PLASTIC LVPS

The PLASTIC LVPS form factor is shown in figures 2-4 and 2-5. Secondary voltages are available on feed-through posts as shown. Pin assignments for the output connector are shown in figure 2-10. Pinout for the input (spacecraft) connector are TBD-PLASTIC.

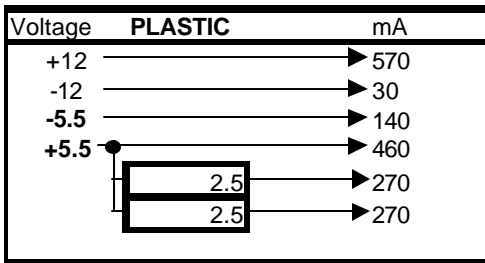
Figure 2-1 LVPS Voltage/Current Requirements



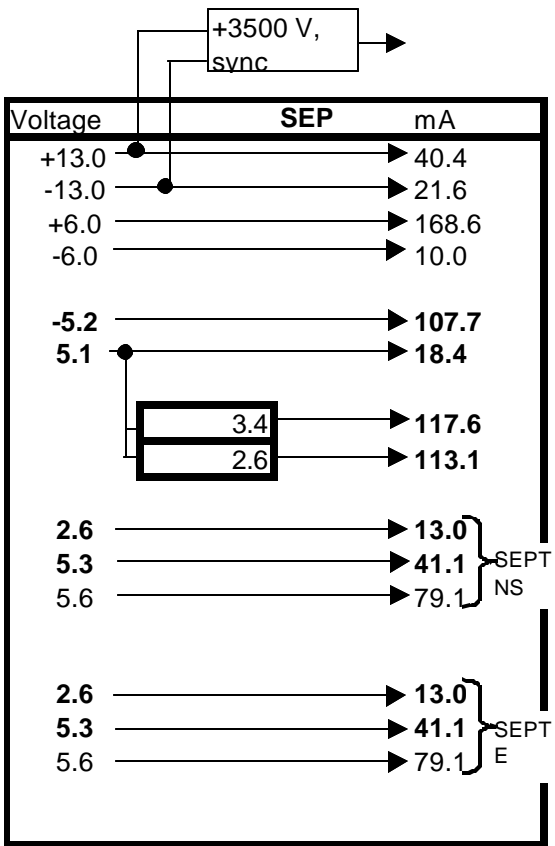
WATTS	SURGE	CAPACITANCE
0.19		6.8uF+MAG
	1.28 Watts	
0.19		6.8uF+MAG
		-
0.08		75uF
0.08		75uF
3.00		51uF+MAG
	3.50 Watts	5uF
<u>0.10</u>		31uF
3.63 Watts	8.41 Watts w/ surge	



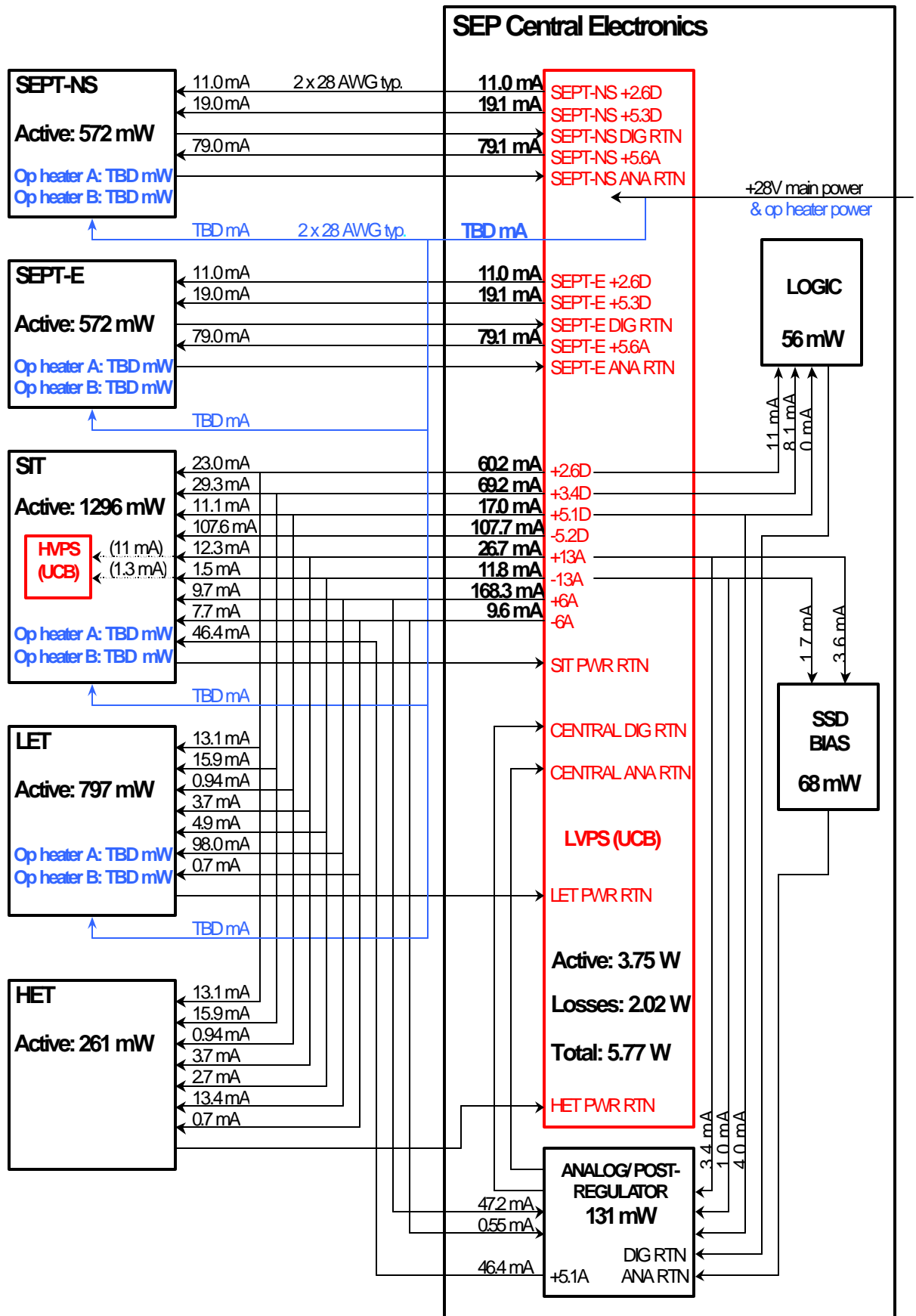
WATTS	SURGE	CAPACITANCE
		-
0.36		4.7uF
0.12		7.8uF
	1.20 Watts	
0.10		7.8uF
0.06		75uF
0.06		75uF
0.10		34uF
<u>0.10</u>		0.7uF
0.90 Watts	2.10 Watts w/ surge	



WATTS	SURGE	CAPACITANCE
6.84		25uF
0.36		20uF
0.77		20uF
2.53		30uF
0.68		?
<u>0.68</u>		25uF
11.85 Watts	(includes test port)	



<u>Watts</u>	<u>CAPACITANCE</u>
0.00	
0.53	203 uF
0.28	195 uF
1.01	224 uF
0.06	81 uF
0.56	6 uF
0.09	187 uF
0.40	281 uF
0.29	152 uF
0.03	11 uF
0.22	12 uF
0.44	50 uF
0.03	11 uF
0.22	12 uF
0.44	50 uF
<hr/>	
4.61 Watts	



SEP Power Flow (Min. = Nom.) 02/26/03  
 Figure 2-1a SEP Power Flow Diagram, Min/Nominal



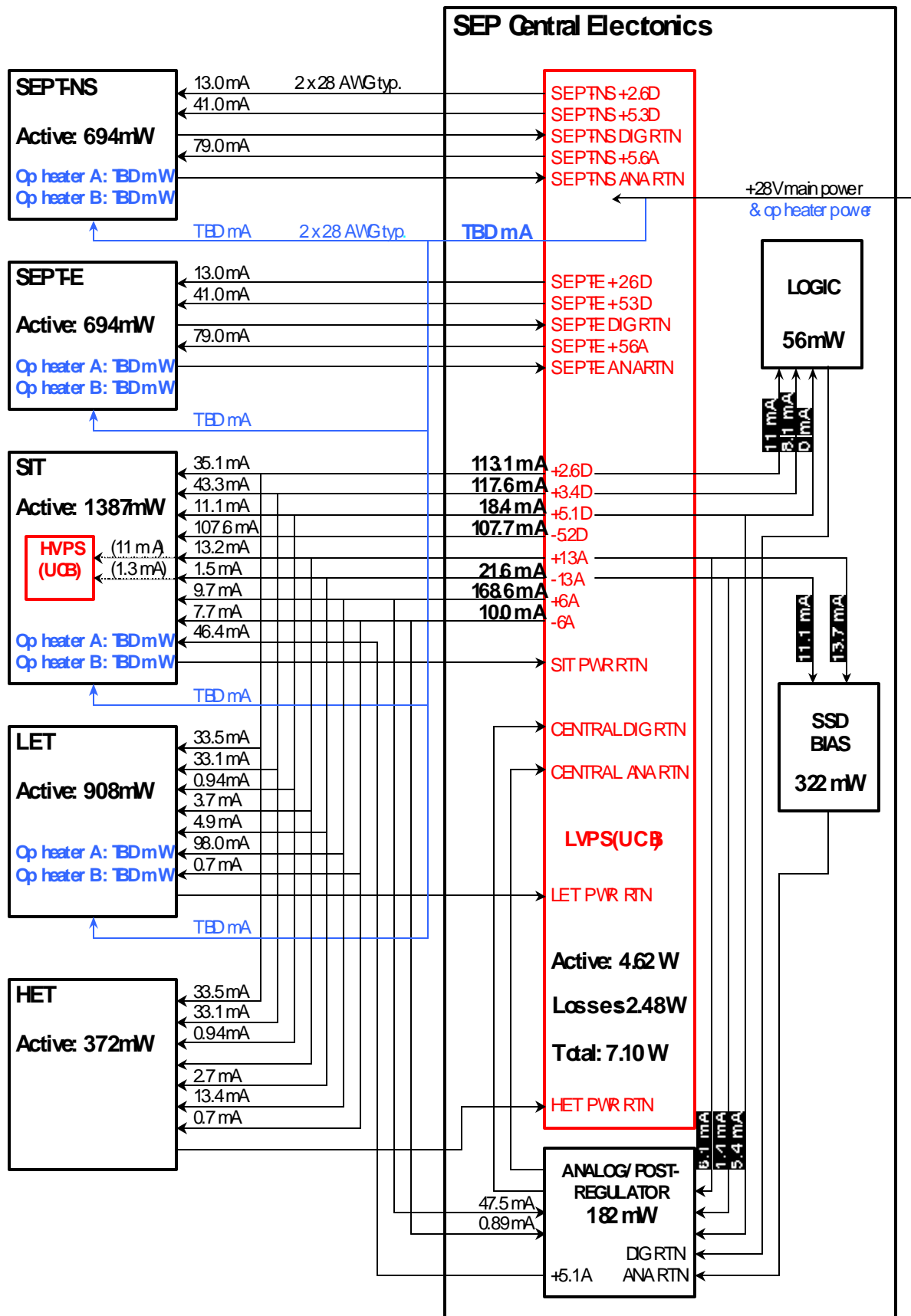


Figure 2-1b SEP Power Flow Diagram, MAX

SEP minimum (nominal) power per voltage line													2/26/2003		
Consum.	Volt.	Comment	SEPT [mA]	SEPT [mW]	SIT [mA]	SIT [mW]	LET [mA]	LET [mW]	HET [mA]	HET [mW]	Central [mA]	Central [mW]	SEP total [mA]	SEP total [mW]	LVPS output [V]
	+2.6	Digital-NS	11.0	29									11.0	29	+2.6
	+5.3	Digital-NS	19.0	101							0.085	0	19.1	101	+5.3
	+5.6	Analog-NS	79.0	442							0.085	0	79.1	443	+5.6
	+2.6	Digital-E	11.0	29									11.0	29	+2.6
	+5.3	Digital-E	19.0	101							0.085	0	19.1	101	+5.3
	+5.6	Analog-E	79.0	442							0.085	0	79.1	443	+5.6
	+2.6	Digital			23.0	60	13.1	34	13.1	34	11.0	29	60.2	157	+2.6
	+3.4	Digital			29.3	100	15.9	54	15.9	54	8.1	28	69.2	235	+3.4
	+5.1	Digital			11.1	57	0.94	5	0.94	5	4.0	20	17.0	87	+5.1
	-5.2	Digital			107.6	560					0.085	0	107.7	560	-5.2
	+13	Analog			12.3	160	3.7	48	3.7	48	7.0	91	26.7	347	+13
	-13	Analog			1.5	20	4.9	64	2.7	35	2.7	35	11.8	153	-13
	+6	Analog			9.7	58	98.0	588	13.4	80	47.2	283	168.3	1010	+6
	-6	Analog			7.7	46	0.7	4	0.7	4	0.5	3	9.6	58	-6
Regulator	+5.1	Analog			46.4	237	97.2	496	12.6	64					From +6
	<b>Instr. subtotal:</b>			<b>1143</b>		<b>1296</b>		<b>797</b>		<b>261</b>		<b>255</b>		<b>3752</b>	
		One half:	571.7												
	<b>LVPS @ 65% efficiency:</b>											<b>2020</b>	<b>2020</b>		
	<b>SEP total:</b>											<b>2275</b>	<b>5772</b>		

SEP maximum power per voltage line													2/26/2003		
Consum.	Volt.	Comment	SEPT [mA]	SEPT [mW]	SIT [mA]	SIT [mW]	LET [mA]	LET [mW]	HET [mA]	HET [mW]	Central [mA]	Central [mW]	SEP total [mA]	SEP total [mW]	LVPS output [V]
	+2.6	Digital-NS	13.0	34									13.0	34	+2.6
	+5.3	Digital-NS	41.0	217							0.085	0	41.1	218	+5.3
	+5.6	Analog-NS	79.0	442							0.085	0	79.1	443	+5.6
	+2.6	Digital-E	13.0	34									13.0	34	+2.6
	+5.3	Digital-E	41.0	217							0.085	0	41.1	218	+5.3
	+5.6	Analog-E	79.0	442							0.085	0	79.1	443	+5.6
	+2.6	Digital			35.1	91	33.5	87	33.5	87	11.0	29	113.1	294	+2.6
	+3.4	Digital			43.3	147	33.1	112	33.1	112	8.1	28	117.6	400	+3.4
	+5.1	Digital			11.1	57	0.94	5	0.94	5	5.4	28	18.4	94	+5.1
	-5.2	Digital			107.6	560					0.085	0	107.7	560	-5.2
	+13	Analog			13.2	172	3.7	48	3.7	48	19.8	257	40.4	525	+13
	-13	Analog			1.5	20	4.9	64	2.7	35	12.5	162	21.6	281	-13
	+6	Analog			9.7	58	98.0	588	13.4	80	47.5	285	168.6	1012	+6
	-6	Analog			7.7	46	0.7	4	0.7	4	0.9	5	10.0	60	-6
	+5.1	Analog			46.4	237	97.2	496	12.6	64					From +6
	<b>Instr. subtotal:</b>			<b>1387</b>		<b>1387</b>		<b>908</b>		<b>372</b>		<b>559</b>		<b>4614</b>	
		One half:	693.5												
	<b>LVPS @ 65% efficiency:</b>											<b>2484</b>	<b>2484</b>		
	<b>SEP total:</b>											<b>3044</b>	<b>7098</b>		

Figure 2-1c, SEP Min/Max Power Requirements

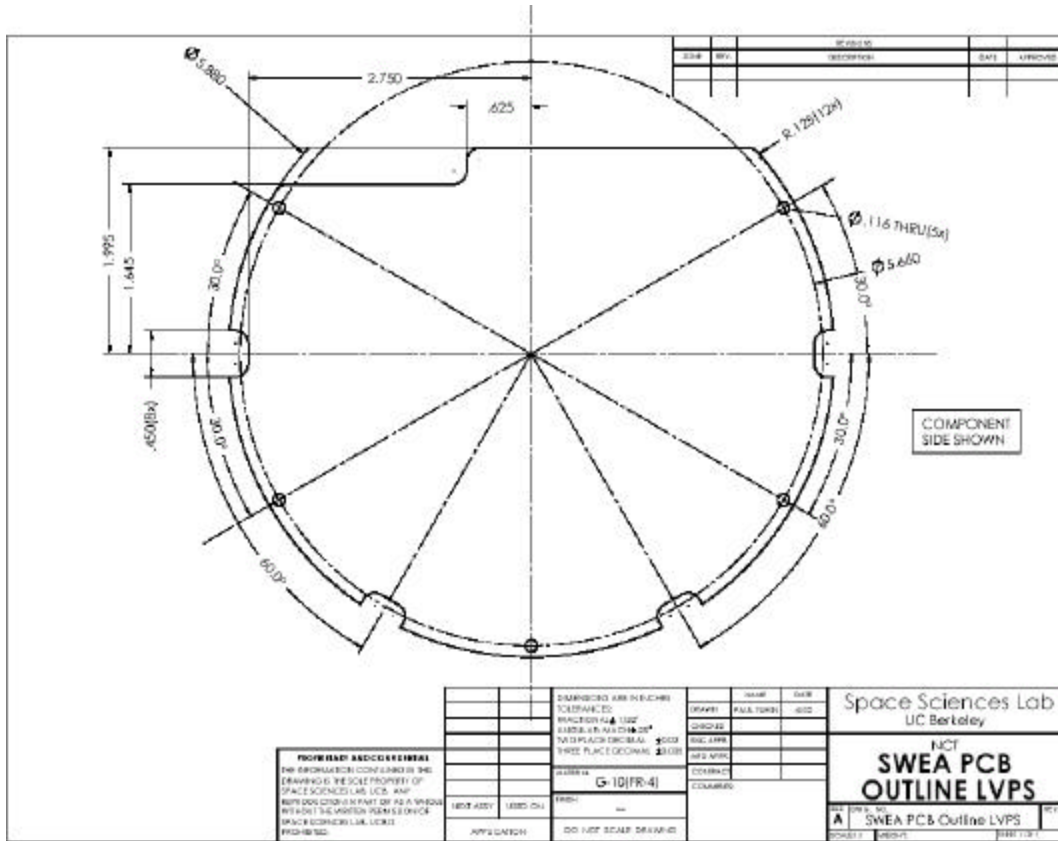


Figure 2-2 SWEA LVPS Form Factor

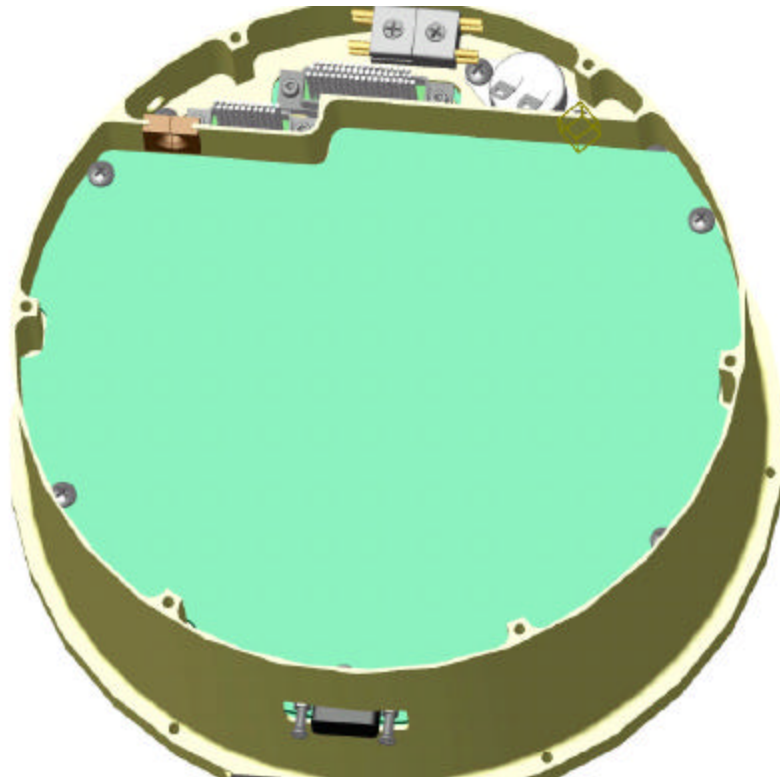


Figure 2-3 SWEA LVPS Form Factor

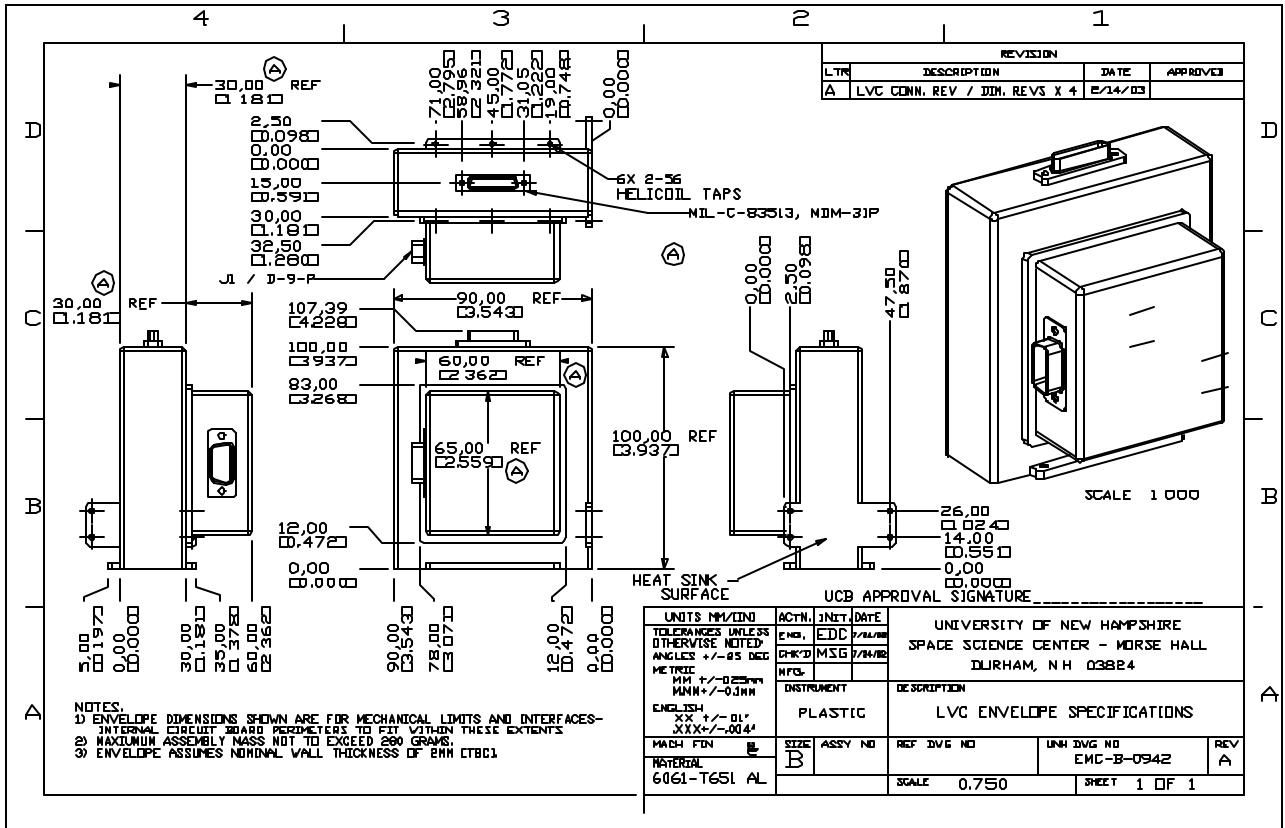


Figure 2-4, PLASTIC LVPS Form Factor

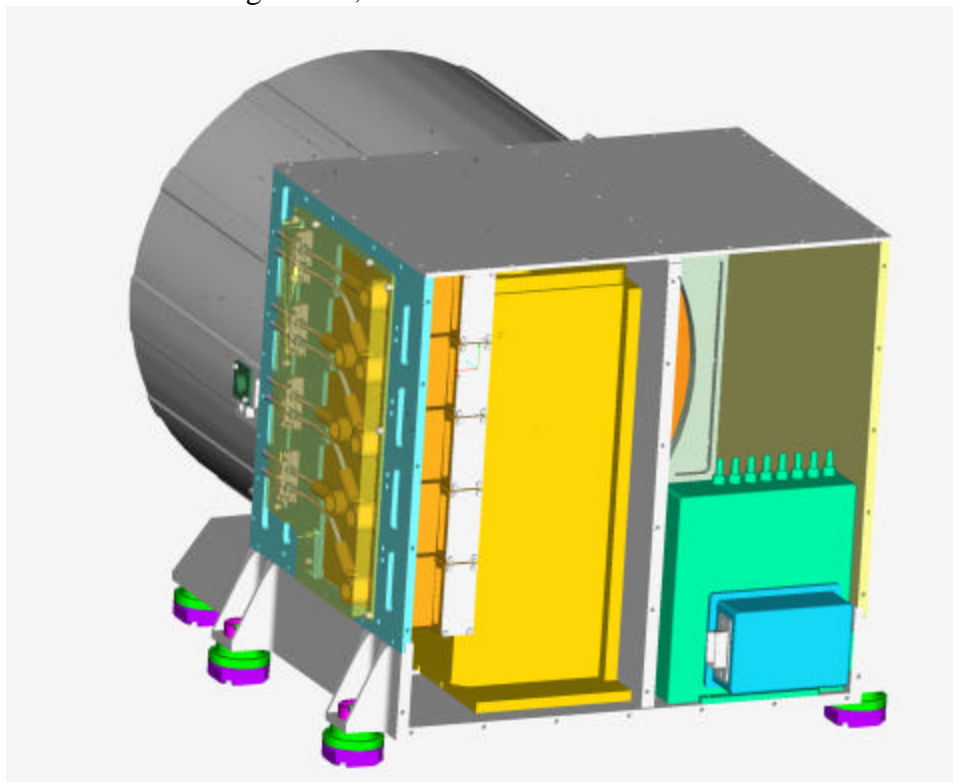


Figure 2-5, PLASTIC LVPS shown in PLASTIC

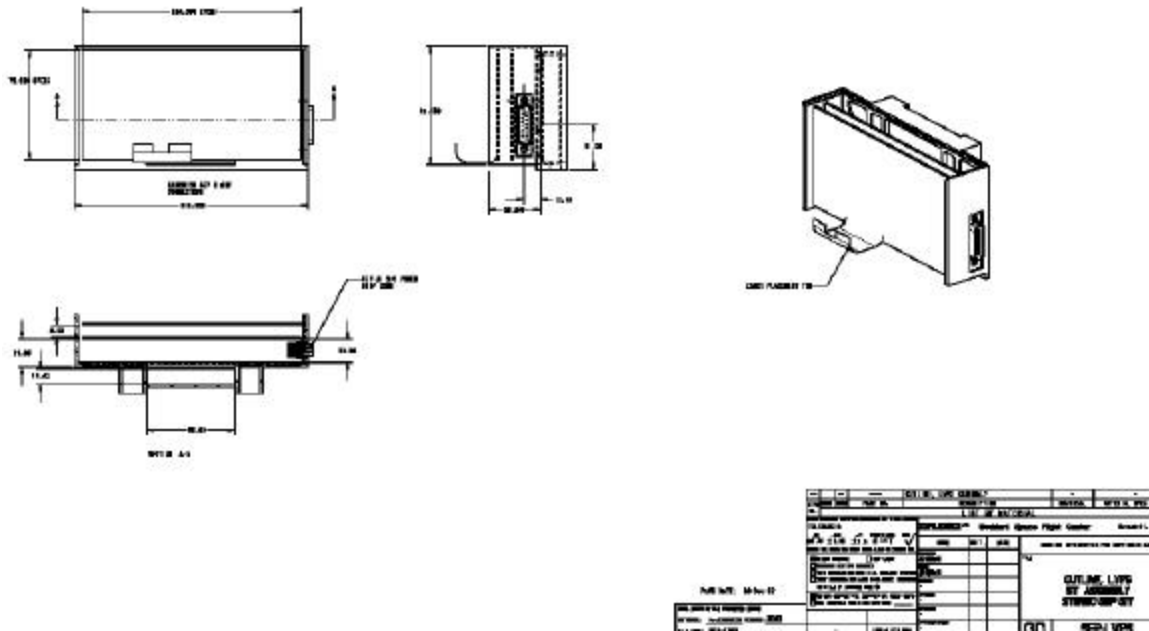


Figure 2-6 SEP LVPS form factor

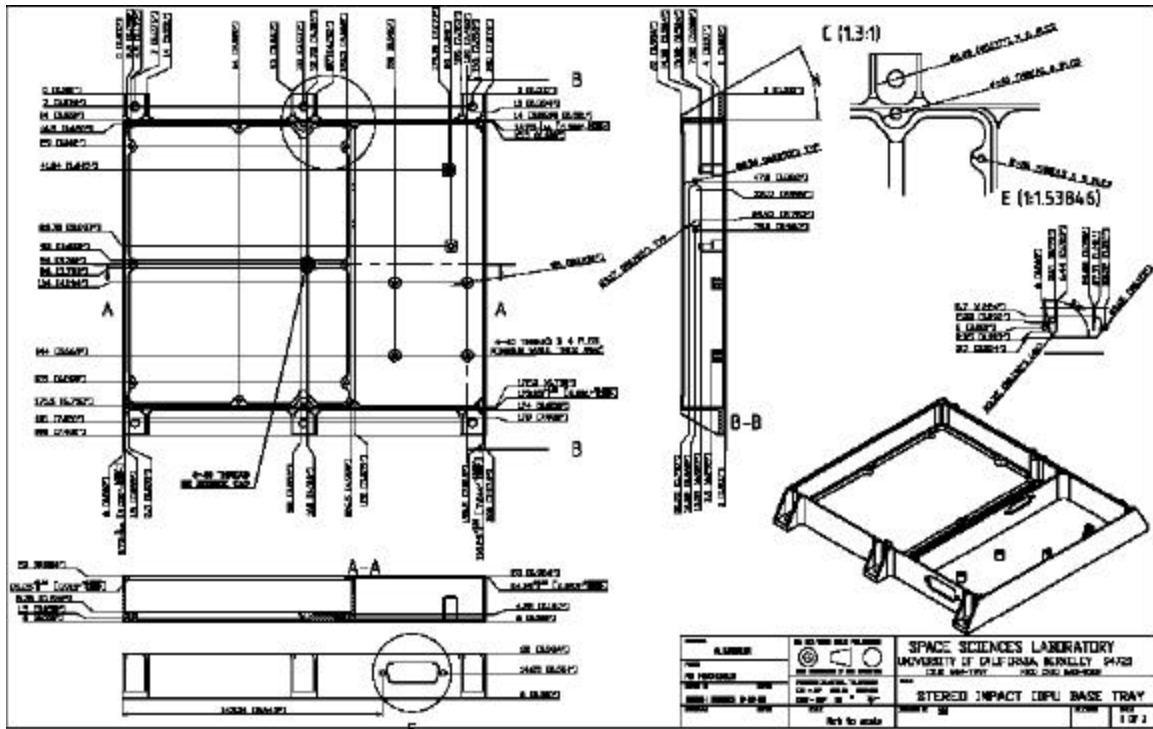


Figure 2-7 IDPU LVPS Form Factor

Airborn M83513/04-C11N (on a pig-tail attached to the LVPS)

<b>Pin</b>	<b>Signal</b>
17	STE Bias Return
16	STE Bias (140V)
7,8	Digital Ground
14	VCC_A (2.5V)
6	+5VD
13,15,9,10	Analog Ground
20	+5.1VA
18	-5.1VA
10	+12.1VA
21	-12.1VA
5	+28V (secondary)
1	+28V primary
11	+28V primary Return
12	SWEA Temp Sensor
3	SWEA Temp Sensor Return
2	+28V Heater
4	+28V Heater Return

Note: Pins 2,3,4,12 do not route to the LVPS. They go from the DAC board to a Winchester connector mounted to the chassis outside the LVPS

Figure 2-8 SWEA LVPS Connector Pinout

**SEP LVPS connectors****2/11/2003**

<b>Internal to SEP</b>		<b>Internal to SEP</b>	
<b>SEP-P19A</b>		<b>SEP-P19B</b>	
<b>LVPS output</b>		<b>LVPS output</b>	
1 SEPT-NS ANA RTN	52 HET +13A	1 LET PWR RTN	
2 SEPT-NS ANA RTN	53 HET +6A	2 LET PWR RTN	
3 SEPT-NS +5.6A	54 HET +6A	3 LET +13A	
4 SEPT-NS +5.6A	55 HET -6A	4 LET +13A	
5 Spare	56 HET -6A	5 LET +6A	
6 Spare	57 HET -13A	6 LET +6A	
7 SEPT-NS DIG RTN	58 HET -13A	7 LET -6A	
8 SEPT-NS DIG RTN	59 HET +2.6D	8 LET -6A	
9 SEPT-NS +2.6D	60 HET +2.6D	9 LET -13A	
10 SEPT-NS +2.6D	61 HET +3.4D	10 LET -13A	
11 SEPT-NS +5.3D	62 HET +3.4D	11 LET +2.6D	
12 SEPT-NS +5.3D	63 HET +5.1D	12 LET +2.6D	
13 SEPT-NS SEP STAR	64 HET +5.1D	13 LET +3.4D	
14 SEPT-NS SEP STAR	65 Spare	14 LET +3.4D	
15 SEPT-E ANA RTN		15 LET +5.1D	
16 SEPT-E ANA RTN		16 LET +5.1D	
17 SEPT-E +5.6A		17 Spare	
18 SEPT-E +5.6A		18 CENTRAL DIG RTN	
19 Spare		19 CENTRAL DIG RTN	
20 Spare		20 CENTRAL +2.6D	
21 SEPT-E DIG RTN		21 CENTRAL +2.6D	
22 SEPT-E DIG RTN		22 CENTRAL +3.4D	
23 SEPT-E +2.6D		23 CENTRAL +3.4D	
24 SEPT-E +2.6D		24 CENTRAL +5.1D	
25 SEPT-E +5.3D		25 CENTRAL +5.1D	
26 SEPT-E +5.3D		26 CENTRAL ANA RTN	
27 SEPT-E SEP STAR		27 CENTRAL ANA RTN	
28 SEPT-E SEP STAR		28 CENTRAL ANA RTN	
29 SIT PWR RTN		29 CENTRAL ANA RTN	
30 SIT PWR RTN		30 CENTRAL +13A	
31 SIT +13A		31 CENTRAL +13A	
32 SIT +13A		32 CENTRAL +6A	
33 SIT +6A		33 CENTRAL +6A	
34 SIT +6A		34 CENTRAL -6A	
35 Spare		35 CENTRAL -6A	
36 Spare		36 CENTRAL -13A	
37 SIT -6A	SEP-P19A Nanonics P/N:	37 CENTRAL -13A	
38 SIT -6A	EM STM065C6N	38 LVPS TEMP SENSOR	
39 SIT -13A	Flight 94036CD065002SE2	39 Spare	
40 SIT -13A	65-pin, TH, horizontal plug, located on flex	40 Spare	
41 SIT -5.2D		41 Spare	
42 SIT -5.2D		42 Spare	
43 SIT +2.6D	SEP-P19B Nanonics P/N:	43 Spare	
44 SIT +2.6D	EM STM051C6N	44 +28V SURV HTR RTN	
45 SIT +3.4D	Flight 94036CD051002SE2	45 +28V SURV HTR RTN	
46 SIT +3.4D	51-pin, TH, horizontal plug, located on flex	46 +28V SURV HTR	
47 SIT +5.1D		47 +28V SURV HTR	
48 SIT +5.1D		48 +28V OP HTR	
49 HET PWR RTN		49 +28V OP HTR	
50 HET PWR RTN		50 +28V OP HTR RTN	
51 HET +13A		51 +28V OP HTR RTN	

Figure 2-9 SEP LVPS Connector pinouts

***Low Voltage Convertor Pin Assignment***

<b><u>Pin #</u></b>	<b><u>Assignment</u></b>	
1	+12V	
2	+12V	
3	+12V	
4	-12V	<b><u>Part</u></b>
5	-12V	ITT Cannon.
6	-12V	M8513/ 04 - E 09 N
7	+5.5V	Receptacle
8	+5.5V	
9	+5.5V	<b><u>Wire Size</u></b>
10	-5.5V	26 Awg
11	-5.5V	
12	-5.5V	
13	+2.5V_A	
14	+2.5V_A	
15	+2.5V_A	
16	+2.5V_B	
17	AGND	
18	AGND	
19	AGND	
20	AGND	
21	AGND	
22	AGND	
23	AGND	
24	AGND	
25	AGND	
26	AGND	
27	AGND	
28	SPARE	
29	SPARE	
30	+2.5V_B	
31	+2.5V_B	

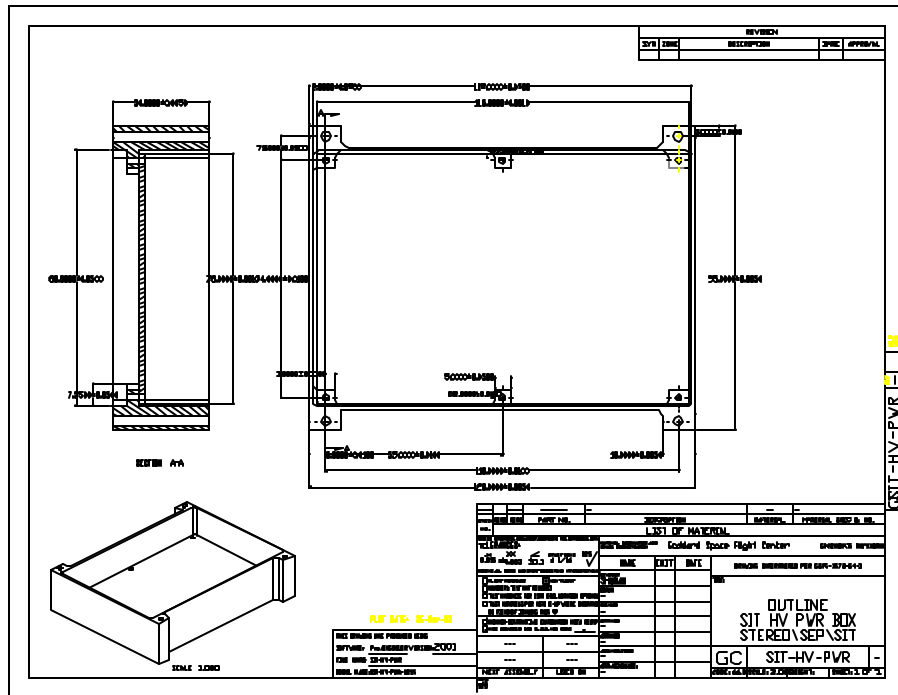
Figure 2-10 PLASTIC LVPS Converter pinout (output).

**3. SIT HVPS Requirements**

The SIT HVPS is part of the SIT instrument. It takes secondary +/-12V and generates a programmable output voltage at up to +3500V plus a number of proportional taps. This supply provides no ground isolation, and does not need to meet the conducted EMC requirements of reference 1. Detailed electrical requirements are described in reference 5.



3.1. **Form Factor**



3.2. **Connectors**

The input connector is described in reference 5. The output shall be un-terminated wires which shall be terminated in the SIT instrument. The wires must be shielded in a continuous fashion between the boxes providing no gap.