STEREO
IMPACT

IMPACT/PLASTIC Power Converter Requirements

LVPSRequirements_E.doc
Version E – 2003-Feb-25

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Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2002-July-15	Preliminary Draft	-
B	2002-July-29	• Small changes to the SEP supply requirements from Caltech • Add PLASTIC currents & mechanical • Add SEP mechanical	-
C	2002-Oct-17	• Update SEP LVPS voltages/currents • Update IDPU LVPS currents • Add IDPU LVPS Form Factor • Add SWEA connector pinout	-
D	2002-Dec-9	• Add SEP connector pinouts • Fix SWEA Pinouts • Add SWEA, IDPU load capacitance • Add reference to HVPS requirements document • Remove SEPT –5.1V supply • Update SEP loads per the CDR values • Add SEP capacitive load • Update SEP form factor	-
E	2003-Feb-25	• PLASTIC +/-5V -> +/-5.5V • PLASTIC loads change • Split PLASTIC 2.5V Load, change connector • Update SEP power consumption & add distribution & min/max figures • Update SEP power connector	

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1. Introduction

This document describes the requirements on the low voltage and high voltage power converters being built at UCB for STEREO. This includes low voltage converters for the IMPACT IDPU, SEP, and SWEA/STE, a low voltage converter for PLASTIC, and a high voltage converter for SIT. UCB will design, build, and test these supplies according to these requirements prior to providing them to the instrument teams.

1.1. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by a code such as UCB indicating who is responsible for providing the data, and a unique reference number.

1.2. *Applicable Documents*

The following reference documents include drawings and STEREO Project policies. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

Or on the APL STEREO web site at:

https://sd-forum.jhuapl.edu/stereo/

1. Project/EMC_7881-9030_RevA - EMC requirements
2. Project/EnvSpec7381-9003Rev- - Environmental specifications
3. Specifications/IDPUDesign_C - IDPU form factors & internal connectors
4. IMPACT_ICD_init_rev - Spacecraft to IMPACT ICD (APL)
5. hvps_requirements_rev1 – SIT HVPS requirements

2. LVPS Requirements

The 4 low voltage power converters shall convert primary spacecraft 28V into secondary voltages as indicated in Figure 2-1.

2.1. *Primary Characteristics*

Each of the 4 supplies shall have a separate switched spacecraft service, as indicated in reference 4. The characteristics of the spacecraft 28V supply are indicated in reference 2 (including ground isolation requirements).

2.2. *EMC*

The supplies shall meet the EMC requirements called out in reference 1, in particular the conducted emissions and susceptibility requirements. Reference 4 includes a typical front end (filter) circuit for the LVPS.

2.3. *Secondary Characteristics*

The supplies shall provide the voltages listed in Figure 2-1. These supplies shall be regulated to +/-5% (half load to full load). High frequency (supply-generated) ripple on the secondaries shall be less than 10mV peak to peak at Max Current.

2.3.1. Digital / Analog Ground

The digital supplies (highlighted in figure 2-1) shall have a separate return from the analog supplies (not highlighted). These returns will be tied together in the instrument.

2.3.2. SEPT Supplies

The SEPT supplies are part of the SEP supply. These supplies shall have separate secondaries with separate isolated returns (both analog and digital). There are two such SEPT supplies (one for SEPT-E and one for SEPT-NS).

2.3.3. Peak Current

Figure 2-1 lists the nominal and surge current requirements. The supply shall perform within specs for loads up to at least 50% above the nominal current indicated.

2.4. *Form Factor and Connector Definitions*

2.4.1. IDPU LVPS

The IDPU LVPS form factor is shown in Figure 2-7. The LVPS shall have an MDM connector between the LVPS half of the tray and the other side. The mating connector shall be wired from there to the power input connector (IDPU-J1; pinout as called out in Reference 4) and the internal connector to the other boards (pinout in reference 3). Mass estimate is 400g (excluding box).

2.4.2. SWEA LVPS

The SWEA LVPS form factor is shown in figure 2-2 and 2-3. The supply shall be harnessed to a connector type MM-222-021-261-41WC (M83513/04-C11N) that mates with the DAC board via a pig-tail. This connector pinout is shown in Figure 2.8.

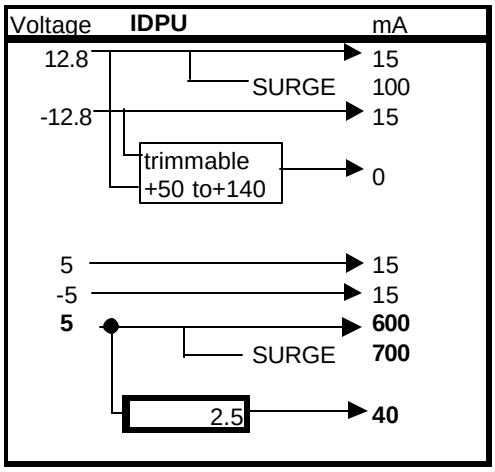
2.4.3. SEP LVPS

The SEP LVPS form factor is shown in figure 2-6. Secondary connector pinouts are shown in Figure 2-9. Primary power connector pinout is defined in reference 4. Mass estimate is 480g (including box). Figure 2.1a shows the SEP power flow to the various subsystems. Figure 2.1b shows the min/max power consumption for SEP. At SEP turn-on loads are at the absolute minimum: in the worst case it can take up to 4 minutes to boot; nominally it takes 1 minute. Following the turn-on boot process SEP will operate in the low-power state indefinitely.

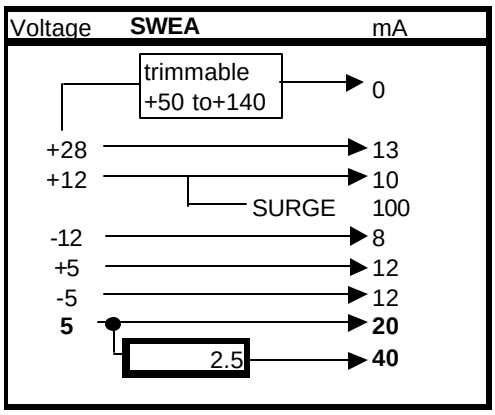
2.4.4. PLASTIC LVPS

The PLASTIC LVPS form factor is shown in figures 2-4 and 2-5. Secondary voltages are available on feed-through posts as shown. Pin assignments for the output connector are shown in figure 2-10. Pinout for the input (spacecraft) connector are TBD-PLASTIC.

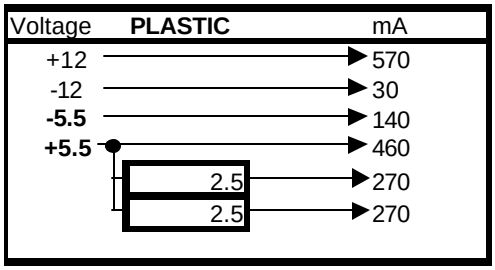
Figure 2-1 LVPS Voltage/Current Requirements



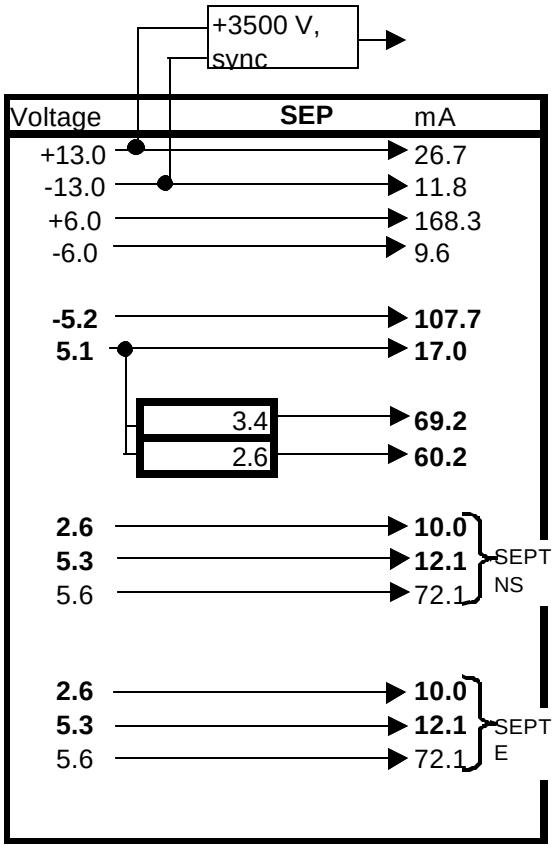
	WATTS	SURGE	CAPACITANCE
12.8	0.19		6.8uF+MAG
SURGE		1.28 Watts	
-12.8	0.19		6.8uF+MAG
trimmable +50 to+140			-
5	0.08		75uF
-5	0.08		75uF
5	3.00		51uF+MAG
SURGE		3.50 Watts	5uF
2.5	0.10		31uF
	3.63 Watts	8.41 Watts w/ surge	



	WATTS	SURGE	CAPACITANCE
trimmable +50 to+140			-
+28	0.36		4.7uF
+12	0.12		7.8uF
SURGE		1.20 Watts	
-12	0.10		7.8uF
+5	0.06		75uF
-5	0.06		75uF
5	0.10		34uF
2.5	0.10		0.7uF
	0.90 Watts	2.10 Watts w/ surge	



	WATTS	SURGE	CAPACITANCE
+12	6.84		25uF
-12	0.36		20uF
-5.5	0.77		20uF
+5.5	2.53		30uF
2.5	0.68		?
2.5	0.68		25uF
	11.85 Watts	(includes test port)	



Watts	CAPACITANCE
0.00	
0.35	30 uF
0.15	46 uF
1.01	83 uF
0.06	76 uF
0.56	6 uF
0.09	102 uF
0.24	136 uF
0.16	104 uF
0.03	11 uF
0.06	12 uF
0.40	50 uF
0.03	11 uF
0.06	12 uF
0.40	50 uF
3.59 Watts	

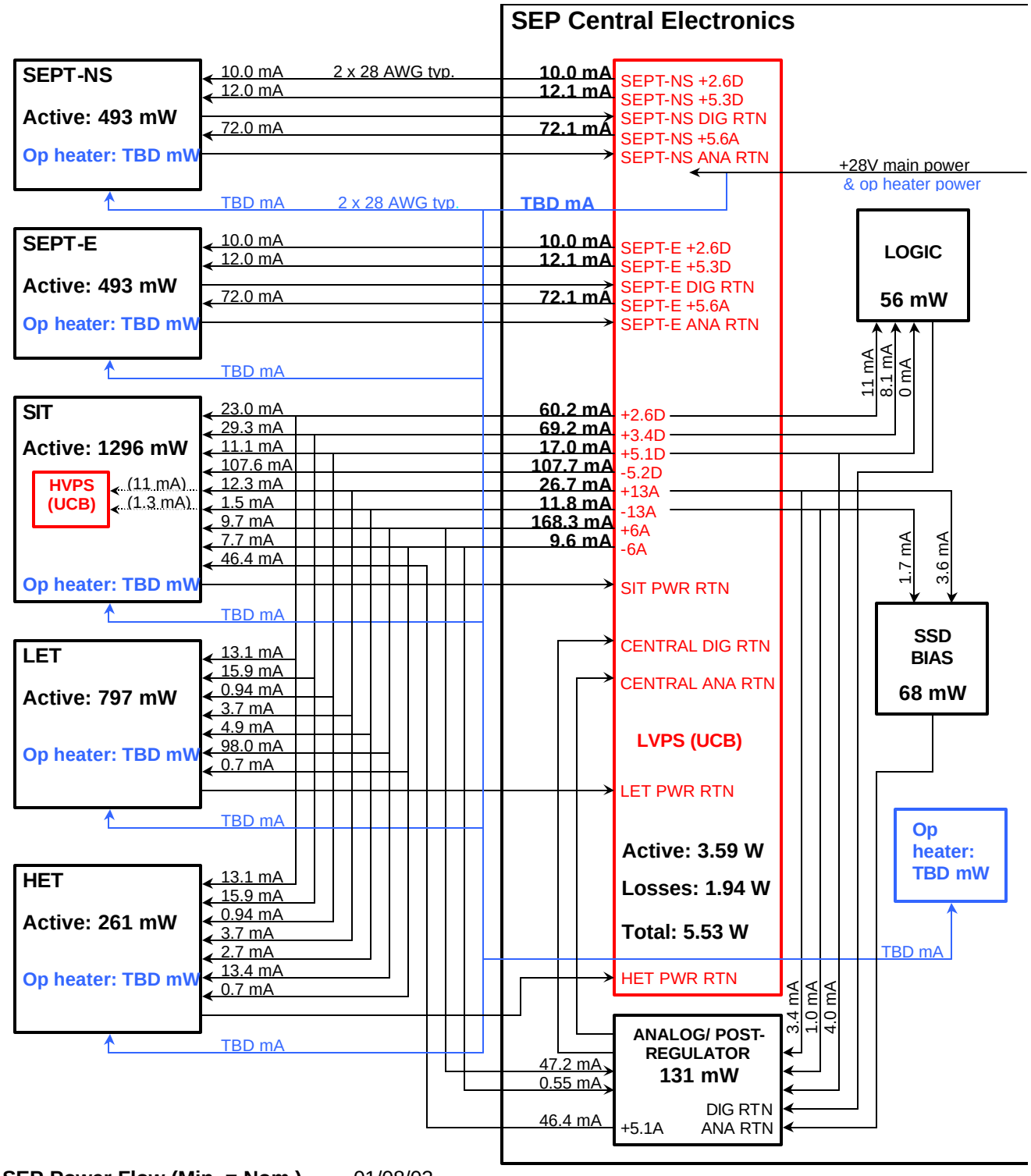


Figure 2.1a SEP power flow diagram

SEP minimum (nominal) power per voltage line

2/5/1999

Consum. Volt. [V]	Comment	SEPT [mA]	SEPT [mW]	SIT [mA]	SIT [mW]	LET [mA]	LET [mW]	HET [mA]	HET [mW]	Central [mA]	Central [mW]	SEP total [mA]	SEP total [mW]
+2.6	Digital-NS	11.0	29									11.0	29
+5.3	Digital-NS	19.0	101							0.000	0	19.0	101
+5.6	Analog-NS	79.0	442							0	0	79.0	442
+2.6	Digital-E	11.0	29									11.0	29
+5.3	Digital-E	19.0	101							0.000	0	19.0	101
+5.6	Analog-E	79.0	442							0	0	79.0	442
+2.6	Digital			23.0	60	0.0	0	0.0	0	0.0	0	23.0	60
+3.4	Digital			29.3	100	0.0	0	0.0	0	0.0	0	29.3	100
+5.1	Digital			11.1	57	0.00	0	0.00	0	0.0	0	11.1	57
-5.2	Digital			107.6	560					0.000	0	107.6	560
+13	Analog			12.3	160	0.0	0	0.0	0	0.0	0	12.3	160
-13	Analog			1.5	20	0.0	0	0.0	0	0.0	0	1.5	20
+6	Analog			9.7	58	0.0	0	0.0	0	46.4	278	56.1	337
-6	Analog			7.7	46	0.0	0	0.0	0	0.0	0	7.7	46
Regulator													
+5.1	Analog			46.4	237	0.0	0	0.0	0				
	Instr. subtotal:		1143		1296		0		0		42		2481
		One half	571.7										
LVPS @ 65% efficiency:											1336		1336
	SEP total:										1378		3817

SEP maximum power per voltage line

2/5/1999

Consum. Volt. [V]	Comment	SEPT [mA]	SEPT [mW]	SIT [mA]	SIT [mW]	LET [mA]	LET [mW]	HET [mA]	HET [mW]	Central [mA]	Central [mW]	SEP total [mA]	SEP total [mW]
+2.6	Digital-NS	13.0	34									13.0	34
+5.3	Digital-NS	41.0	217							0.000	0	41.0	217
+5.6	Analog-NS	79.0	442							0	0	79.0	442
+2.6	Digital-E	13.0	34									13.0	34
+5.3	Digital-E	41.0	217							0.000	0	41.0	217
+5.6	Analog-E	79.0	442							0	0	79.0	442
+2.6	Digital			35.1	91	0.0	0	0.0	0	0.0	0	35.1	91
+3.4	Digital			43.3	147	0.0	0	0.0	0	0.0	0	43.3	147
+5.1	Digital			11.1	57	0.00	0	0.00	0	0.0	0	11.1	57
-5.2	Digital			107.6	560					0.000	0	107.6	560
+13	Analog			13.2	172	0.0	0	0.0	0	0.0	0	13.2	172
-13	Analog			1.5	20	0.0	0	0.0	0	0.0	0	1.5	20
+6	Analog			9.7	58	0.0	0	0.0	0	46.4	278	56.1	337
-6	Analog			7.7	46	0.0	0	0.0	0	0.0	0	7.7	46
+5.1	Analog			46.4	237	0.0	0	0.0	0				
	Instr. subtotal:		1387		1387		0		0		42		2816
			694										
LVPS @ 65% efficiency:											1516		1516
	SEP total:										1558		4332

Figure 2.2b, SEP Min/Max Power Requirements

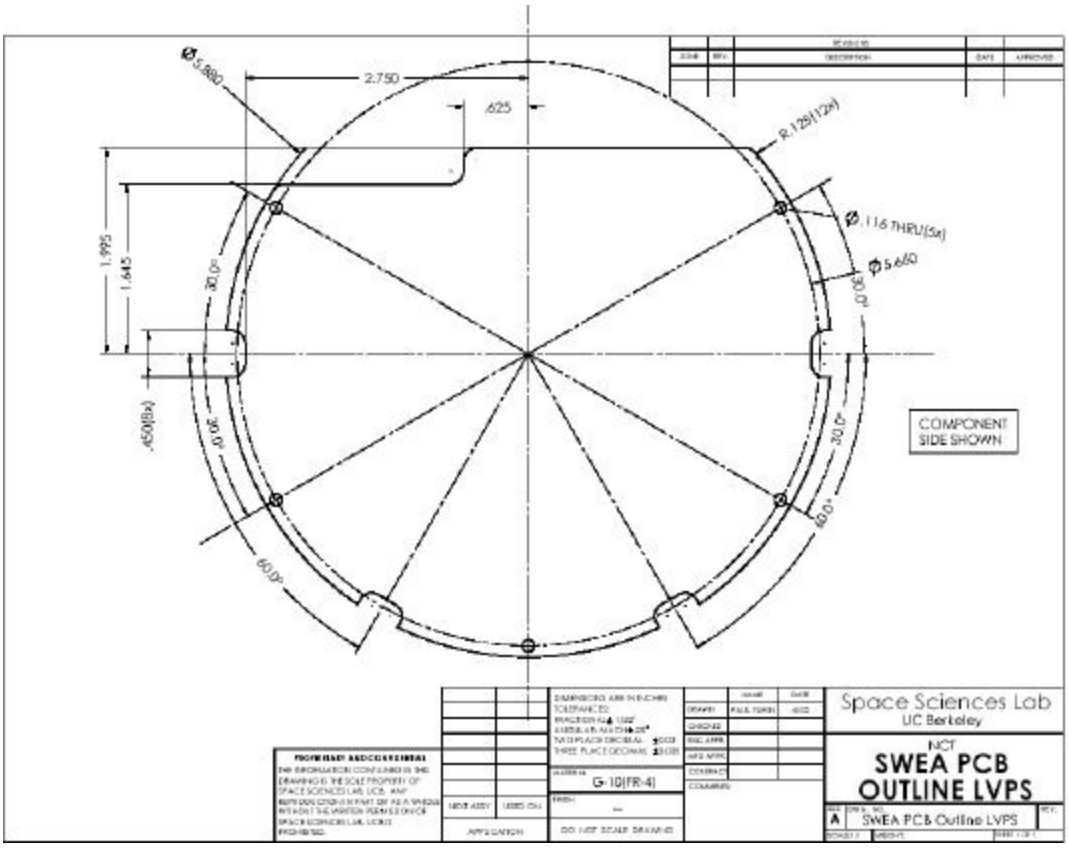


Figure 2-2 SWEA LVPS Form Factor

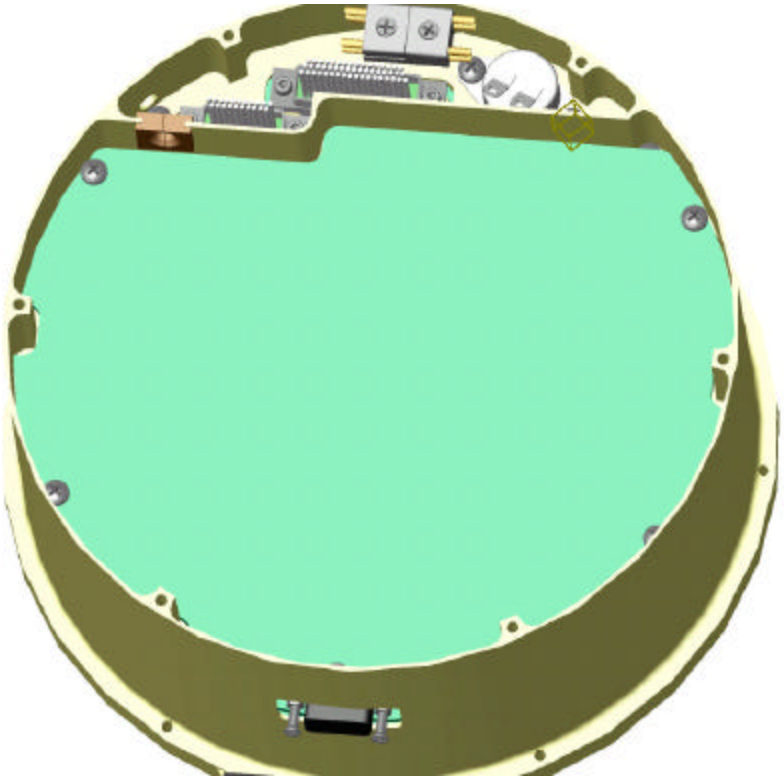


Figure 2-3 SWEA LVPS Form Factor

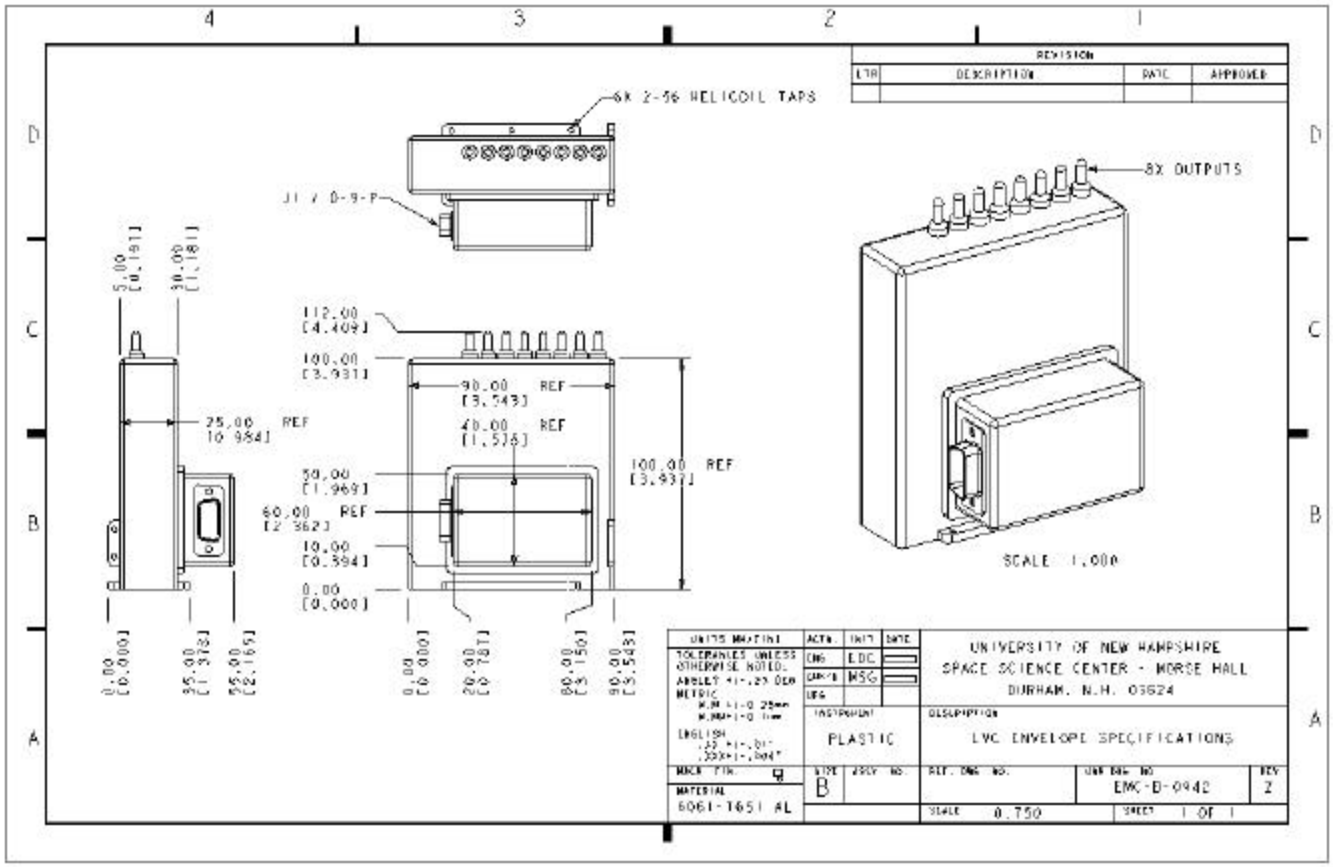


Figure 2-4, PLASTIC LVPS Form Factor

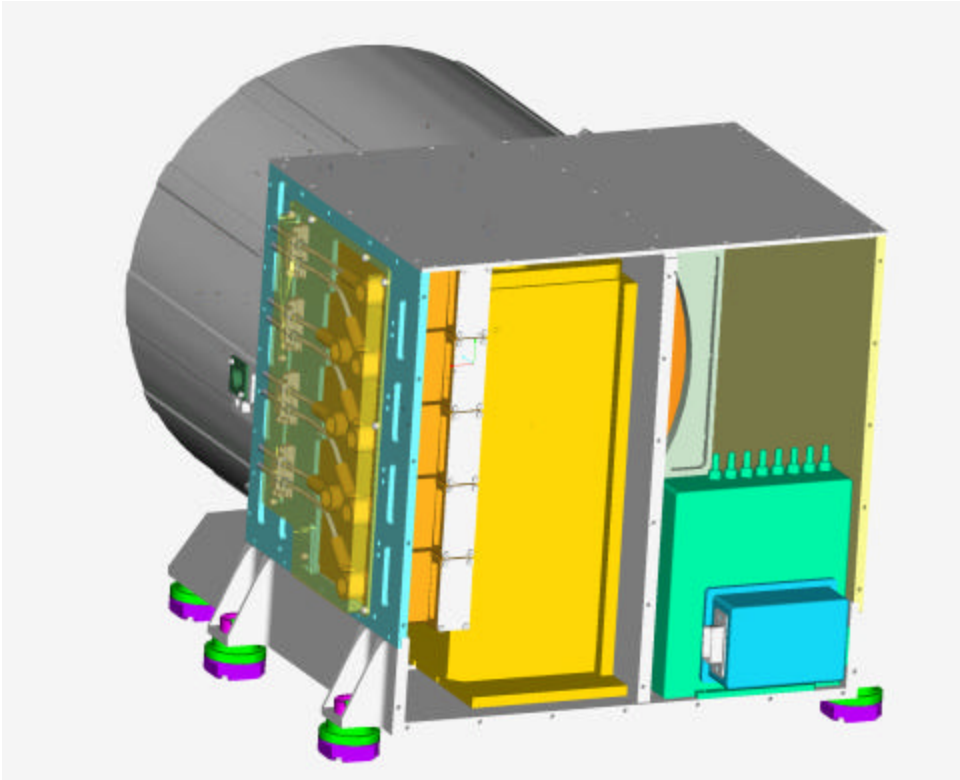


Figure 2-5, PLASTIC LVPS shown in PLASTIC

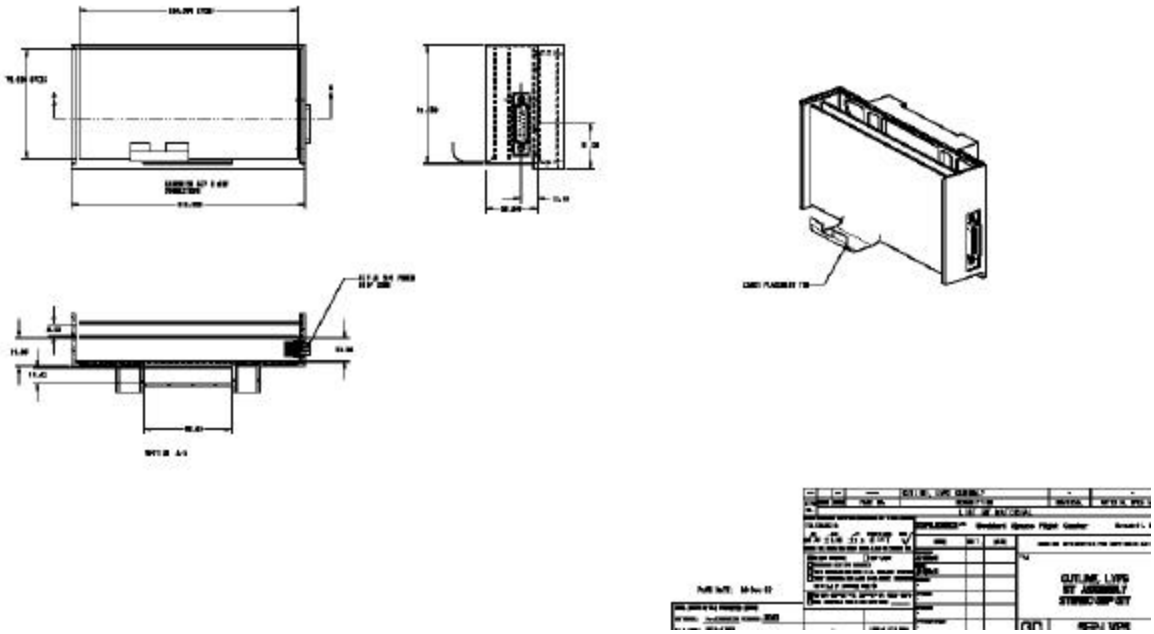


Figure 2-6 SEP LVPS form factor

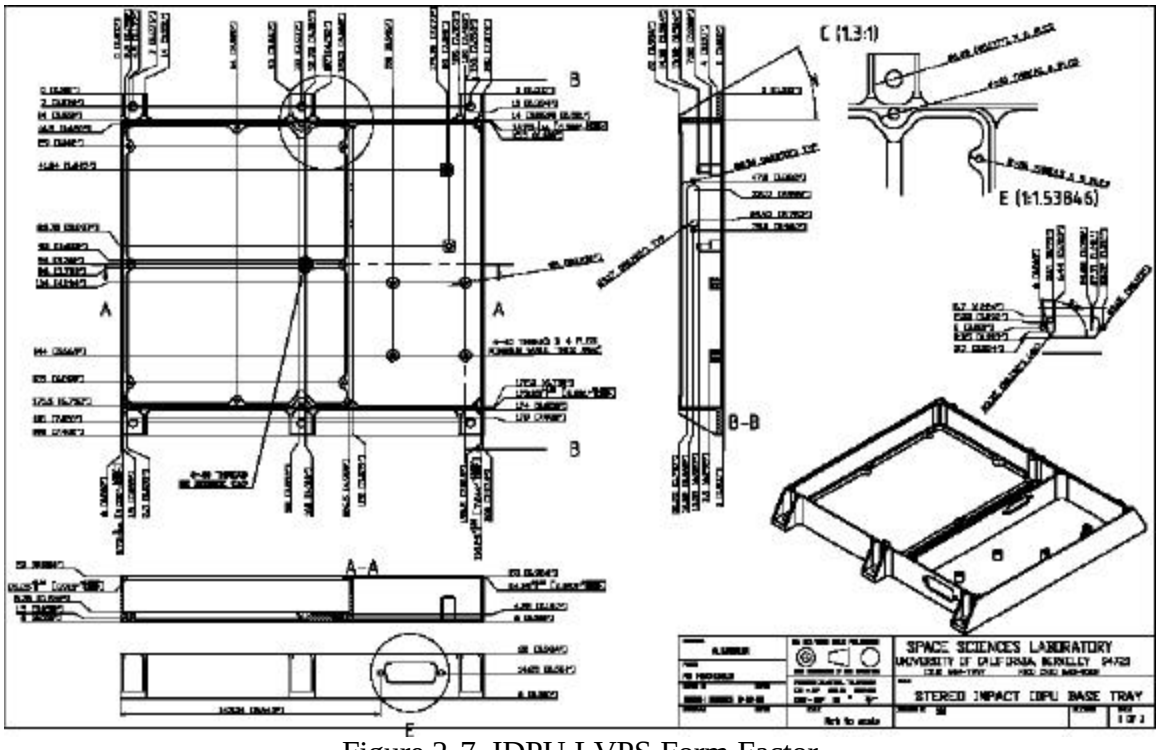


Figure 2-7 IDPU LVPS Form Factor

Airborn M83513/04-C11N (on a pig-tail attached to the LVPS)

Pin	Signal
17	STE Bias Return
16	STE Bias (140V)
7,8	Digital Ground
14	VCC_A (2.5V)
6	+5VD
13,15,9,10	Analog Ground
20	+5.1VA
18	-5.1VA
10	+12.1VA
21	-12.1VA
5	+28V (secondary)
1	+28V primary
11	+28V primary Return
12	SWEA Temp Sensor
3	SWEA Temp Sensor Return
2	+28V Heater
4	+28V Heater Return

Note: Pins 2,3,4,12 do not route to the LVPS. They go from the DAC board to a Winchester connector mounted to the chassis outside the LVPS

Figure 2-8 SWEA LVPS Connector Pinout

SEP LVPS connectors 2/11/2003

Internal to SEP
SEP-P19A
LVPS output

1	SEPT-NS ANA RTN	52	HET +13A	1	LET PWR RTN
2	SEPT-NS ANA RTN	53	HET +6A	2	LET PWR RTN
3	SEPT-NS +5.6A	54	HET +6A	3	LET +13A
4	SEPT-NS +5.6A	55	HET -6A	4	LET +13A
5	Spare	56	HET -6A	5	LET +6A
6	Spare	57	HET -13A	6	LET +6A
7	SEPT-NS DIG RTN	58	HET -13A	7	LET -6A
8	SEPT-NS DIG RTN	59	HET +2.6D	8	LET -6A
9	SEPT-NS +2.6D	60	HET +2.6D	9	LET -13A
10	SEPT-NS +2.6D	61	HET +3.4D	10	LET -13A
11	SEPT-NS +5.3D	62	HET +3.4D	11	LET +2.6D
12	SEPT-NS +5.3D	63	HET +5.1D	12	LET +2.6D
13	SEPT-NS SEP STAR	64	HET +5.1D	13	LET +3.4D
14	SEPT-NS SEP STAR	65	Spare	14	LET +3.4D
15	SEPT-E ANA RTN			15	LET +5.1D
16	SEPT-E ANA RTN			16	LET +5.1D
17	SEPT-E +5.6A		**External to SEP**	17	Spare
18	SEPT-E +5.6A		**SEP-J1**	18	CENTRAL DIG RTN
19	Spare		**S/C power & heaters**	19	CENTRAL DIG RTN
20	Spare	1	Spare	20	CENTRAL +2.6D
21	SEPT-E DIG RTN	2	+28V MAIN/OP HTR	21	CENTRAL +2.6D
22	SEPT-E DIG RTN	3	+28V MAIN/OP HTR	22	CENTRAL +3.4D
23	SEPT-E +2.6D	4	Spare	23	CENTRAL +3.4D
24	SEPT-E +2.6D	5	+28V SURV HTR	24	CENTRAL +5.1D
25	SEPT-E +5.3D	6	+28V SURV HTR	25	CENTRAL +5.1D
26	SEPT-E +5.3D	7	Spare	26	CENTRAL ANA RTN
27	SEPT-E SEP STAR	8	CHASSIS	27	CENTRAL ANA RTN
28	SEPT-E SEP STAR	9	Spare	28	CENTRAL ANA RTN
29	SIT PWR RTN	10	+28V MAIN/OP HTR RTN	29	CENTRAL ANA RTN
30	SIT PWR RTN	11	+28V MAIN/OP HTR RTN	30	CENTRAL +13A
31	SIT +13A	12	Spare	31	CENTRAL +13A
32	SIT +13A	13	+28V SURV HTR RTN	32	CENTRAL +6A
33	SIT +6A	14	+28V SURV HTR RTN	33	CENTRAL +6A
34	SIT +6A	15	Spare	34	CENTRAL -6A
35	Spare			35	CENTRAL -6A
36	Spare			36	CENTRAL -13A
37	SIT -6A	SEP-P19A	Nanonics P/N:	37	CENTRAL -13A
38	SIT -6A	EM	STM065C6N	38	LVPS TEMP SENSOR
39	SIT -13A	Flight	94036CD065002SE2	39	Spare
40	SIT -13A	65-pin, TH, horizontal plug, located on flex		40	Spare
41	SIT -5.2D			41	Spare
42	SIT -5.2D			42	Spare
43	SIT +2.6D	SEP-P19B	Nanonics P/N:	43	Spare
44	SIT +2.6D	EM	STM051C6N	44	+28V SURV HTR RTN
45	SIT +3.4D	Flight	94036CD051002SE2	45	+28V SURV HTR RTN
46	SIT +3.4D	51-pin, TH, horizontal plug, located on flex		46	+28V SURV HTR
47	SIT +5.1D			47	+28V SURV HTR
48	SIT +5.1D			48	+28V OP HTR
49	HET PWR RTN			49	+28V OP HTR
50	HET PWR RTN			50	+28V OP HTR RTN
51	HET +13A			51	+28V OP HTR RTN

Internal to SEP
SEP-P19B
LVPS output

Figure 2-9 SEP LVPS Connector pinouts

Low Voltage Convertor Pin Assignment

Pin #	**Assignment**
1	+12V
2	+12V
3	+12V
4	-12V
5	-12V
6	-12V
7	+5.5V
8	+5.5V
9	+5.5V
10	-5.5V
11	-5.5V
12	-5.5V
13	+2.5V_A
14	+2.5V_A
15	+2.5V_A
16	+2.5V_B
17	AGND
18	AGND
19	AGND
20	AGND
21	AGND
22	AGND
23	AGND
24	AGND
25	AGND
26	AGND
27	AGND
28	SPARE
29	SPARE
30	+2.5V_B
31	+2.5V_B

Part
ITT Cannon.
M8513/ 04 - E 09 N
Receptacle

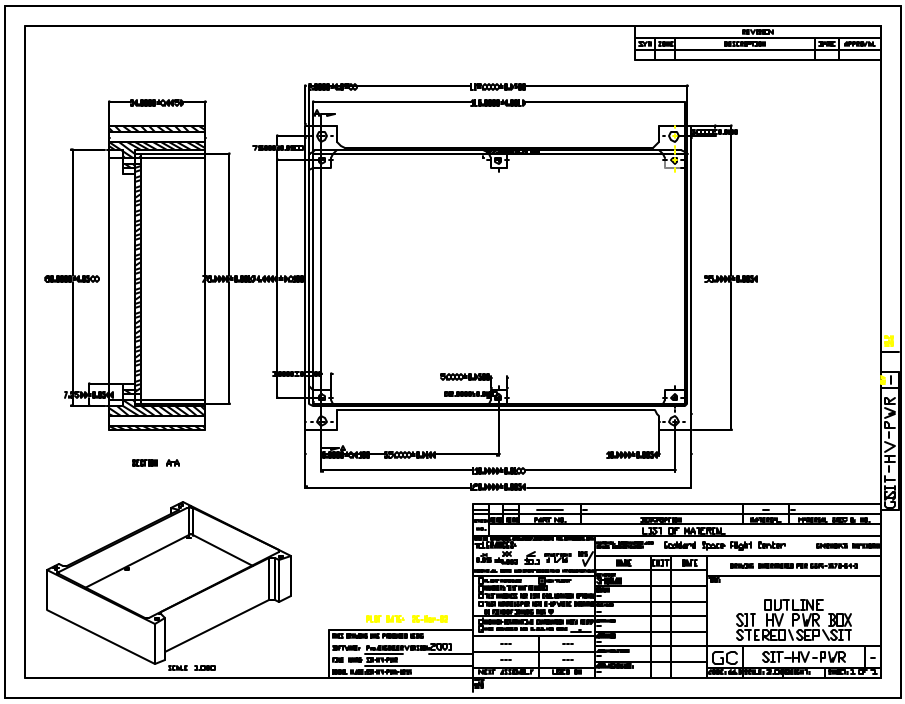
Wire Size
26 Awg

Figure 2-10 PLASTIC LVPS Converter pinout (output).

3. SIT HVPS Requirements

The SIT HVPS is part of the SIT instrument. It takes secondary +/-12V and generates a programmable output voltage at up to +3500V plus a number of proportional taps. This supply provides no ground isolation, and does not need to meet the conducted EMC requirements of reference 1. Detailed electrical requirements are described in reference 5.

3.1. *Form Factor*



3.2. *Connectors*

The input connector is described in reference 5. The output shall be un-terminated wires which shall be terminated in the SIT instrument. The wires must be shielded in a continuous fashion between the boxes providing no gap.