STEREO
IMPACT

IMPACT/PLASTIC Power Converter Requirements

LVPSRequirements_D.doc
Version D – 2002-Dec-09

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Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2002-July-15	Preliminary Draft	-
B	2002-July-29	• Small changes to the SEP supply requirements from Caltech • Add PLASTIC currents & mechanical • Add SEP mechanical	-
C	2002-Oct-17	• Update SEP LVPS voltages/currents • Update IDPU LVPS currents • Add IDPU LVPS Form Factor • Add SWEA connector pinout	-
D	2002-Dec-9	• Add SEP connector pinouts • Fix SWEA Pinouts • Add SWEA, IDPU load capacitance • Add reference to HVPS requirements document • Remove SEPT –5.1V supply • Update SEP loads per the CDR values • Add SEP capacitive load • Update SEP form factor	

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1. Introduction

This document describes the requirements on the low voltage and high voltage power converters being built at UCB for STEREO. This includes low voltage converters for the IMPACT IDPU, SEP, and SWEA/STE, a low voltage converter for PLASTIC, and a high voltage converter for SIT. UCB will design, build, and test these supplies according to these requirements prior to providing them to the instrument teams.

1.1. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by a code such as UCB indicating who is responsible for providing the data, and a unique reference number.

1.2. *Applicable Documents*

The following reference documents include drawings and STEREO Project policies. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

Or on the APL STEREO web site at:

https://sd-forum.jhuapl.edu/stereo/

1. Project/EMC_7881-9030_Rev- - EMC requirements
2. Project/EnvSpec7381-9003Rev- - Environmental specifications
3. Specifications/IDPUDesign_C - IDPU form factors & internal connectors
4. IMPACT_ICD_init_rev - Spacecraft to IMPACT ICD (APL)
5. hvps_requirements_rev1 – SIT HVPS requirements

2. LVPS Requirements

The 4 low voltage power converters shall convert primary spacecraft 28V into secondary voltages as indicated in Figure 2-1.

2.1. *Primary Characteristics*

Each of the 4 supplies shall have a separate switched spacecraft service, as indicated in reference 4. The characteristics of the spacecraft 28V supply are indicated in reference 2 (including ground isolation requirements).

2.2. *EMC*

The supplies shall meet the EMC requirements called out in reference 1, in particular the conducted emissions and susceptibility requirements. Reference 4 includes a typical front end (filter) circuit for the LVPS.

2.3. *Secondary Characteristics*

The supplies shall provide the voltages listed in Figure 2-1. These supplies shall be regulated to +/-5% (half load to full load). High frequency (supply-generated) ripple on the secondaries shall be less than 10mV peak to peak at Max Current.

2.3.1. Digital / Analog Ground

The digital supplies (highlighted in figure 2-1) shall have a separate return from the analog supplies (not highlighted). These returns will be tied together in the instrument.

2.3.2. SEPT Supplies

The SEPT supplies are part of the SEP supply. These supplies shall have separate secondaries with separate isolated returns (both analog and digital). There are two such SEPT supplies (one for SEPT-E and one for SEPT-NS).

2.3.3. Peak Current

Figure 2-1 lists the nominal and surge current requirements. The supply shall perform within specs for loads up to at least 50% above the nominal current indicated.

2.4. *Form Factor and Connector Definitions*

2.4.1. IDPU LVPS

The IDPU LVPS form factor is shown in Figure 2-7. The LVPS shall have an MDM connector between the LVPS half of the tray and the other side. The mating connector shall be wired from there to the power input connector (IDPU-J1; pinout as called out in Reference 4) and the internal connector to the other boards (pinout in reference 3). Mass estimate is 400g (excluding box).

2.4.2. SWEA LVPS

The SWEA LVPS form factor is shown in figure 2-2 and 2-3. The supply shall be harnessed to a connector type MM-222-021-261-41WC (M83513/04-C11N) that mates with the DAC board via a pig-tail. This connector pinout is shown in Figure 2.8.

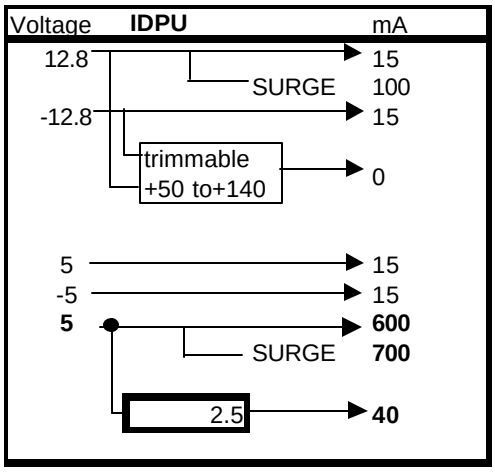
2.4.3. SEP LVPS

The SEP LVPS form factor is shown in figure 2-6. Secondary connector pinouts are shown in Figure 2-9. Primary power connector pinout is defined in reference 4. Mass estimate is 480g (including box).

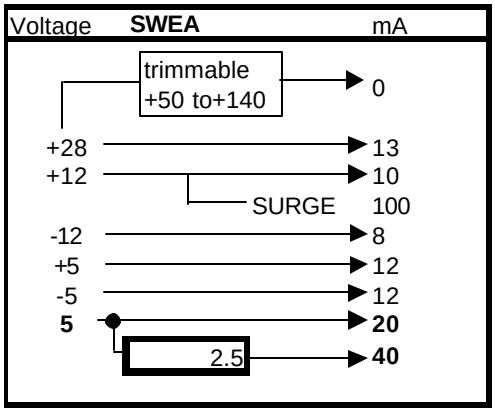
2.4.4. PLASTIC LVPS

The PLASTIC LVPS form factor is shown in figures 2-4 and 2-5. Secondary voltages are available on feed-through posts as shown. Pin assignments are TBD-UCB.

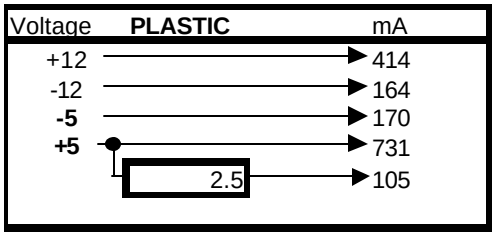
Figure 2-1 LVPS Voltage/Current Requirements



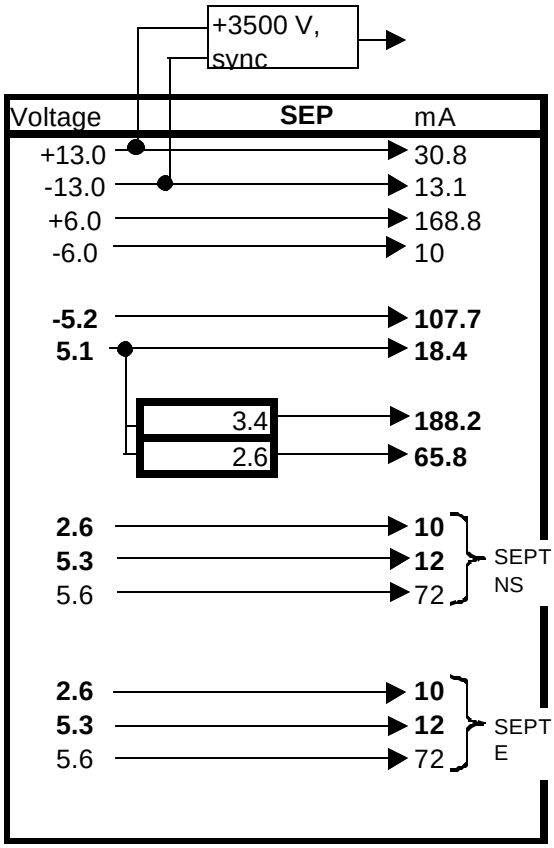
	WATTS	SURGE	CAPACITANCE
12.8	0.19		6.8uF+MAG
SURGE		1.28 Watts	
-12.8	0.19		6.8uF+MAG
trimmable +50 to+140			-
5	0.08		75uF
-5	0.08		75uF
5	3.00		51uF+MAG
SURGE		3.50 Watts	5uF
2.5	0.10		31uF
	3.63 Watts	8.41 Watts w/ surge	



	WATTS	SURGE	CAPACITANCE
trimmable +50 to+140			-
+28	0.36		4.7uF
+12	0.12		7.8uF
SURGE		1.20 Watts	
-12	0.10		7.8uF
+5	0.06		75uF
-5	0.06		75uF
5	0.10		34uF
2.5	0.10		0.7uF
	0.90 Watts	2.10 Watts w/ surge	



	WATTS	SURGE	CAPACITANCE
+12	4.97		25uF
-12	1.97		20uF
-5	0.85		20uF
+5	3.66		30uF
2.5	0.26		25uF
	11.70 Watts	(includes test port)	



	Watts	CAPACITANCE
	0.00	
+13.0 @ 30.8 mA	0.40	30 uF
-13.0 @ 13.1 mA	0.17	46 uF
+6.0 @ 168.8 mA	1.01	83 uF
-6.0 @ 10 mA	0.06	76 uF
-5.2 @ 107.7 mA	0.56	6 uF
5.1 @ 18.4 mA	0.09	102 uF
3.4 @ **188.2 mA**	0.64	136 uF
2.6 @ **65.8 mA**	0.17	104 uF
2.6 @ 10 mA (SEPTNS)	0.03	11 uF
5.3 @ 12 mA (SEPTNS)	0.06	12 uF
5.6 @ 72 mA (SEPTNS)	0.40	50 uF
2.6 @ 10 mA (SEPTE)	0.03	11 uF
5.3 @ 12 mA (SEPTE)	0.06	12 uF
5.6 @ 72 mA (SEPTE)	0.40	50 uF
	4.09 Watts	

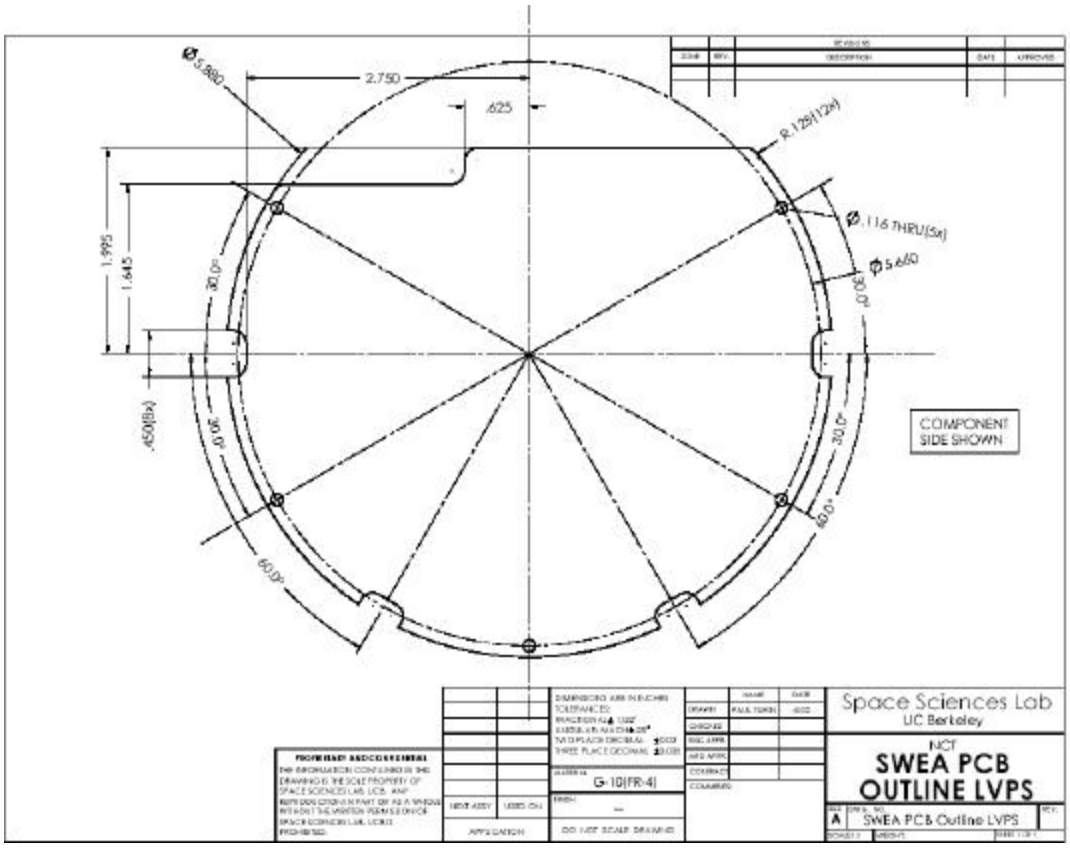


Figure 2-2 SWEA LVPS Form Factor

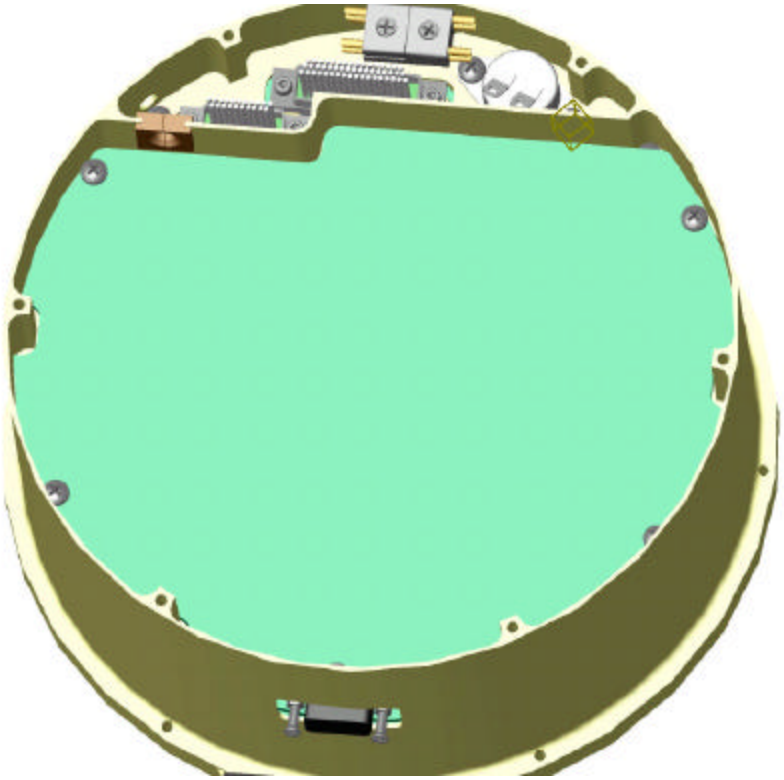


Figure 2-3 SWEA LVPS Form Factor

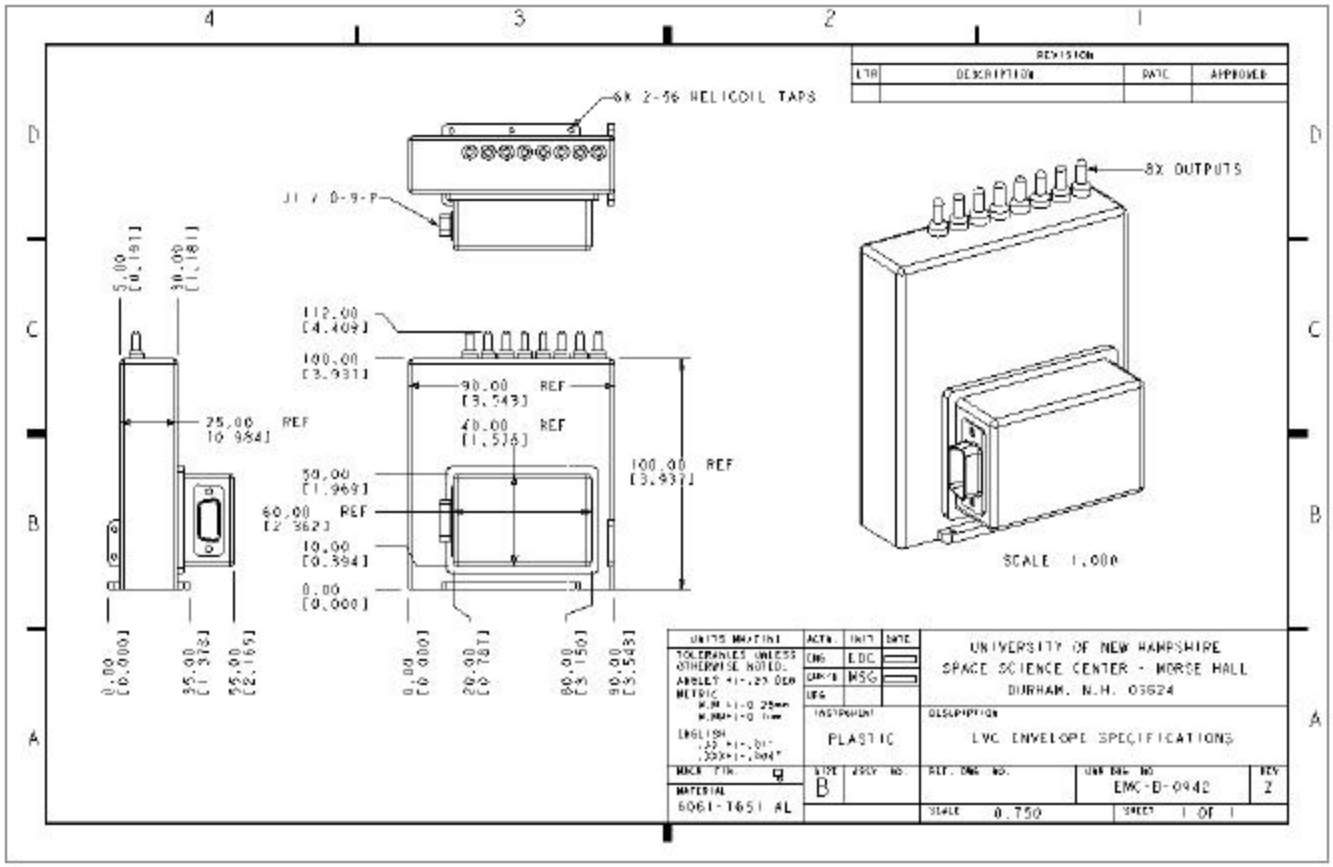


Figure 2-4, PLASTIC LVPS Form Factor

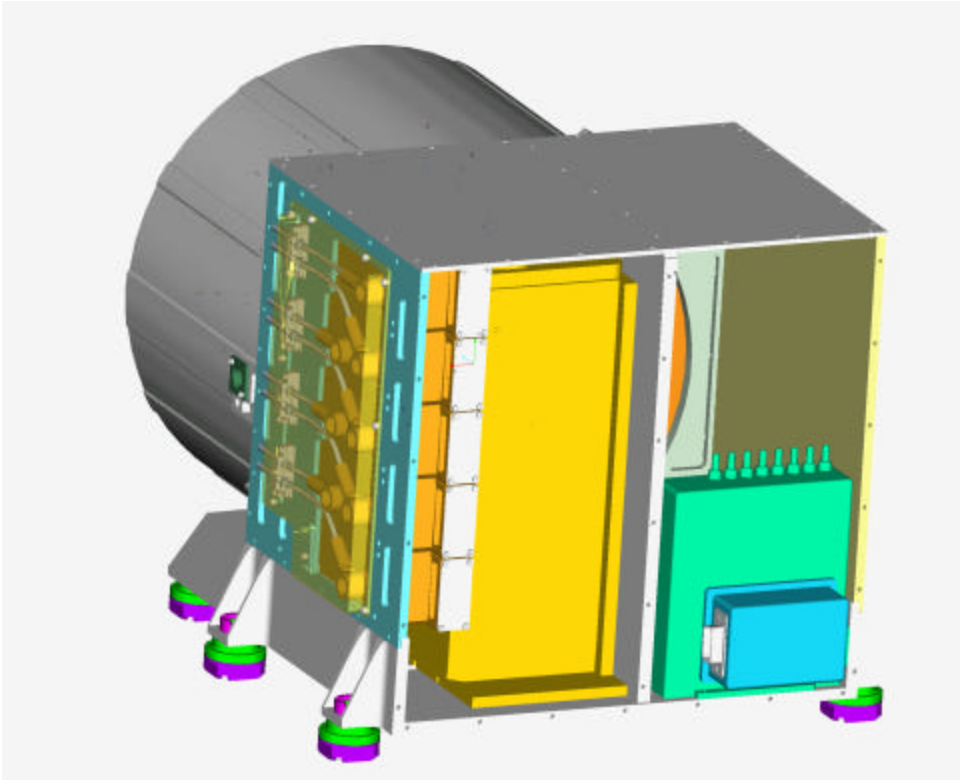


Figure 2-5, PLASTIC LVPS shown in PLASTIC

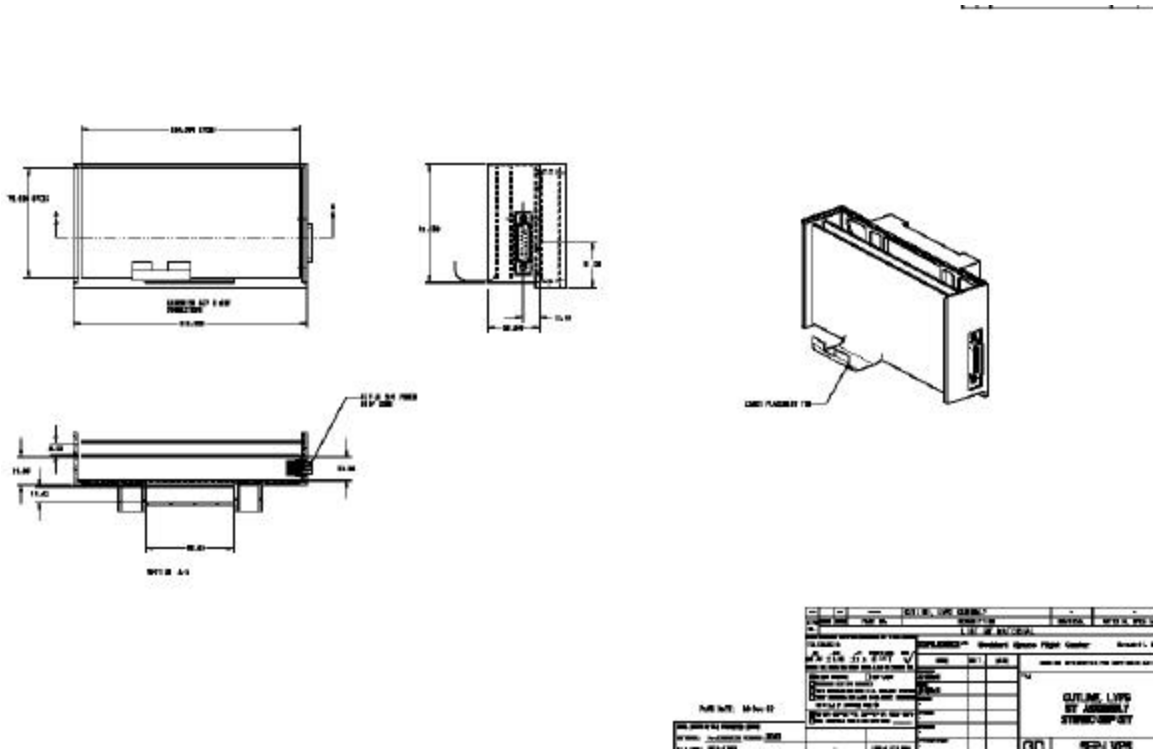


Figure 2-6 SEP LVPS form factor

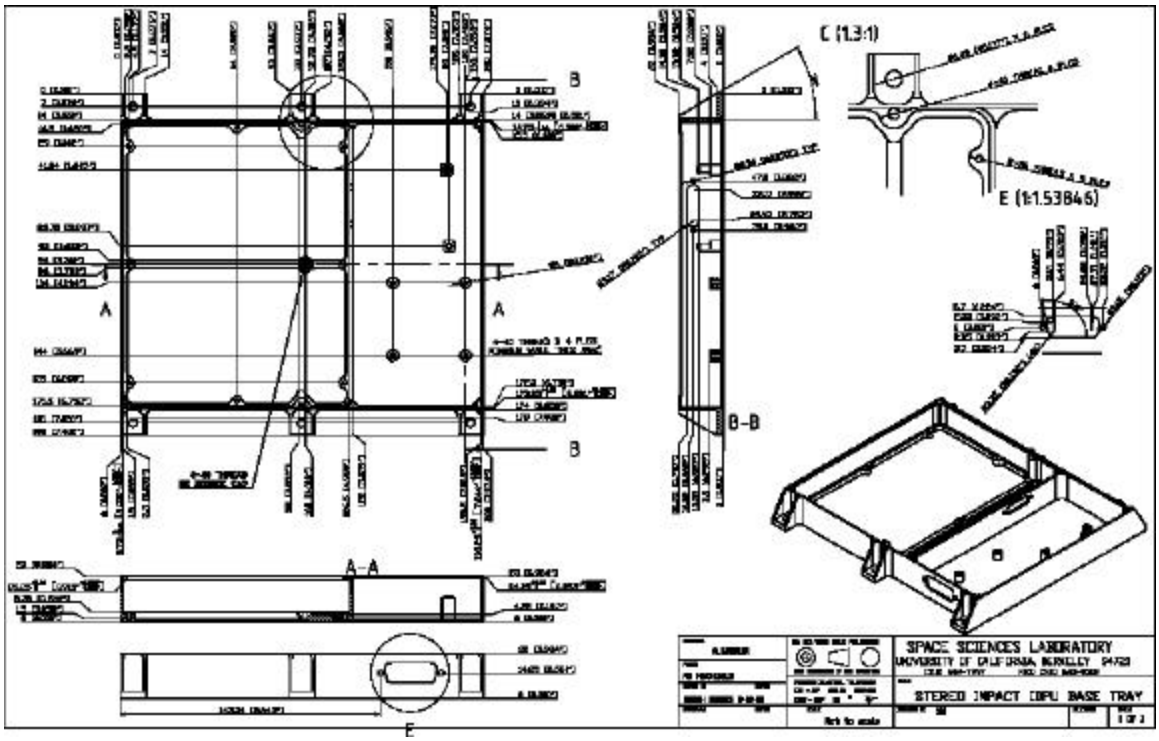


Figure 2-7 IDPU LVPS Form Factor

Airbourn M83513/04-C11N (on a pig-tail attached to the LVPS)

Pin	Signal
17	STE Bias Return
16	STE Bias (140V)
7,8	Digital Ground
14	VCC_A (2.5V)
6	+5VD
13,15,9,10	Analog Ground
20	+5.1VA
18	-5.1VA
10	+12.1VA
21	-12.1VA
5	+28V (secondary)
1	+28V primary
11	+28V primary Return
12	SWEA Temp Sensor
3	SWEA Temp Sensor Return
2	+28V Heater
4	+28V Heater Return

Note: Pins 2,3,4,12 do not route to the LVPS. They go from the DAC board to a Winchester connector mounted to the chassis outside the LVPS

Figure 2-8 SWEA LVPS Connector Pinout

LVPS connectors

12/3/02

Internal to SEP
SEP-J12A
LVPS output

1	SEPT-NS ANA RTN
33	SEPT-NS ANA RTN
2	SEPT-NS +5.6A
34	SEPT-NS +5.6A
3	Spare
35	Spare
4	SEPT-NS DIG RTN
36	SEPT-NS DIG RTN
5	SEPT-NS +2.6D
37	SEPT-NS +2.6D
6	SEPT-NS +5.3D
38	SEPT-NS +5.3D
7	SEPT-NS SEP STAR
39	SEPT-NS SEP STAR
8	SEPT-E ANA RTN
40	SEPT-E ANA RTN
9	SEPT-E +5.6A
41	SEPT-E +5.6A
10	Spare
42	Spare
11	SEPT-E DIG RTN
43	SEPT-E DIG RTN
12	SEPT-E +2.6D
44	SEPT-E +2.6D
13	SEPT-E +5.3D
45	SEPT-E +5.3D
14	SEPT-E SEP STAR
46	SEPT-E SEP STAR
15	SIT PWR RTN
47	SIT PWR RTN
16	SIT +13A
48	SIT +13A
17	SIT +6A
49	SIT +6A
18	SIT +5.1A RTN
50	SIT +5.1A RTN
19	SIT -6A
51	SIT -6A
20	SIT -13A
52	SIT -13A
21	SIT -5.2D
53	SIT -5.2D
22	SIT +2.6D
54	SIT +2.6D
23	SIT +3.4D
55	SIT +3.4D
24	SIT +5.1D
56	SIT +5.1D
25	HET PWR RTN
57	HET PWR RTN
26	HET +13A
58	HET +13A
27	HET +6A
59	HET +6A
28	HET -6A
60	HET -6A
29	HET -13A
61	HET -13A
30	HET +2.6D
62	HET +2.6D
31	HET +3.4D
63	HET +3.4D
32	HET +5.1D
64	HET +5.1D
65	Spare

External to SEP
SEP-J1
S/C power & heaters

1	Spare
2	+28V MAIN/OP HTR
3	+28V MAIN/OP HTR
4	Spare
5	+28V SURV HTR
6	+28V SURV HTR
7	Spare
8	CHASSIS
9	Spare
10	+28V MAIN/OP HTR RTN
11	+28V MAIN/OP HTR RTN
12	Spare
13	+28V SURV HTR RTN
14	+28V SURV HTR RTN
15	Spare

Internal to SEP
SEP-J12B
LVPS output

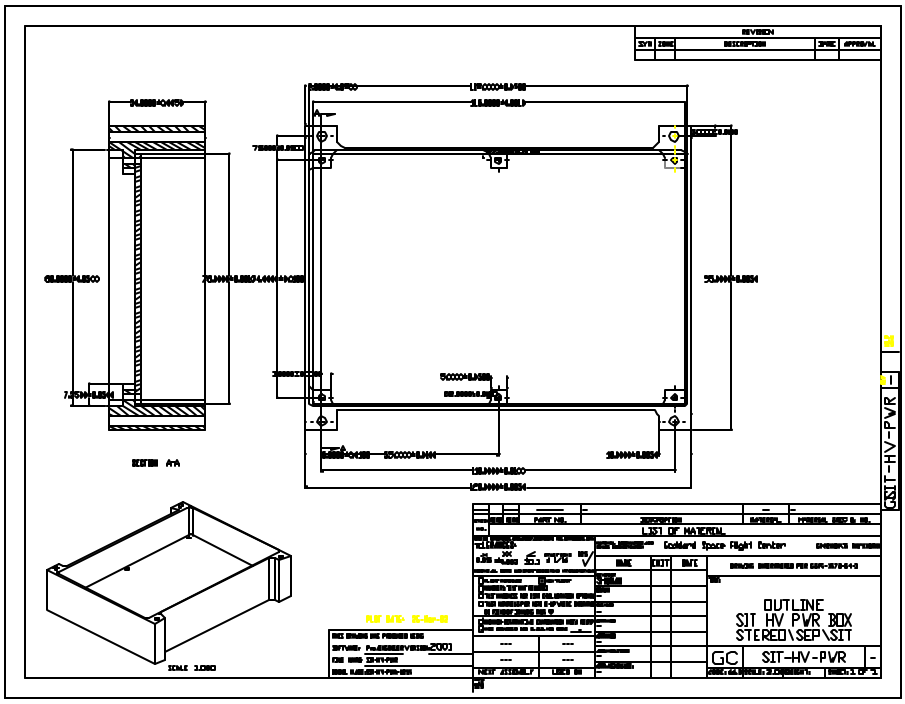
1	LET PWR RTN
26	LET PWR RTN
2	LET +13A
27	LET +13A
3	LET +6A
28	LET +6A
4	LET -6A
29	LET -6A
5	LET -13A
30	LET -13A
6	LET +2.6D
31	LET +2.6D
7	LET +3.4D
32	LET +3.4D
8	LET +5.1D
33	LET +5.1D
9	CENTRAL ANA RTN
34	CENTRAL ANA RTN
10	CENTRAL +13A
35	CENTRAL +13A
11	CENTRAL +6A
36	CENTRAL +6A
12	CENTRAL -6A
37	CENTRAL -6A
13	CENTRAL -13A
38	CENTRAL -13A
14	CENTRAL DIG RTN
39	CENTRAL DIG RTN
15	CENTRAL +2.6D
40	CENTRAL +2.6D
16	CENTRAL +3.4D
41	CENTRAL +3.4D
17	CENTRAL +5.1D
42	CENTRAL +5.1D
18	BIAS RTN
43	BIAS RTN
19	LVPS TEMP SENSOR
44	Spare
20	Spare
45	Spare
21	Spare
46	Spare
22	Spare
47	+28V SURV HTR
23	+28V SURV HTR
48	+28V SURV HTR RTN
24	+28V SURV HTR RTN
49	+28V OP HTR
25	+28V OP HTR
50	+28V OP HTR RTN
51	+28V OP HTR RTN

Figure 2-9 SEP LVPS Connector pinouts

3. SIT HVPS Requirements

The SIT HVPS is part of the SIT instrument. It takes secondary +/-12V and generates a programmable output voltage at up to +3500V plus a number of proportional taps. This supply provides no ground isolation, and does not need to meet the conducted EMC requirements of reference 1. Detailed electrical requirements are described in reference 5.

3.1. *Form Factor*



3.2. *Connectors*

The input connector is described in reference 5. The output shall be un-terminated wires which shall be terminated in the SIT instrument. The wires must be shielded in a continuous fashion between the boxes providing no gap.