STEREO
IMPACT

IMPACT/PLASTIC Low Voltage Power Converter Requirements

LVPSRequirements_C.doc
Version C – 2002-Oct-17

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Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2002-July-15	Preliminary Draft	-
B	2002-July-29	• Small changes to the SEP supply requirements from Caltech • Add PLASTIC currents & mechanical • Add SEP mechanical	-
C	2002-Oct-17	• Update SEP LVPS voltages/currents • Update IDPU LVPS currents • Add IDPU LVPS Form Factor • Add SWEA connector pinout	

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1. Introduction

This document describes the requirements on the low voltage and high voltage power converters being built at UCB for STEREO. This includes low voltage converters for the IMPACT IDPU, SEP, and SWEA/STE, a low voltage converter for PLASTIC, and a high voltage converter for SIT. UCB will design, build, and test these supplies according to these requirements prior to providing them to the instrument teams.

1.1. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by a code such as UCB indicating who is responsible for providing the data, and a unique reference number.

1.2. *Applicable Documents*

The following reference documents include drawings and STEREO Project policies. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

Or on the APL STEREO web site at:

https://sd-forum.jhuapl.edu/stereo/

1. Project/EMC_7881-9030_Rev- - EMC requirements
2. Project/EnvSpec7381-9003Rev- - Environmental specifications
3. Specifications/IDPUDesign_C - IDPU form factors & internal connectors
4. IMPACT_ICD_init_rev - Spacecraft to IMPACT ICD (APL)

2. LVPS Requirements

The 4 low voltage power converters shall convert primary spacecraft 28V into secondary voltages as indicated in Figure 2-1.

2.1. *Primary Characteristics*

Each of the 4 supplies shall have a separate switched spacecraft service, as indicated in reference 4. The characteristics of the spacecraft 28V supply are indicated in reference 2 (including ground isolation requirements).

2.2. *EMC*

The supplies shall meet the EMC requirements called out in reference 1, in particular the conducted emissions and susceptibility requirements. Reference 4 includes a typical front end (filter) circuit for the LVPS.

2.3. *Secondary Characteristics*

The supplies shall provide the voltages listed in Figure 2-1. These supplies shall be regulated to +/-5% (half load to full load). High frequency (supply-generated) ripple on the secondaries shall be less than 10mV peak to peak at Max Current.

2.3.1. Digital / Analog Ground

The digital supplies (highlighted in figure 2-1) shall have a separate return from the analog supplies (not highlighted). These returns will be tied together in the instrument.

2.3.2. SEPT Supplies

The SEPT supplies are part of the SEP supply. These supplies shall have separate secondaries with separate isolated returns (both analog and digital). There are two such SEPT supplies (one for SEPT-E and one for SEPT-NS).

2.3.3. Peak Current

Figure 2-1 lists the nominal and surge current requirements. The supply shall perform within specs for loads up to at least 50% above the nominal current indicated.

2.4. *Form Factor and Connector Definitions*

2.4.1. IDPU LVPS

The IDPU LVPS form factor is shown in Figure 2-7. The LVPS shall have an MDM connector between the LVPS half of the tray and the other side. The mating connector shall be wired from there to the power input connector (IDPU-J1; pinout as called out in Reference 4) and the internal connector to the other boards (pinout in reference 3). Mass estimate is 400g (excluding box).

2.4.2. SWEA LVPS

The SWEA LVPS form factor is shown in figure 2-2 and 2-3. The supply shall be harnessed to a connector type MM-222-021-261-41WC (M83513/04-C11N) that mates with the DAC board via a pig-tail. This connector pinout is shown in Figure 2.8.

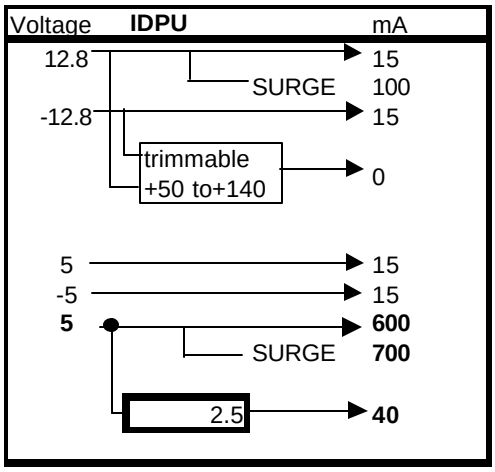
2.4.3. SEP LVPS

The SEP LVPS form factor is shown in figure 2-6. Secondary connector pinouts are TBD. Primary power connector pinout is defined in reference 4. Mass estimate is 480g (including box).

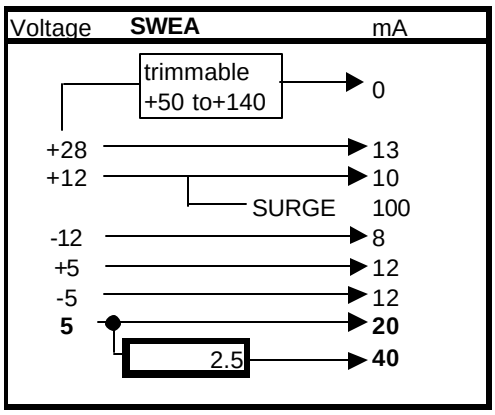
2.4.4. PLASTIC LVPS

The PLASTIC LVPS form factor is shown in figures 2-4 and 2-5. Secondary voltages are available on feed-through posts as shown. Pin assignments are TBD-UCB.

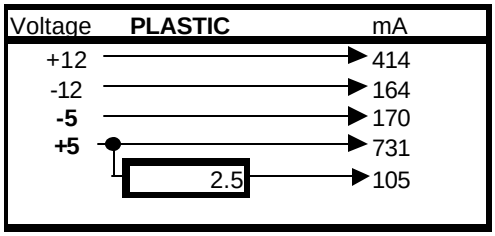
Figure 2-1 LVPS Voltage/Current Requirements



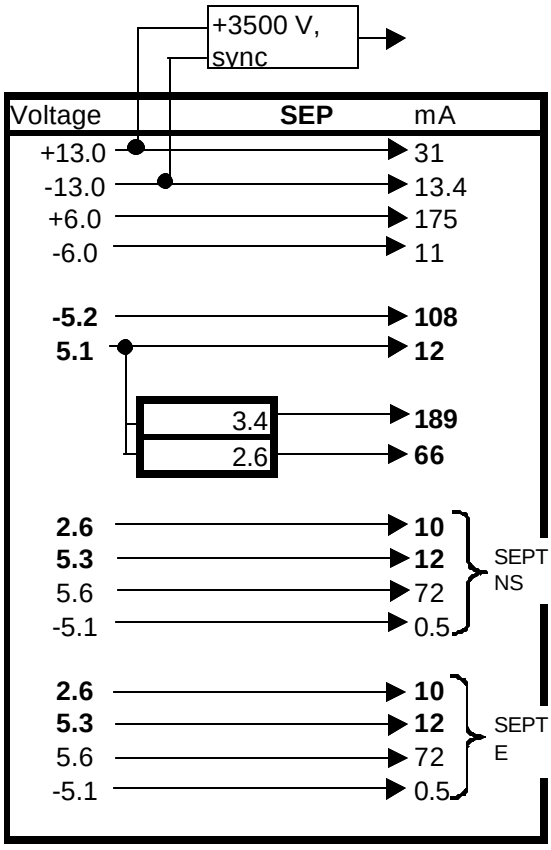
	WATTS		SURGE	CAPACITANCE
12.8	0.19			
SURGE			1.28	Watts
-12.8	0.19			
trimmable +50 to+140				
5	0.08			
-5	0.08			
5	3.00			
SURGE			3.50	Watts
2.5	0.10			
	3.63	Watts	8.41	Watts w/ surge



	WATTS		SURGE	CAPACITANCE
trimmable +50 to+140				
+28	0.36			
+12	0.12			
SURGE			1.20	Watts
-12	0.10			
+5	0.06			
-5	0.06			
5	0.10			
2.5	0.10			
	0.90	Watts	2.10	Watts w/ surge



	WATTS		SURGE	CAPACITANCE
+12	4.97			25uF
-12	1.97			20uF
-5	0.85			20uF
+5	3.66			30uF
2.5	0.26			25uF
	11.70	Watts	(includes test port)	



	Watts
	0.00
	0.40
	0.17
	1.05
	0.07
	0.56
	0.06
	0.64
	0.17
	0.03
	0.06
	0.40
	0.00
	0.03
	0.06
	0.40
	0.00
	4.12 Watts

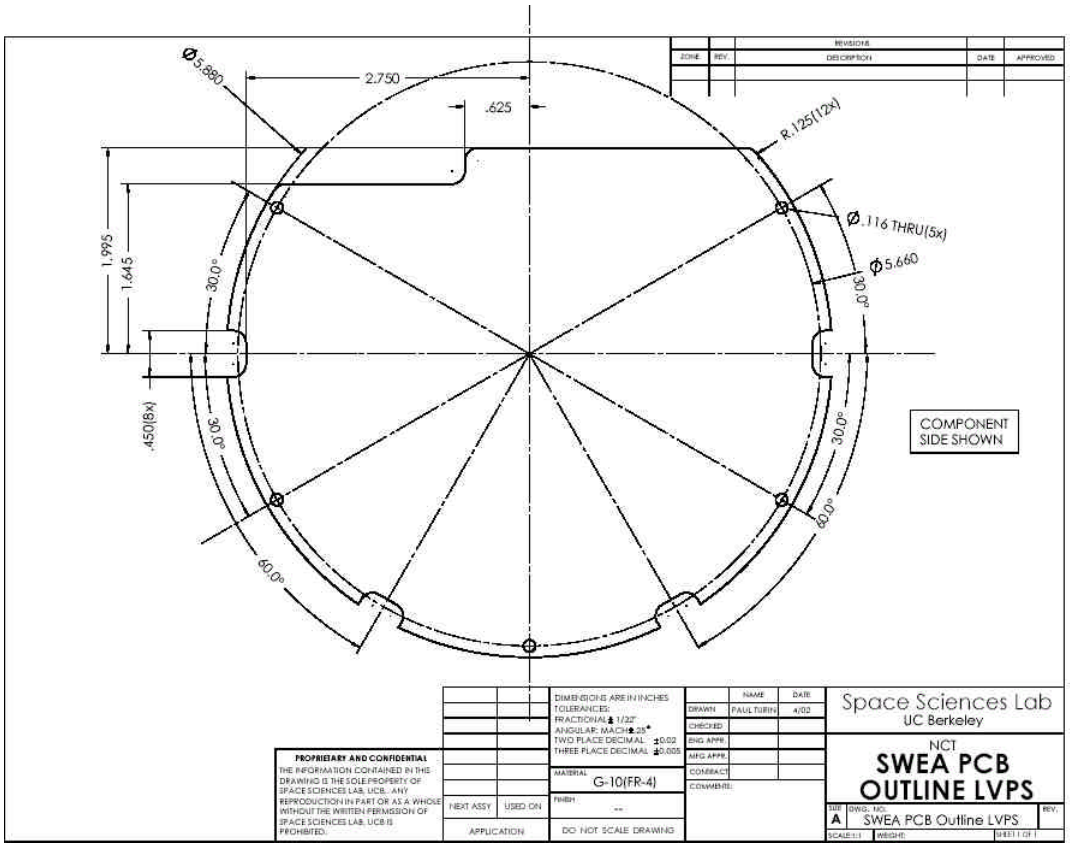


Figure 2-2 SWEA LVPS Form Factor

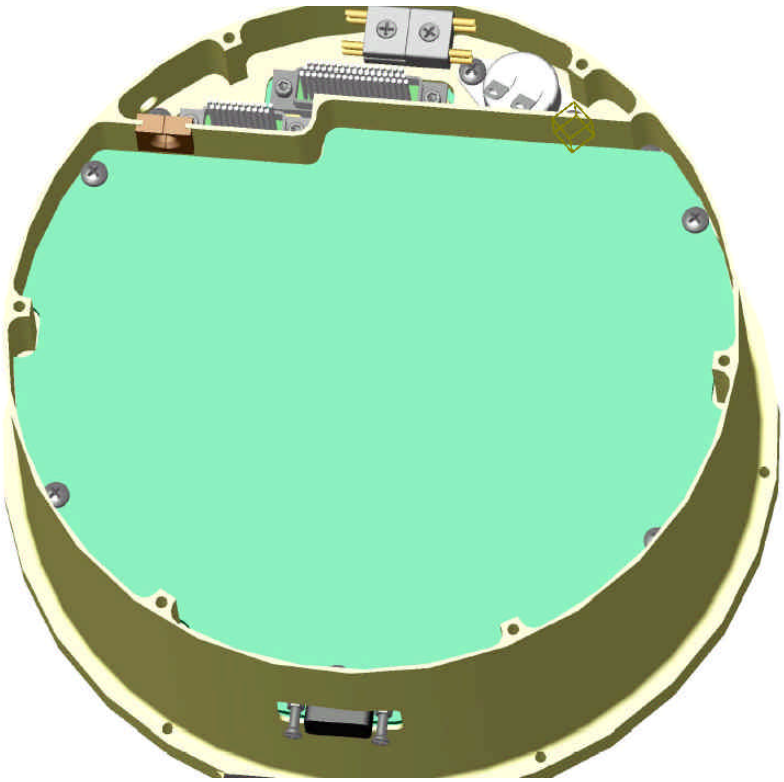


Figure 2-3 SWEA LVPS Form Factor

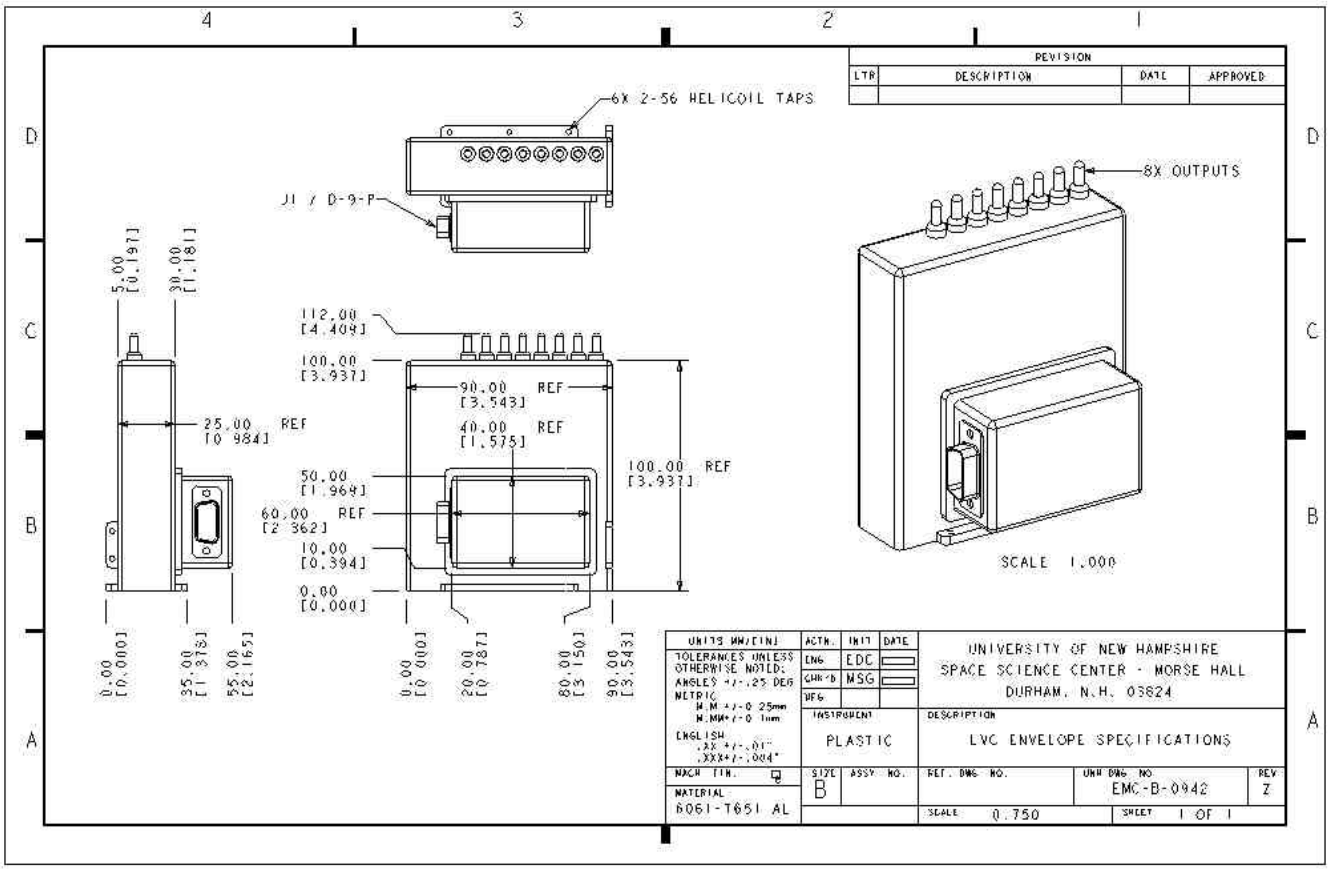


Figure 2-4, PLASTIC LVPS Form Factor

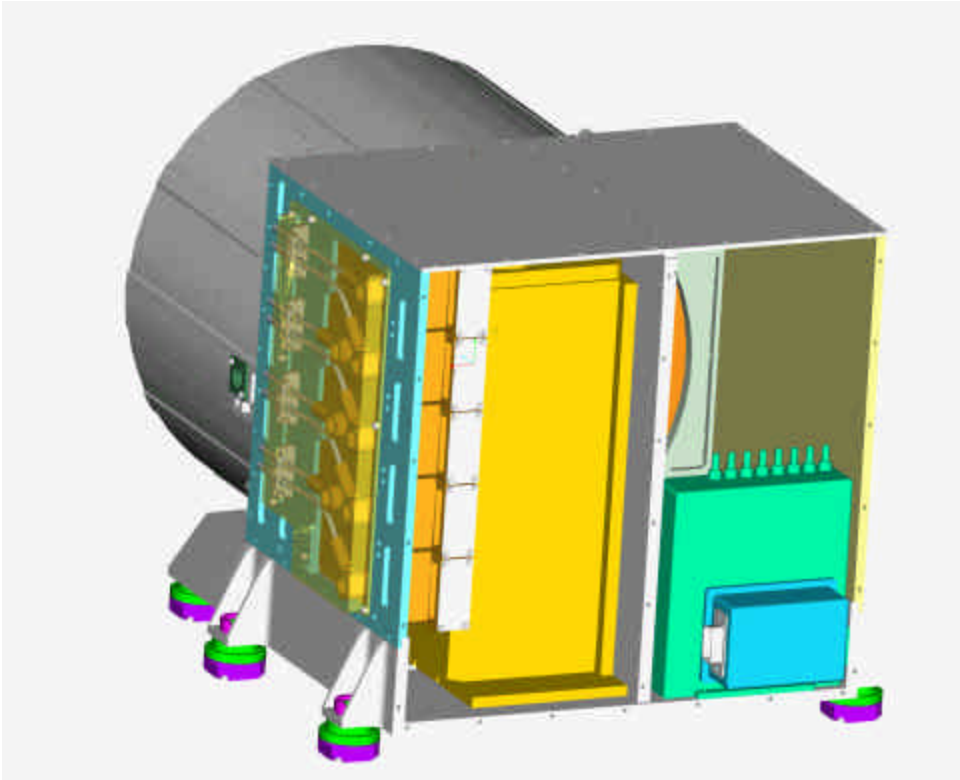


Figure 2-5, PLASTIC LVPS shown in PLASTIC

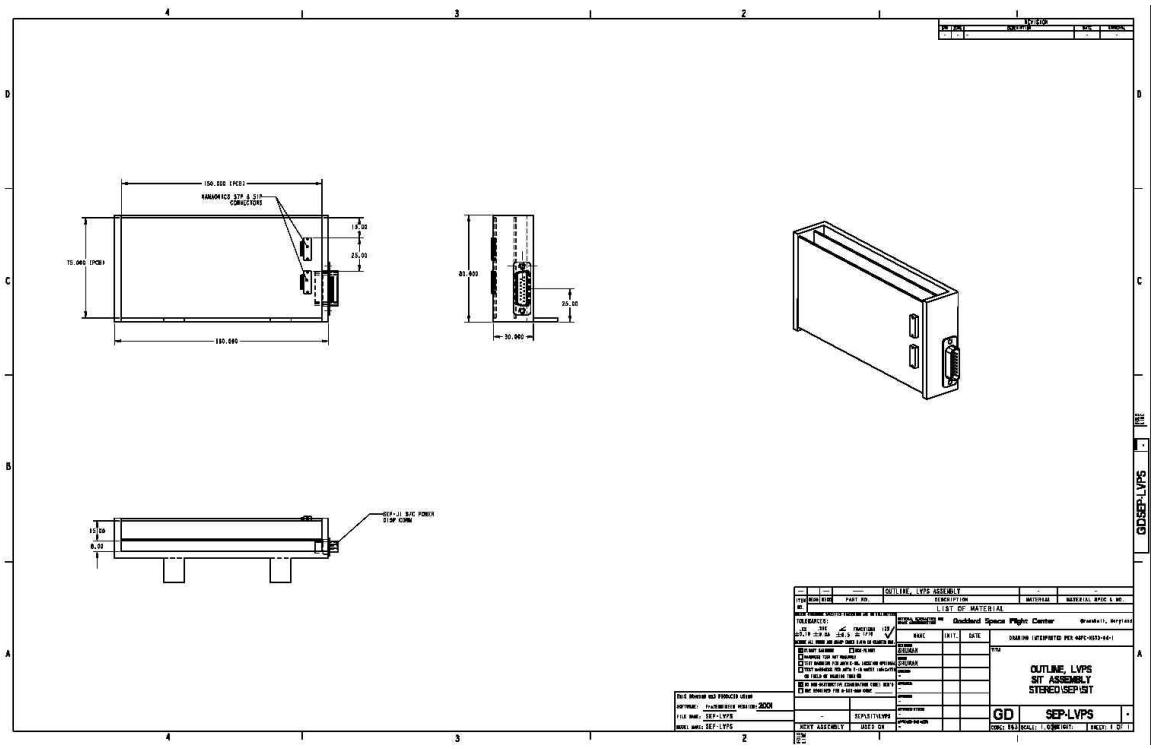


Figure 2-6 SEP LVPS form factor

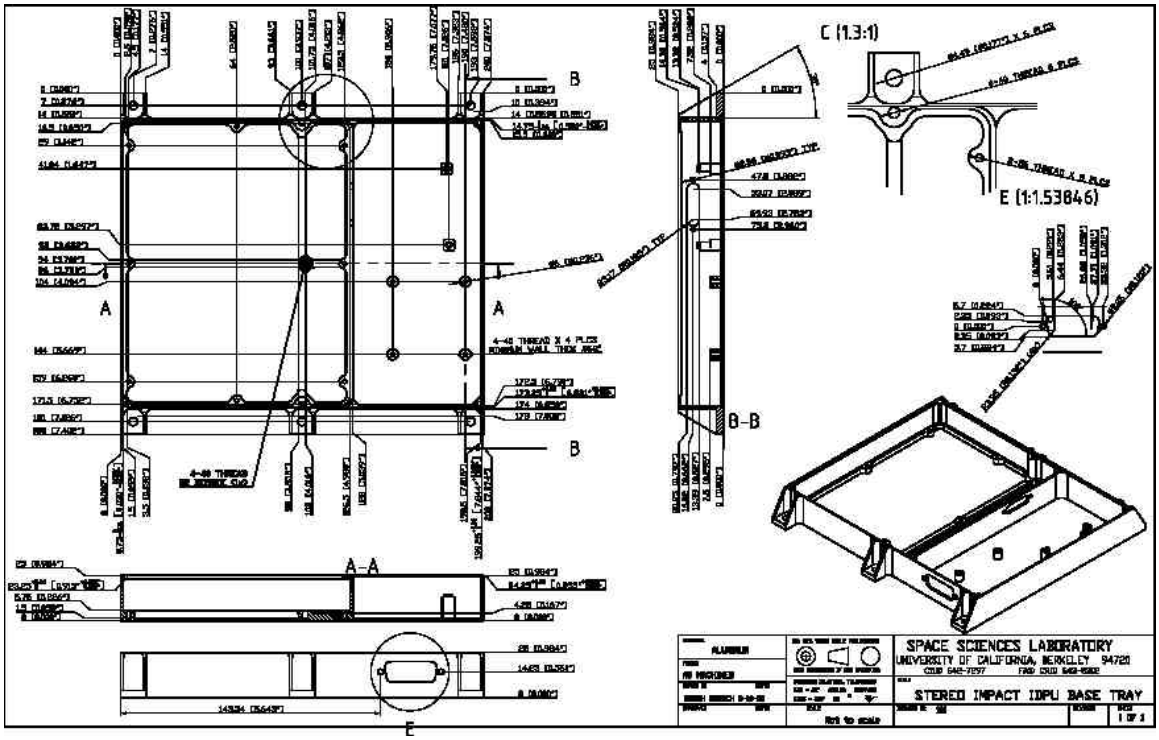


Figure 2-7 IDPU LVPS Form Factor

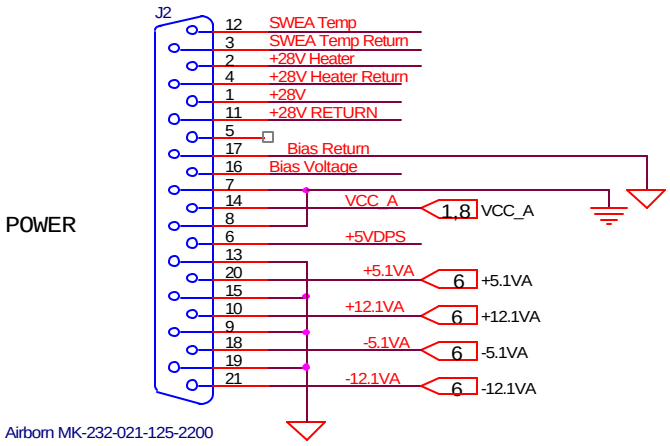


Figure 2-8 SWEA LVPS Connector Pinout (DAC board end)

3. SIT HVPS Requirements

The SIT HVPS is part of the SIT instrument. It takes secondary +/-12V and generates a programmable output voltage at up to +3500V plus a number of proportional taps. This supply provides no ground isolation, and does not need to meet the conducted EMC requirements of reference 1.

3.1. *Synchronization*

The supply shall be synchronized by a 100kHz digital signal provided on the input connector. In the absence of this synchronization signal the converter will continue to run, but at an uncontrolled frequency near 100kHz.

3.2. *Control*

An analog signal shall control the SIT HVPS output with a voltage gain of 840.

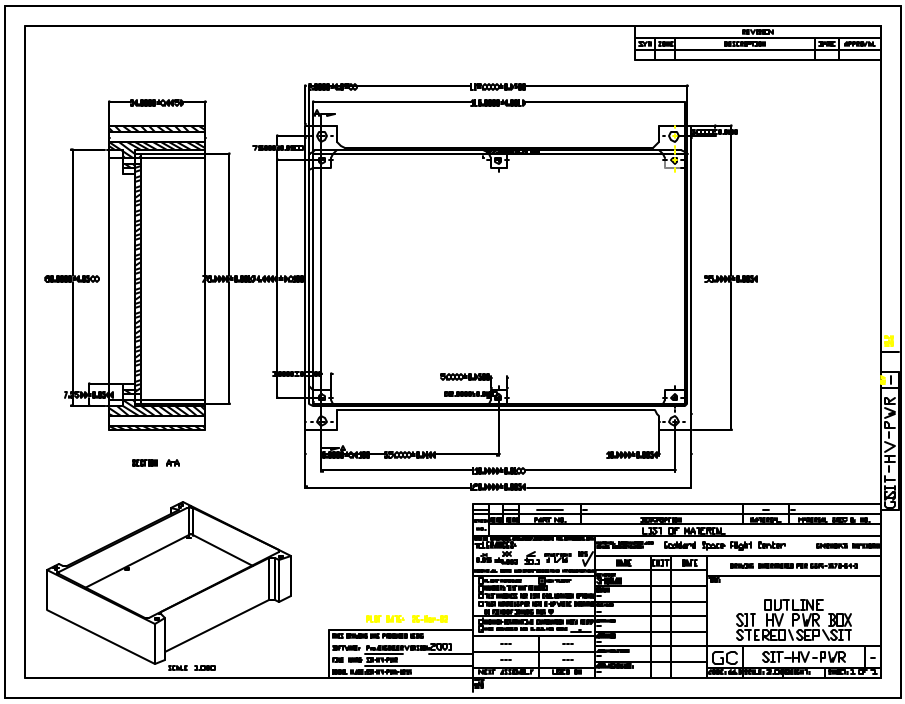
3.3. *Input Requirements*

The supply runs off +/-12V, +/-10%, at TBDmA. The current ripple shall be less than TBDmA peak-peak.

3.4. *Output Requirements*

The supply shall provide a primary programmable voltage between zero and +4200V, based on the control signal described in 3.2. In addition there shall be a number of taps proportional to this voltage generated by resistor dividers and alternate taps on the HV stack. The voltage and current requirements are given in table TBD. The output ripple shall be less that TBD at maximum load.

3.5. *Form Factor*



3.6. *Connectors*

The input connector is an MDM -9-S-H-003-B-A174. The output shall be have un-terminated wires which shall be terminated in the SIT instrument. The wires must be shielded in a continuous fashion between the boxes providing no gap.