STEREO
IMPACT

IMPACT/PLASTIC Power Converter Requirements

LVPSRequirements_H.doc
Version H – 2003-Nov-25

David Curtis, UCB IMPACT Project Manager

Peter Berg, UCB LVPS Designer

Document Revision Record

Rev.	Date	Description of Change	Approved By
A	2002-July-15	Preliminary Draft	-
B	2002-July-29	• Small changes to the SEP supply requirements from Caltech • Add PLASTIC currents & mechanical • Add SEP mechanical	-
C	2002-Oct-17	• Update SEP LVPS voltages/currents • Update IDPU LVPS currents • Add IDPU LVPS Form Factor • Add SWEA connector pinout	-
D	2002-Dec-9	• Add SEP connector pinouts • Fix SWEA Pinouts • Add SWEA, IDPU load capacitance • Add reference to HVPS requirements document • Remove SEPT –5.1V supply • Update SEP loads per the CDR values • Add SEP capacitive load • Update SEP form factor	-
E	2003-Feb-25	• PLASTIC +/-5V -> +/-5.5V • PLASTIC loads change • Split PLASTIC 2.5V Load, change connector • Update SEP power consumption & add distribution & min/max figures • Update SEP power connector	
F	2003-Mar-5	• Update SEP loads & capacitance (figures 2-1, 2-2a-c). Fig 2-1 contains has max case. • Update PLASTIC LVPS form factor (fig 2-4)	
G	2003-Jun-10	• Update PLASTIC output connector, add input connector • Fix piout of SWEA connector	
H	2003-Nov-25	• Increased load on IDPU and SWEA +/-5VA • New SWEA LVPS form factor • Update IDPU MAG (12.8V) current	

Distribution List

Dave Curtis, UCB
Peter Berg, UCB
Steve McBride, UCB
Branislav Kecman, Caltech
Peter Walpole, UMd
Reinhold Mueller-Mellin, U.Kiel
Ludovic Duvet, ESTEC
Tycho von Ronsenvinge, GSFC
John Schiefele, GSFC
Claude Aoustin, CESR
Steve Turco, UNH

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1. Introduction

This document describes the requirements on the low voltage and high voltage power converters being built at UCB for STEREO. This includes low voltage converters for the IMPACT IDPU, SEP, and SWEA/STE, a low voltage converter for PLASTIC, and a high voltage converter for SIT. UCB will design, build, and test these supplies according to these requirements prior to providing them to the instrument teams.

1.1. *Document Conventions*

In this document, TBD (To Be Determined) means that no data currently exists. A value followed by TBR (To Be Resolved) means that this value is preliminary. In either case, the value is typically followed by a code such as UCB indicating who is responsible for providing the data, and a unique reference number.

1.2. *Applicable Documents*

The following reference documents include drawings and STEREO Project policies. All documents and drawings can be found on the Berkeley STEREO/IMPACT FTP site:

http://sprg.ssl.berkeley.edu/impact/dwc/

Or on the APL STEREO web site at:

https://sd-forum.jhuapl.edu/stereo/

1. Project/EMC_7881-9030_RevB - EMC requirements
2. Project/EnvSpec7381-9003RevB - Environmental specifications
3. Specifications/IDPUDesign_D - IDPU form factors & internal connectors
4. IMPACT_ICD_RevA - Spacecraft to IMPACT ICD (APL)
5. hvps_requirements_rev1 – SIT HVPS requirements

2. LVPS Requirements

The 4 low voltage power converters shall convert primary spacecraft 28V into secondary voltages as indicated in Figure 2-1.

2.1. *Primary Characteristics*

Each of the 4 supplies shall have a separate switched spacecraft service, as indicated in reference 4. The characteristics of the spacecraft 28V supply are indicated in reference 2 (including ground isolation requirements).

2.2. *EMC*

The supplies shall meet the EMC requirements called out in reference 1, in particular the conducted emissions and susceptibility requirements. Reference 4 includes a typical front end (filter) circuit for the LVPS.

2.3. *Secondary Characteristics*

The supplies shall provide the voltages listed in Figure 2-1. These supplies shall be regulated to +/-5% (half load to full load). High frequency (supply-generated) ripple on the secondaries shall be less than 10mV peak to peak at Max Current.

2.3.1. Digital / Analog Ground

The digital supplies (highlighted in figure 2-1) shall have a separate return from the analog supplies (not highlighted). These returns will be tied together in the instrument.

2.3.2. SEPT Supplies

The SEPT supplies are part of the SEP supply. These supplies shall have separate secondaries with separate isolated returns (both analog and digital). There are two such SEPT supplies (one for SEPT-E and one for SEPT-NS).

2.3.3. Peak Current

Figure 2-1 lists the nominal and surge current requirements. The supply shall perform within specs for loads up to at least 50% above the nominal current indicated.

2.4. *Form Factor and Connector Definitions*

2.4.1. IDPU LVPS

The IDPU LVPS form factor is shown in Figure 2-7. The LVPS shall have an MDM connector between the LVPS half of the tray and the other side. The mating connector shall be wired from there to the power input connector (IDPU-J1; pinout as called out in Reference 4) and the internal connector to the other boards (pinout in reference 3). Mass estimate is 400g (excluding box).

2.4.2. SWEA LVPS

The SWEA LVPS form factor is shown in figure 2-2 and 2-3. The supply shall be harnessed to a connector type MM-222-021-261-41WC (M83513/04-C11N) that mates with the DAC board via a pig-tail. This connector pinout is shown in Figure 2.8.

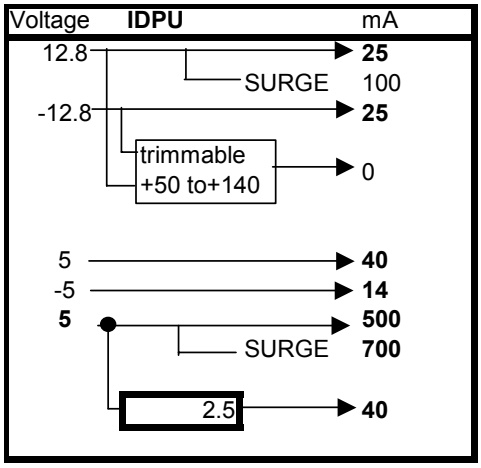
2.4.3. SEP LVPS

The SEP LVPS form factor is shown in figure 2-6. Secondary connector pinouts are shown in Figure 2-9. Primary power connector pinout is defined in reference 4. Mass estimate is 480g (including box). Figure 2.1a/b shows the SEP power flow to the various subsystems. Figure 2.1c shows the min/max power consumption for SEP. At SEP turn-on loads are at the absolute minimum: in the worst case it can take up to 4 minutes to boot; nominally it takes 1 minute. Following the turn-on boot process SEP will operate in the low-power state indefinitely.

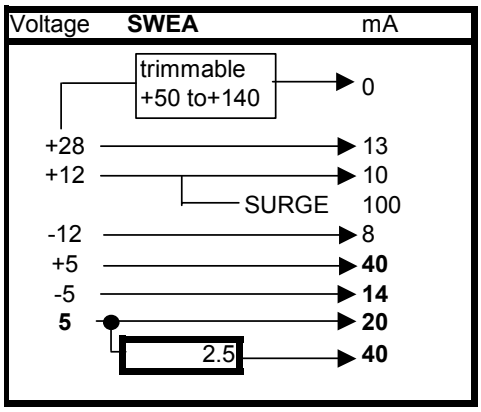
2.4.4. PLASTIC LVPS

The PLASTIC LVPS form factor is shown in figures 2-4 and 2-5. Secondary voltages are available on feed-through posts as shown. Pin assignments for the output connector are shown in figure 2-10. Pinout for the input (spacecraft) connector is shown in figure 2-11.

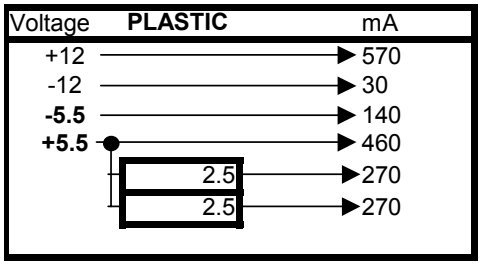
Figure 2-1 LVPS Voltage/Current Requirements



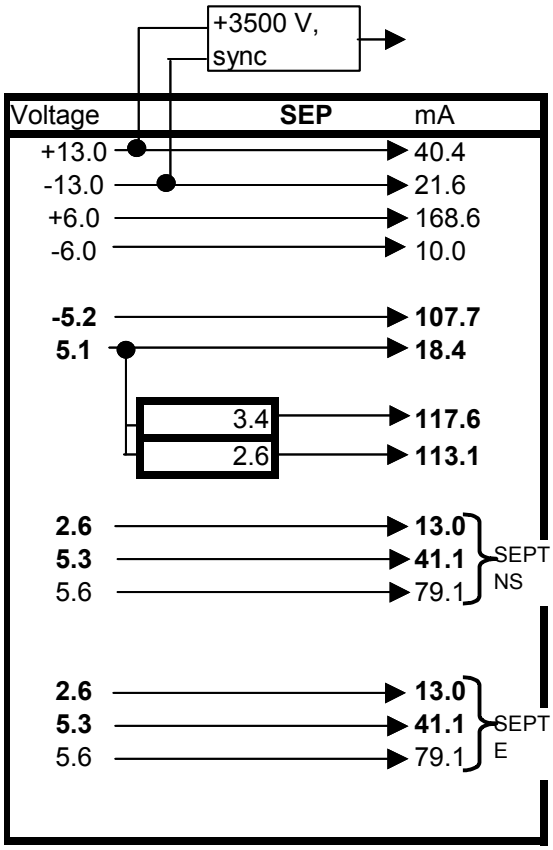
WATTS	SURGE	CAPACITANCE
0.32		6.8uF+MAG
	1.28 Watts	
0.32		6.8uF+MAG
		-
0.20	**90** mA (*)	75uF
0.07	**60** mA (*)	75uF
2.50		51uF+MAG
	3.50 Watts	5uF
0.10		31uF
3.51 Watts	8.77 Watts w/ surge	
	(*) - during high count rate	



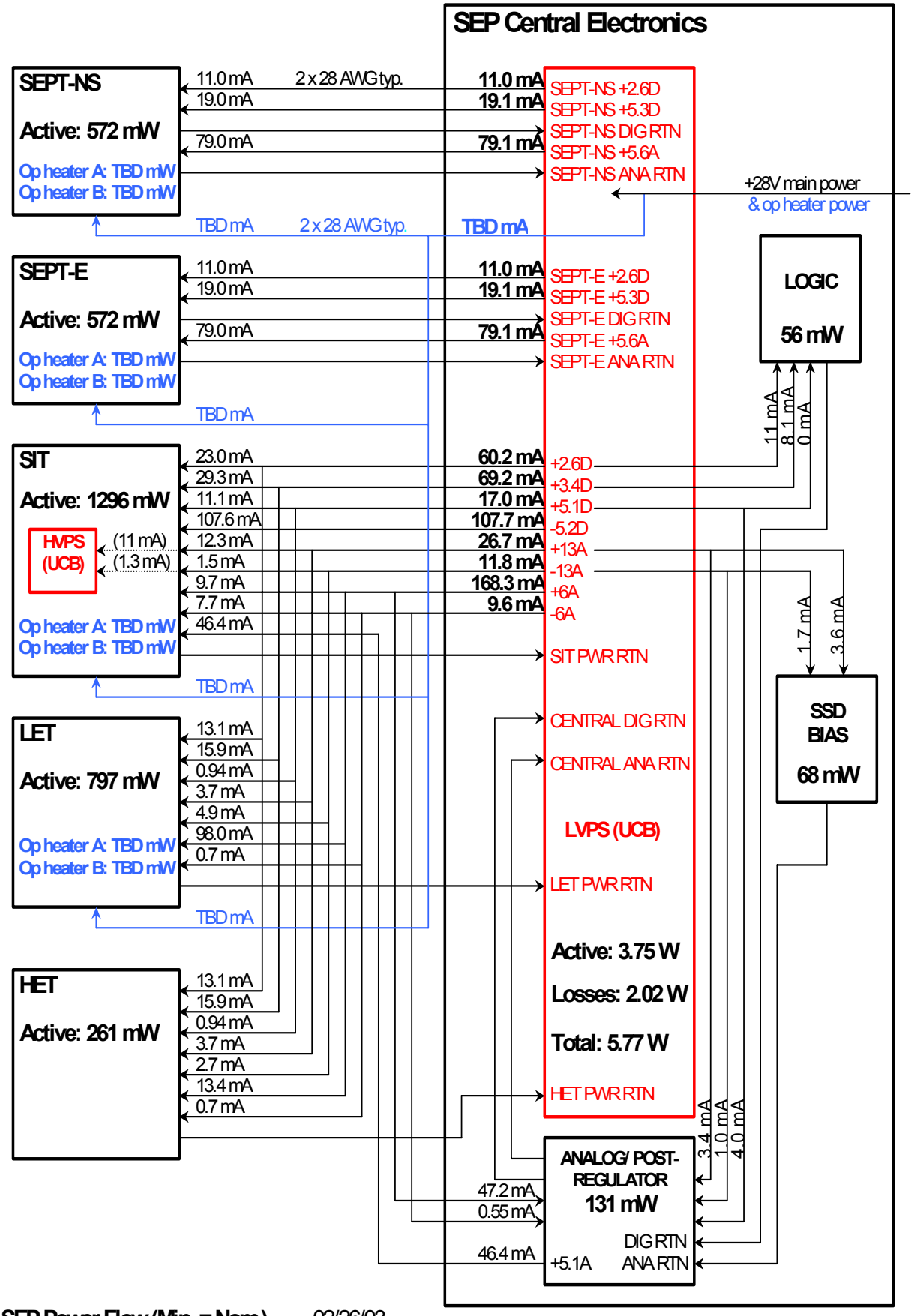
WATTS	SURGE	CAPACITANCE
		-
0.36		4.7uF
0.12		7.8uF
	1.20 Watts	
0.10		7.8uF
0.20	**90** mA (*)	75uF
0.07	**60** mA (*)	75uF
0.10		34uF
0.10		0.7uF
1.05 Watts	2.73 Watts w/ surge	
	(*) - during high count rate	



WATTS	SURGE	CAPACITANCE
6.84		25uF
0.36		20uF
0.77		20uF
2.53		30uF
0.68		?
0.68		25uF
11.85 Watts	(includes test port)	

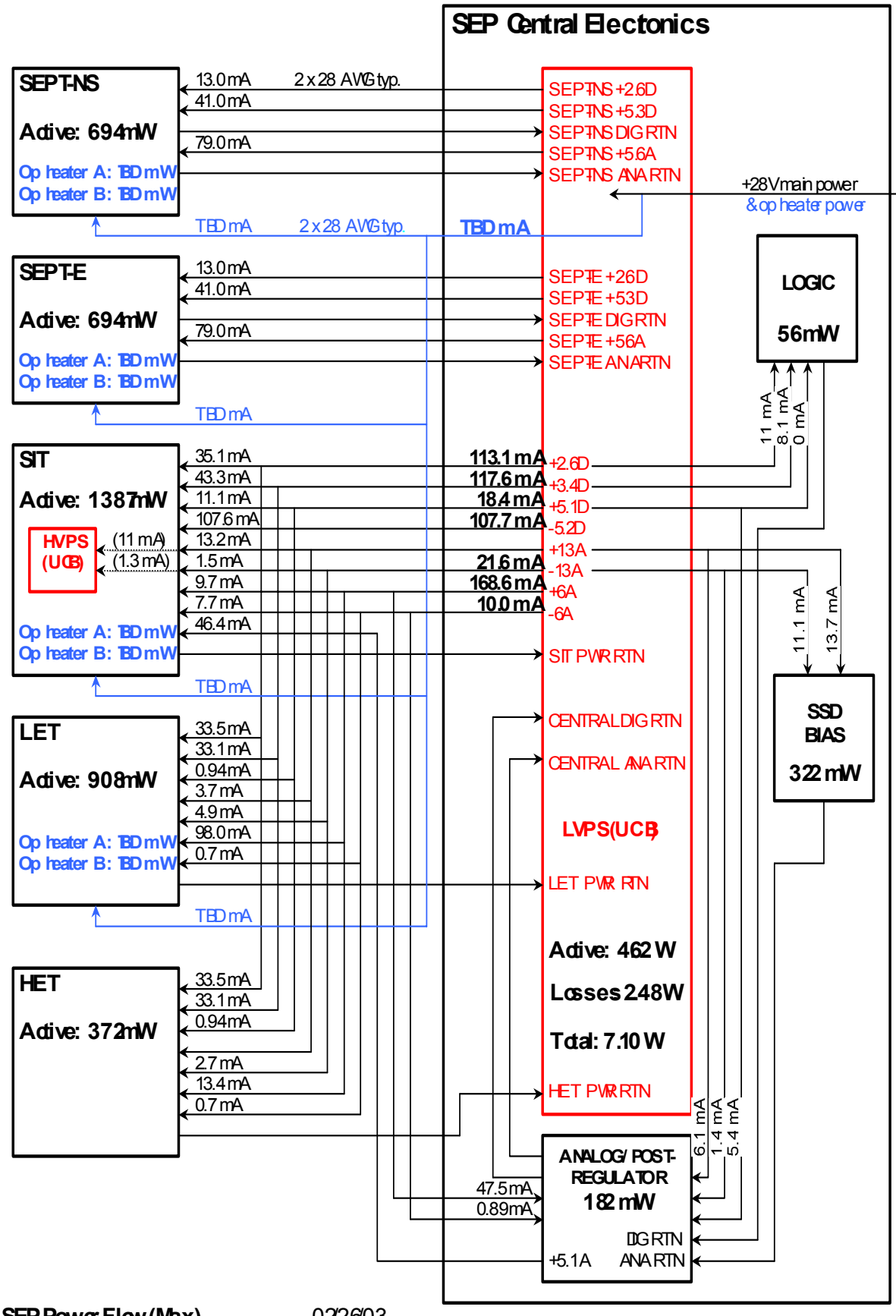


	Watts	CAPACITANCE
	0.00	
	0.53	203 uF
	0.28	195 uF
	1.01	224 uF
	0.06	81 uF
	0.56	6 uF
	0.09	187 uF
	0.40	281 uF
	0.29	152 uF
	0.03	11 uF
	0.22	12 uF
	0.44	50 uF
	0.03	11 uF
	0.22	12 uF
	0.44	50 uF
	4.61 Watts	



SEP Power Flow (Min. = Nom.) 02/26/03

Figure 2-1a SEP Power Flow Diagram, Min/Nominal



SEP Power Flow (Max) 02/26/03

Figure 2-1b SEP Power Flow Diagram, MAX

SEP minimum (nominal) power per voltage line

2/26/2003

Consum. Volt. [V]	Comment	SEPT [mA]	SEPT [mW]	SIT [mA]	SIT [mW]	LET [mA]	LET [mW]	HET [mA]	HET [mW]	Central [mA]	Central [mW]	SEP total [mA]	SEP total [mW]	LVPS output [V]
+2.6	Digital-NS	11.0	**29**									11.0	**29**	**+2.6**
+5.3	Digital-NS	19.0	**101**							0.085	**0**	19.1	**101**	**+5.3**
+5.6	Analog-NS	79.0	**442**							0.085	**0**	79.1	**443**	**+5.6**
+2.6	Digital-E	11.0	**29**									11.0	**29**	**+2.6**
+5.3	Digital-E	19.0	**101**							0.085	**0**	19.1	**101**	**+5.3**
+5.6	Analog-E	79.0	**442**							0.085	**0**	79.1	**443**	**+5.6**
+2.6	Digital			23.0	**60**	13.1	**34**	13.1	**34**	11.0	**29**	60.2	**157**	**+2.6**
+3.4	Digital			29.3	**100**	15.9	**54**	15.9	**54**	8.1	**28**	69.2	**235**	**+3.4**
+5.1	Digital			11.1	**57**	0.94	**5**	0.94	**5**	4.0	**20**	17.0	**87**	**+5.1**
-5.2	Digital			107.6	**560**					0.085	**0**	107.7	**560**	**-5.2**
+13	Analog			12.3	**160**	3.7	**48**	3.7	**48**	7.0	**91**	26.7	**347**	**+13**
-13	Analog			1.5	**20**	4.9	**64**	2.7	**35**	2.7	**35**	11.8	**153**	**-13**
+6	Analog			9.7	**58**	98.0	**588**	13.4	**80**	47.2	**283**	168.3	**1010**	**+6**
-6	Analog			7.7	**46**	0.7	**4**	0.7	**4**	0.5	**3**	9.6	**58**	**-6**
Regulator **+5.1**	Analog			46.4	**237**	97.2	**496**	12.6	**64**					**From +6**
Instr. subtotal:			**1143**		**1296**		**797**		**261**		**255**		**3752**	
	One half:		571.7											
LVPS @ 65% efficiency:											**2020**		**2020**	
SEP total:											**2275**		**5772**	

SEP maximum power per voltage line

2/26/2003

Consum. Volt. [V]	Comment	SEPT [mA]	SEPT [mW]	SIT [mA]	SIT [mW]	LET [mA]	LET [mW]	HET [mA]	HET [mW]	Central [mA]	Central [mW]	SEP total [mA]	SEP total [mW]	LVPS output [V]
+2.6	Digital-NS	13.0	**34**									13.0	**34**	**+2.6**
+5.3	Digital-NS	41.0	**217**							0.085	**0**	41.1	**218**	**+5.3**
+5.6	Analog-NS	79.0	**442**							0.085	**0**	79.1	**443**	**+5.6**
+2.6	Digital-E	13.0	**34**									13.0	**34**	**+2.6**
+5.3	Digital-E	41.0	**217**							0.085	**0**	41.1	**218**	**+5.3**
+5.6	Analog-E	79.0	**442**							0.085	**0**	79.1	**443**	**+5.6**
+2.6	Digital			35.1	**91**	33.5	**87**	33.5	**87**	11.0	**29**	113.1	**294**	**+2.6**
+3.4	Digital			43.3	**147**	33.1	**112**	33.1	**112**	8.1	**28**	117.6	**400**	**+3.4**
+5.1	Digital			11.1	**57**	0.94	**5**	0.94	**5**	5.4	**28**	18.4	**94**	**+5.1**
-5.2	Digital			107.6	**560**					0.085	**0**	107.7	**560**	**-5.2**
+13	Analog			13.2	**172**	3.7	**48**	3.7	**48**	19.8	**257**	40.4	**525**	**+13**
-13	Analog			1.5	**20**	4.9	**64**	2.7	**35**	12.5	**162**	21.6	**281**	**-13**
+6	Analog			9.7	**58**	98.0	**588**	13.4	**80**	47.5	**285**	168.6	**1012**	**+6**
-6	Analog			7.7	**46**	0.7	**4**	0.7	**4**	0.9	**5**	10.0	**60**	**-6**
+5.1	Analog			46.4	**237**	97.2	**496**	12.6	**64**					**From +6**
Instr. subtotal:			**1387**		**1387**		**908**		**372**		**559**		**4614**	
	One half:		693.5											
LVPS @ 65% efficiency:											**2484**		**2484**	
SEP total:											**3044**		**7098**	

Figure 2-1c, SEP Min/Max Power Requirements

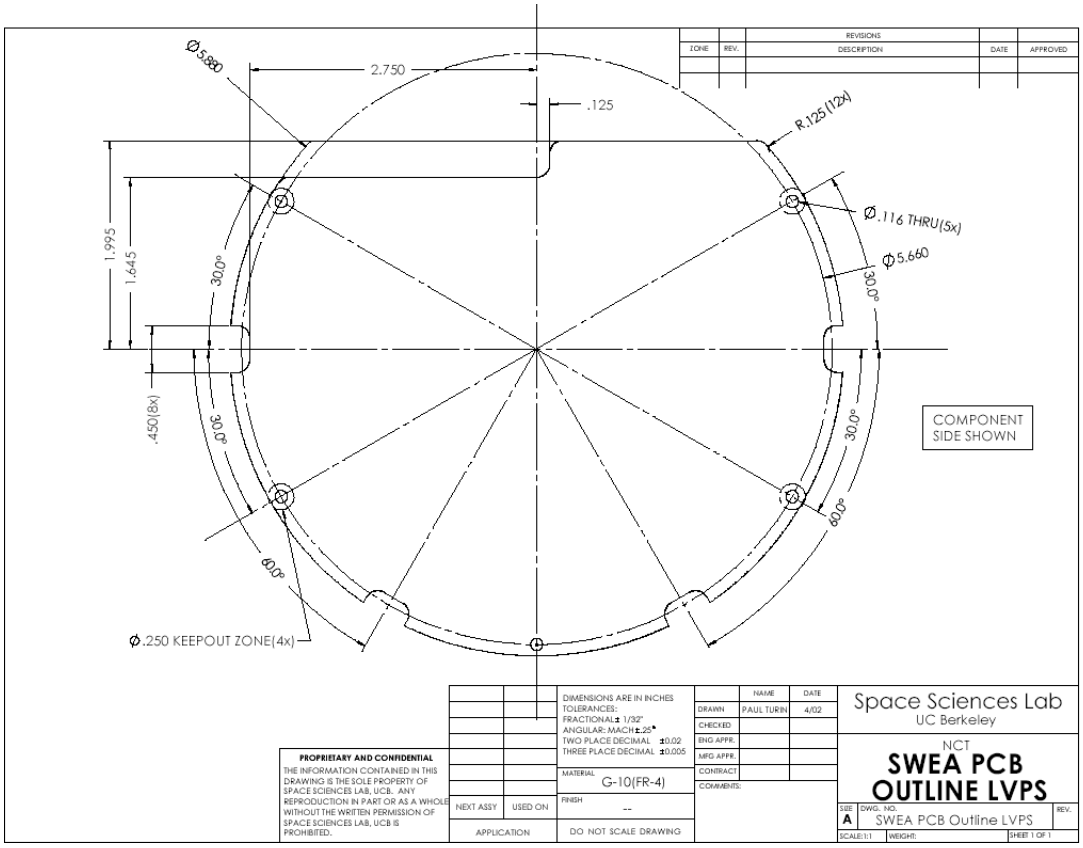


Figure 2-2 SWEA LVPS Form Factor

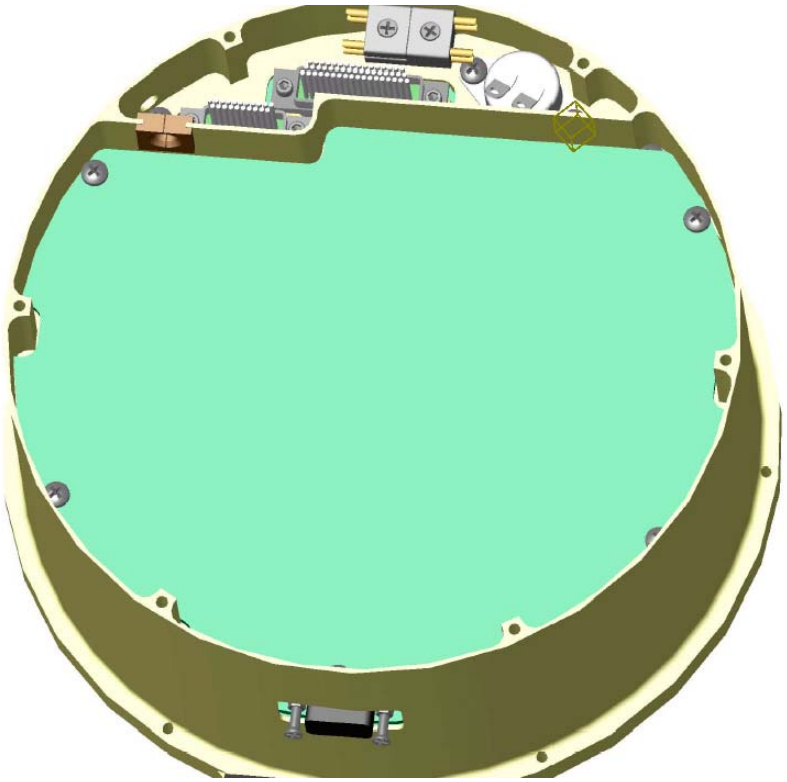


Figure 2-3 SWEA LVPS Form Factor

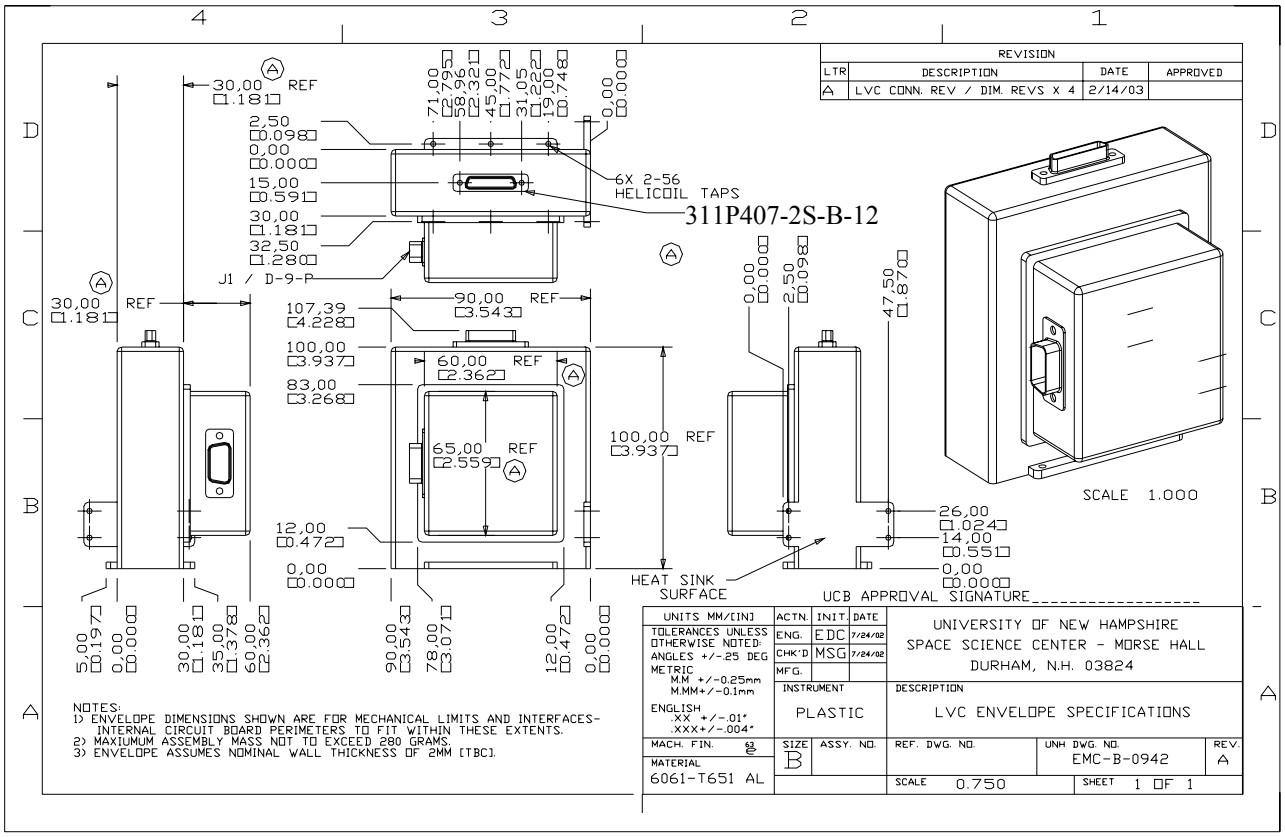


Figure 2-4, PLASTIC LVPS Form Factor

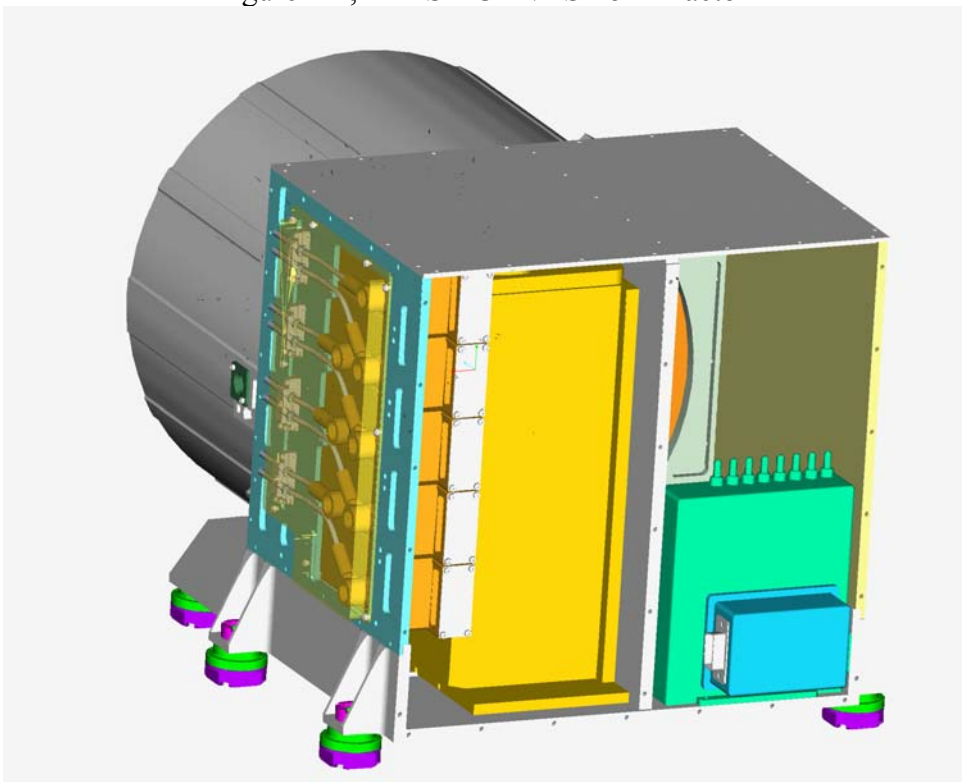


Figure 2-5, PLASTIC LVPS shown in PLASTIC

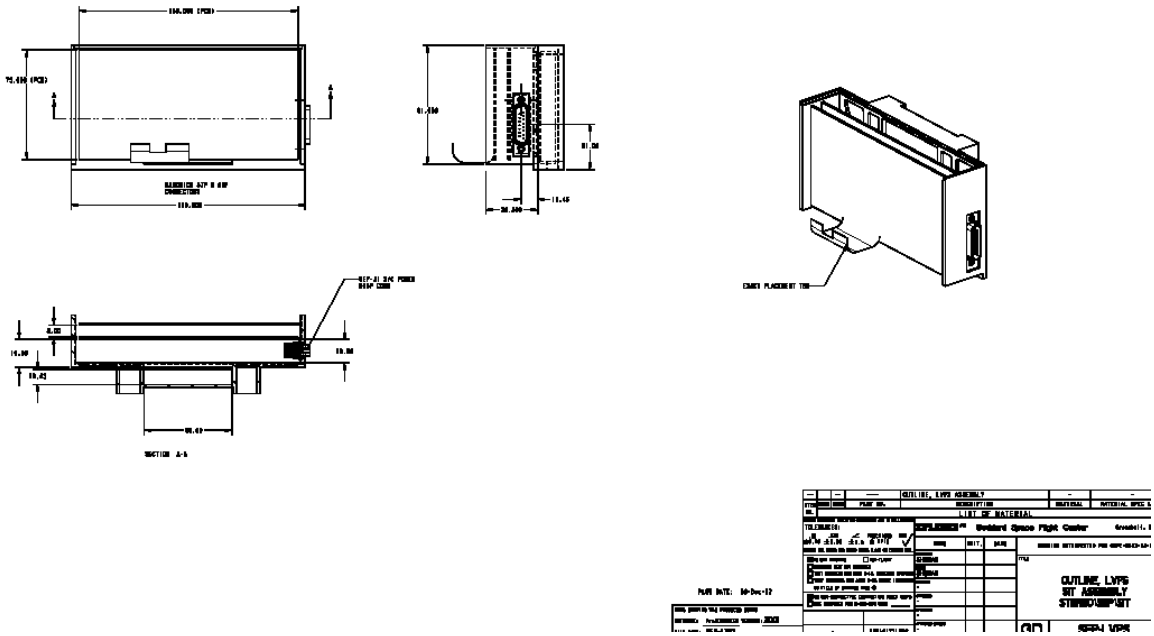


Figure 2-6 SEP LVPS form factor

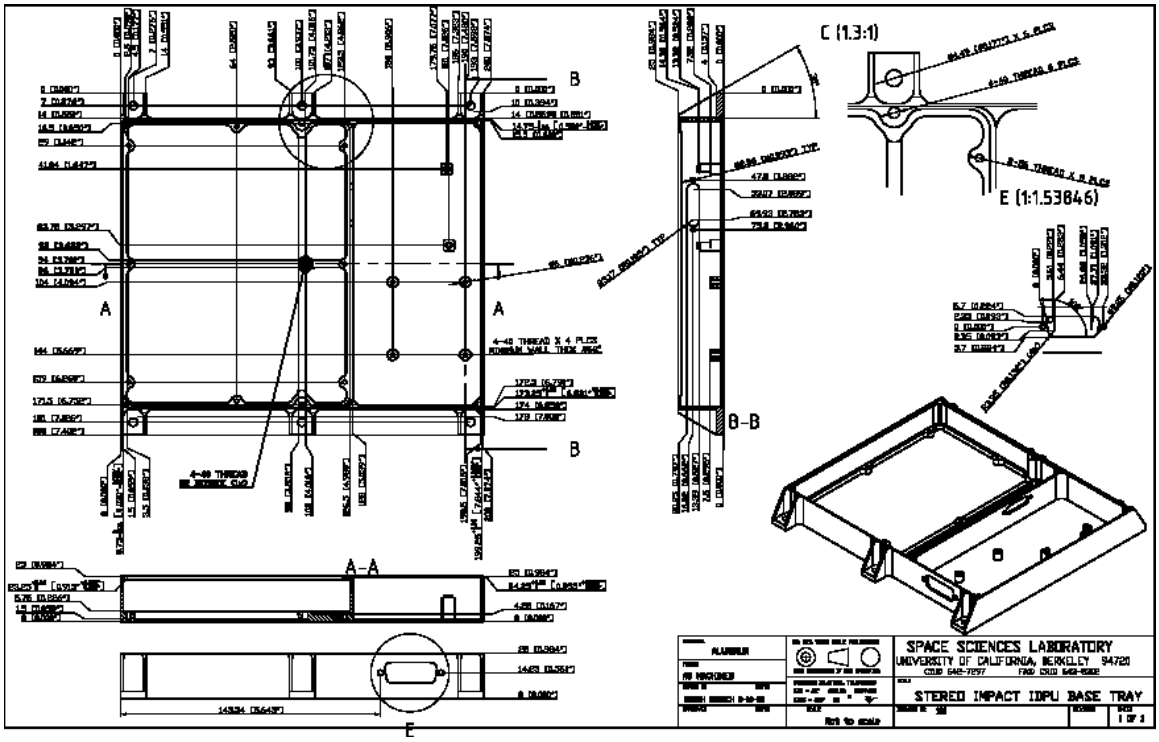


Figure 2-7 IDPU LVPS Form Factor

Airborn M83513/04-C11N (on a pig-tail attached to the LVPS)

Pin	Signal
17	STE Bias Return
16	STE Bias (140V)
7,8	Digital Ground
14	VCC_A (2.5V)
6	+5VD
13,15,9,19	Analog Ground
20	+5.1VA
18	-5.1VA
10	+12.1VA
21	-12.1VA
5	+28V (secondary)
1	+28V primary
11	+28V primary Return
12	SWEA Temp Sensor
3	SWEA Temp Sensor Return
2	+28V Heater
4	+28V Heater Return

Note: Pins 2,3,4,12 do not route to the LVPS. They go from the DAC board to a Winchester connector mounted to the chassis outside the LVPS

Figure 2-8 SWEA LVPS Connector Pinout

SEP LVPS connectors 2/11/2003

Internal to SEP
SEP-P19A
LVPS output

1	SEPT-NS ANA RTN	52	HET +13A
2	SEPT-NS ANA RTN	53	HET +6A
3	SEPT-NS +5.6A	54	HET +6A
4	SEPT-NS +5.6A	55	HET -6A
5	Spare	56	HET -6A
6	Spare	57	HET -13A
7	SEPT-NS DIG RTN	58	HET -13A
8	SEPT-NS DIG RTN	59	HET +2.6D
9	SEPT-NS +2.6D	60	HET +2.6D
10	SEPT-NS +2.6D	61	HET +3.4D
11	SEPT-NS +5.3D	62	HET +3.4D
12	SEPT-NS +5.3D	63	HET +5.1D
13	SEPT-NS SEP STAR	64	HET +5.1D
14	SEPT-NS SEP STAR	65	Spare
15	SEPT-E ANA RTN		
16	SEPT-E ANA RTN		
17	SEPT-E +5.6A		
18	SEPT-E +5.6A		
19	Spare		
20	Spare		
21	SEPT-E DIG RTN		
22	SEPT-E DIG RTN		
23	SEPT-E +2.6D		
24	SEPT-E +2.6D		
25	SEPT-E +5.3D		
26	SEPT-E +5.3D		
27	SEPT-E SEP STAR		
28	SEPT-E SEP STAR		
29	SIT PWR RTN		
30	SIT PWR RTN		
31	SIT +13A		
32	SIT +13A		
33	SIT +6A		
34	SIT +6A		
35	Spare		
36	Spare		
37	SIT -6A		
38	SIT -6A		
39	SIT -13A		
40	SIT -13A		
41	SIT -5.2D		
42	SIT -5.2D		
43	SIT +2.6D		
44	SIT +2.6D		
45	SIT +3.4D		
46	SIT +3.4D		
47	SIT +5.1D		
48	SIT +5.1D		
49	HET PWR RTN		
50	HET PWR RTN		
51	HET +13A		

External to SEP
SEP-J1
S/C power & heaters

1	Spare		
2	+28V MAIN/OP HTR		
3	+28V MAIN/OP HTR		
4	Spare		
5	+28V SURV HTR		
6	+28V SURV HTR		
7	Spare		
8	CHASSIS		
9	Spare		
10	+28V MAIN/OP HTR RTN		
11	+28V MAIN/OP HTR RTN		
12	Spare		
13	+28V SURV HTR RTN		
14	+28V SURV HTR RTN		
15	Spare		

SEP-P19A Nanonics P/N:
EM STM065C6N
Flight 94036CD065002SE2
65-pin, TH, horizontal plug, located on flex

SEP-P19B Nanonics P/N:
EM STM051C6N
Flight 94036CD051002SE2
51-pin, TH, horizontal plug, located on flex

Internal to SEP
SEP-P19B
LVPS output

1	LET PWR RTN	52	+28V SURV HTR RTN
2	LET PWR RTN	53	+28V SURV HTR RTN
3	LET +13A	54	+28V SURV HTR
4	LET +13A	55	+28V SURV HTR
5	LET +6A	56	+28V OP HTR
6	LET +6A	57	+28V OP HTR
7	LET -6A	58	+28V OP HTR RTN
8	LET -6A	59	+28V OP HTR RTN
9	LET -13A		
10	LET -13A		
11	LET +2.6D		
12	LET +2.6D		
13	LET +3.4D		
14	LET +3.4D		
15	LET +5.1D		
16	LET +5.1D		
17	Spare		
18	CENTRAL DIG RTN		
19	CENTRAL DIG RTN		
20	CENTRAL +2.6D		
21	CENTRAL +2.6D		
22	CENTRAL +3.4D		
23	CENTRAL +3.4D		
24	CENTRAL +5.1D		
25	CENTRAL +5.1D		
26	CENTRAL ANA RTN		
27	CENTRAL ANA RTN		
28	CENTRAL ANA RTN		
29	CENTRAL ANA RTN		
30	CENTRAL +13A		
31	CENTRAL +13A		
32	CENTRAL +6A		
33	CENTRAL +6A		
34	CENTRAL -6A		
35	CENTRAL -6A		
36	CENTRAL -13A		
37	CENTRAL -13A		
38	LVPS TEMP SENSOR		
39	Spare		
40	Spare		
41	Spare		
42	Spare		
43	Spare		
44	+28V SURV HTR RTN		
45	+28V SURV HTR RTN		
46	+28V SURV HTR		
47	+28V SURV HTR		
48	+28V OP HTR		
49	+28V OP HTR		
50	+28V OP HTR RTN		
51	+28V OP HTR RTN		

Figure 2-9 SEP LVPS Connector pinouts

Low Voltage Convertor Pin Assignment

Pin #	Assignment
9	+12V
18	+12V
26	+12V
8	-12V
17	-12V
25	-12V
7	+5.5V
16	+5.5V
24	+5.5V
6	-5.5V
15	-5.5V
23	-5.5V
5	+2.5V_A
14	+2.5V_A
22	+2.5V_A
4	+2.5V_B
13	+2.5V_B
21	+2.5V_B
1	AGND
2	AGND
3	AGND
10	AGND
11	AGND
12	AGND
19	AGND
20	AGND

Part
HD26S on LVPS
311P407-2S-B-12

Figure 2-10 PLASTIC LVPS pinout (output).

PLASTIC Low Voltage Converter
Input Connector Pinout

Pin #	Assignment
1	spare
2	28V Primary
3	28V Redundant
4	spare
5	spare
6	spare
7	28V Return Primary
8	28V Return Redundant
9	Chassis

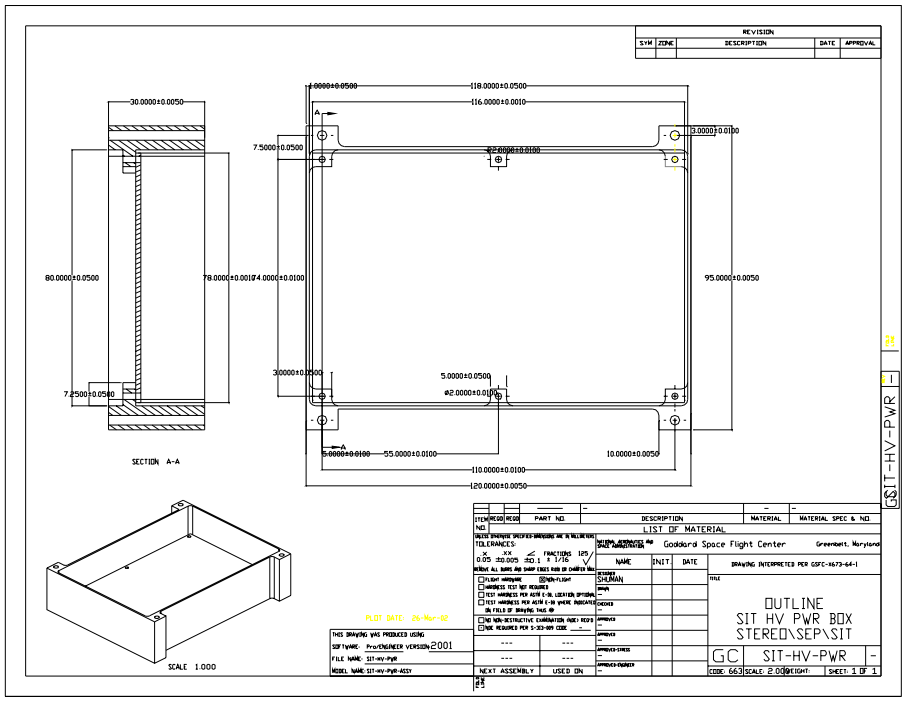
Part
D9P on LVPS
311P409-1P-B-12

Figure 2-11 PLASTIC LVPS pinout (input)

3. SIT HVPS Requirements

The SIT HVPS is part of the SIT instrument. It takes secondary +/-12V and generates a programmable output voltage at up to +3500V plus a number of proportional taps. This supply provides no ground isolation, and does not need to meet the conducted EMC requirements of reference 1. Detailed electrical requirements are described in reference 5.

3.1. *Form Factor*



3.2. *Connectors*

The input connector is described in reference 5. The output shall be un-terminated wires which shall be terminated in the SIT instrument. The wires must be shielded in a continuous fashion between the boxes providing no gap.