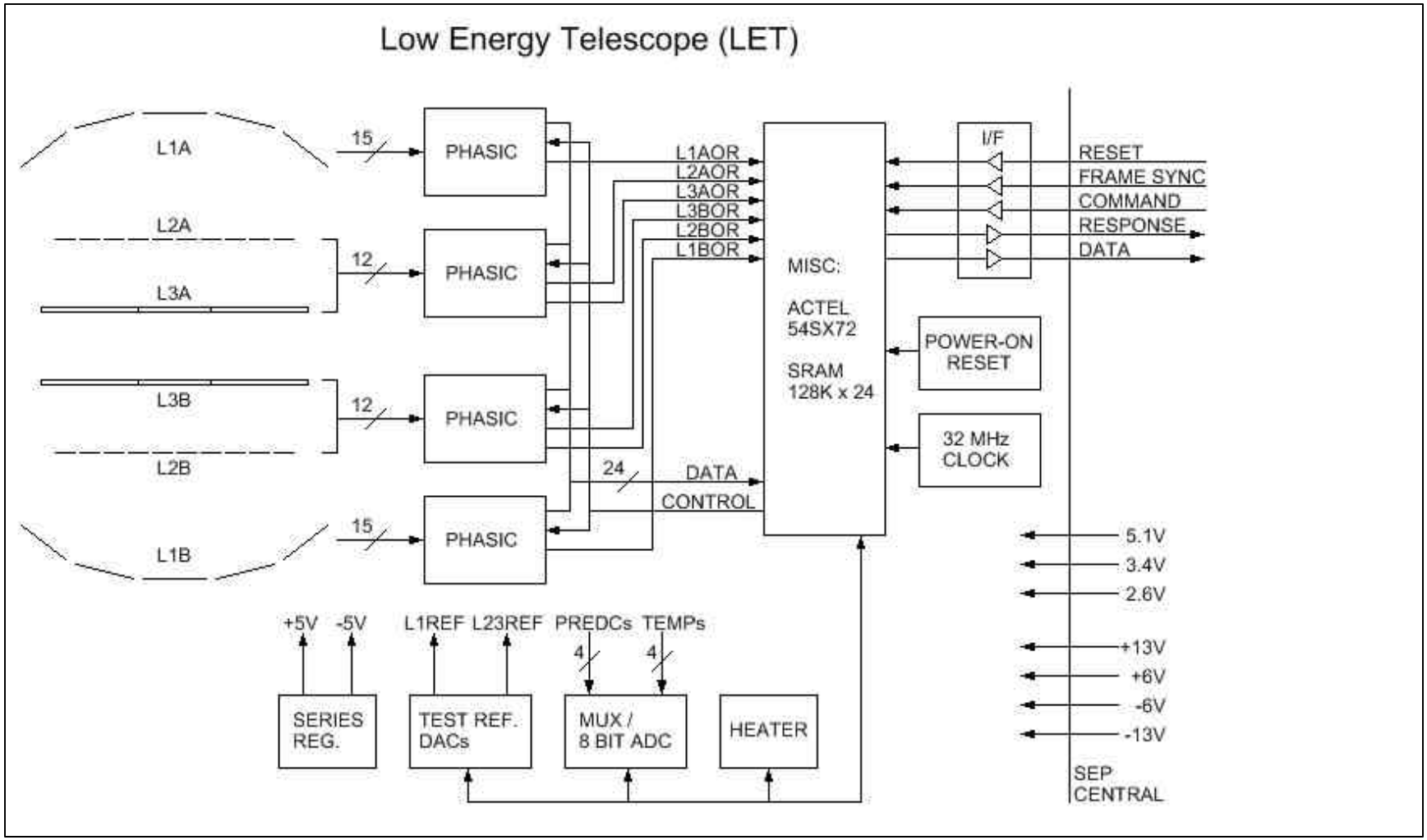
LET Electronics

Rick Cook
wrc@srl.caltech.edu
626-395-4263


Low Energy Telescope (LET)
L1A
L2A
L3A
L3B
L2B
L1B
15
12
12
15
PHASIC
PHASIC
PHASIC
PHASIC
L1AOR
L2AOR
L3AOR
L3BOR
L2BOR
L1BOR
24
DATA
CONTROL
MISC:
ACTEL
54SX72
SRAM
128K x 24
I/F
RESET
FRAME SYNC
COMMAND
RESPONSE
DATA
POWER-ON
RESET
32 MHz
CLOCK
5.1V
3.4V
2.6V
+13V
+6V
-6V
-13V
SEP
CENTRAL
+5V
-5V
L1REF
L23REF
PREDCs
TEMPs
4
4
SERIES
REG.
TEST REF.
DACs
MUX /
8 BIT ADC
HEATER

Interfaces to S/C and SEP Central Electronics

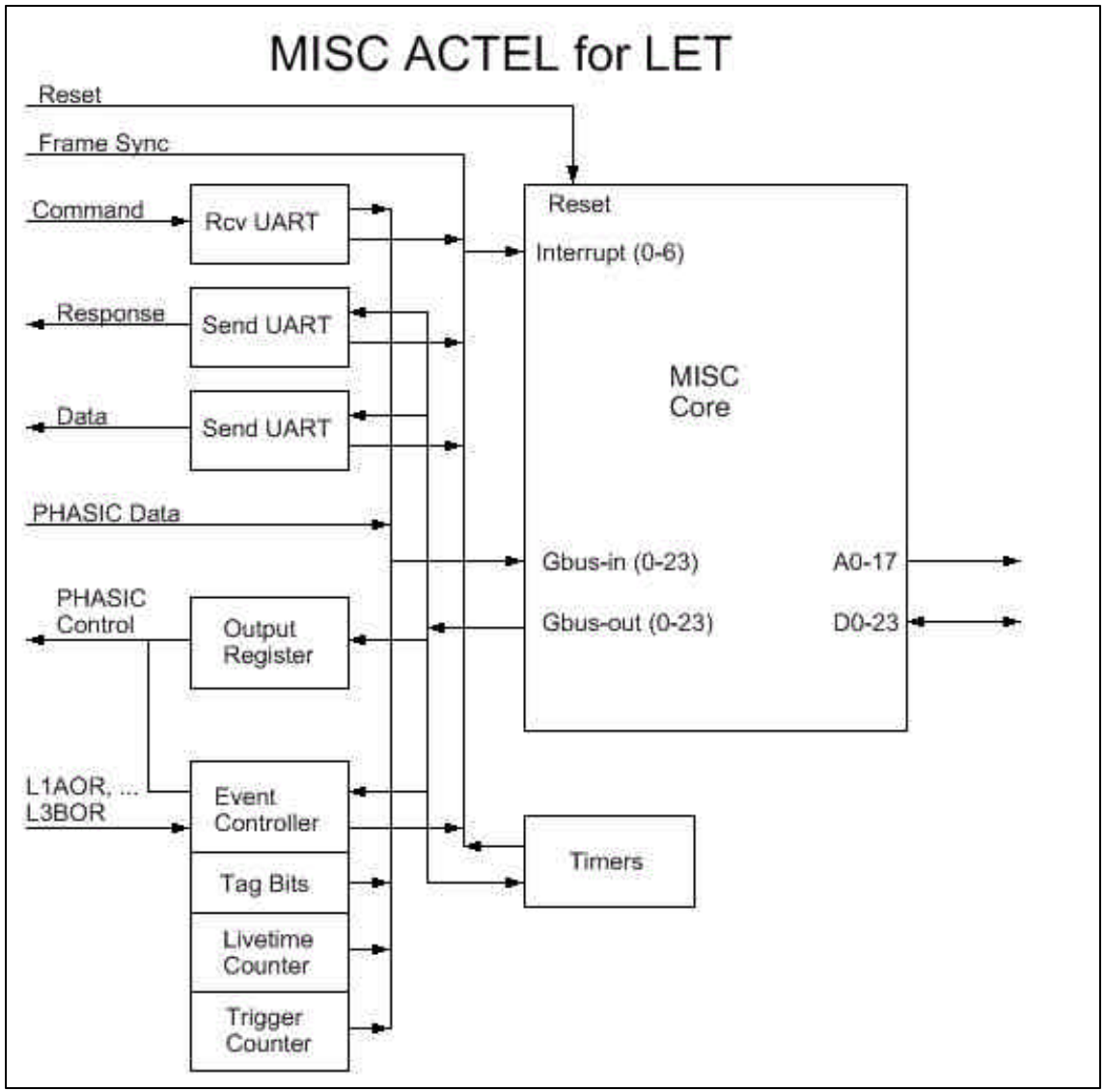
- **Electrical**
  - Main & operational/survival heater power from SEP Central.
  - S/C-monitored thermistor located inside box.
  - Conductively coupled to SEP Central box via support bracket.
  - Data/command link with SEP Central via serial interface.
- **Mechanical**
  - Mounted on a bracket for clear field of view.
- **Thermal**
  - Conductively coupled to SEP Central box via support bracket.
- **Purge**
  - Flow rate regulated by SEP Central manifold, 5 liters/hour.

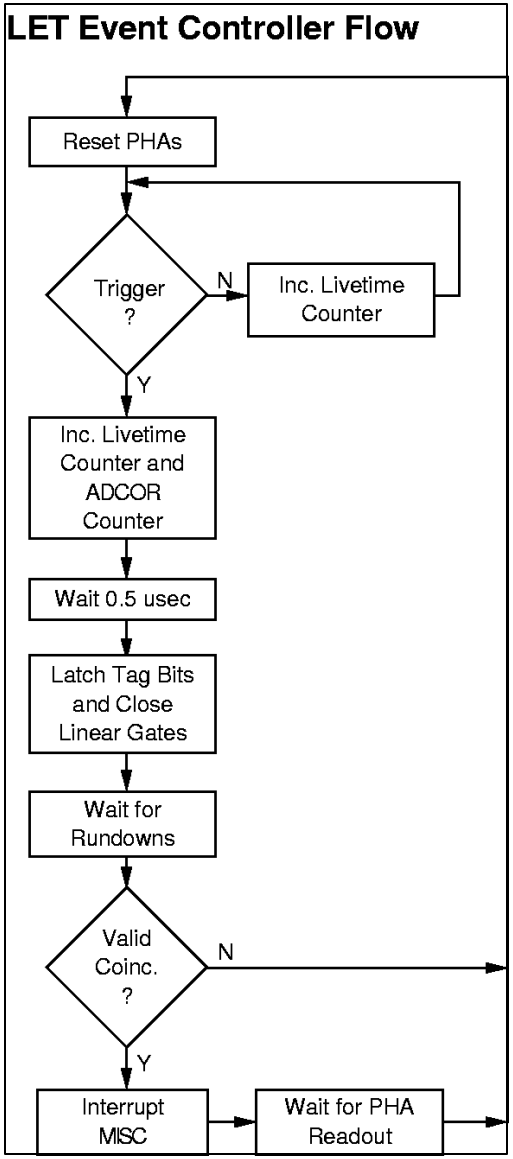
LET Electronics Packaging

- A single rigid-flex assembly contains all electronics.
- Assembly consists of two roughly circular rigid boards ("Front-end" and "Back-end") connected by a flexible ribbon.
- Connection to SEP-Central via flexible ribbon "pigtail" terminated with Nanonics connector.
- Front-end board supports 4 hybrids containing Caltech PHASIC chips, detector connector terminations, and passive detector connection networks.
- Back-end board contains everything else: MISC system, logic, reference voltage generator, series regulators, house-keeping ADC, test reference generation DACs, and heater.
- Packaging approach evolved from discussions with JPL experts with recent rigid-flex experience.
- Engineering board layouts, which will be the same as flight board layouts, are in progress.

MISC (Minimal Instruction Set Computer)

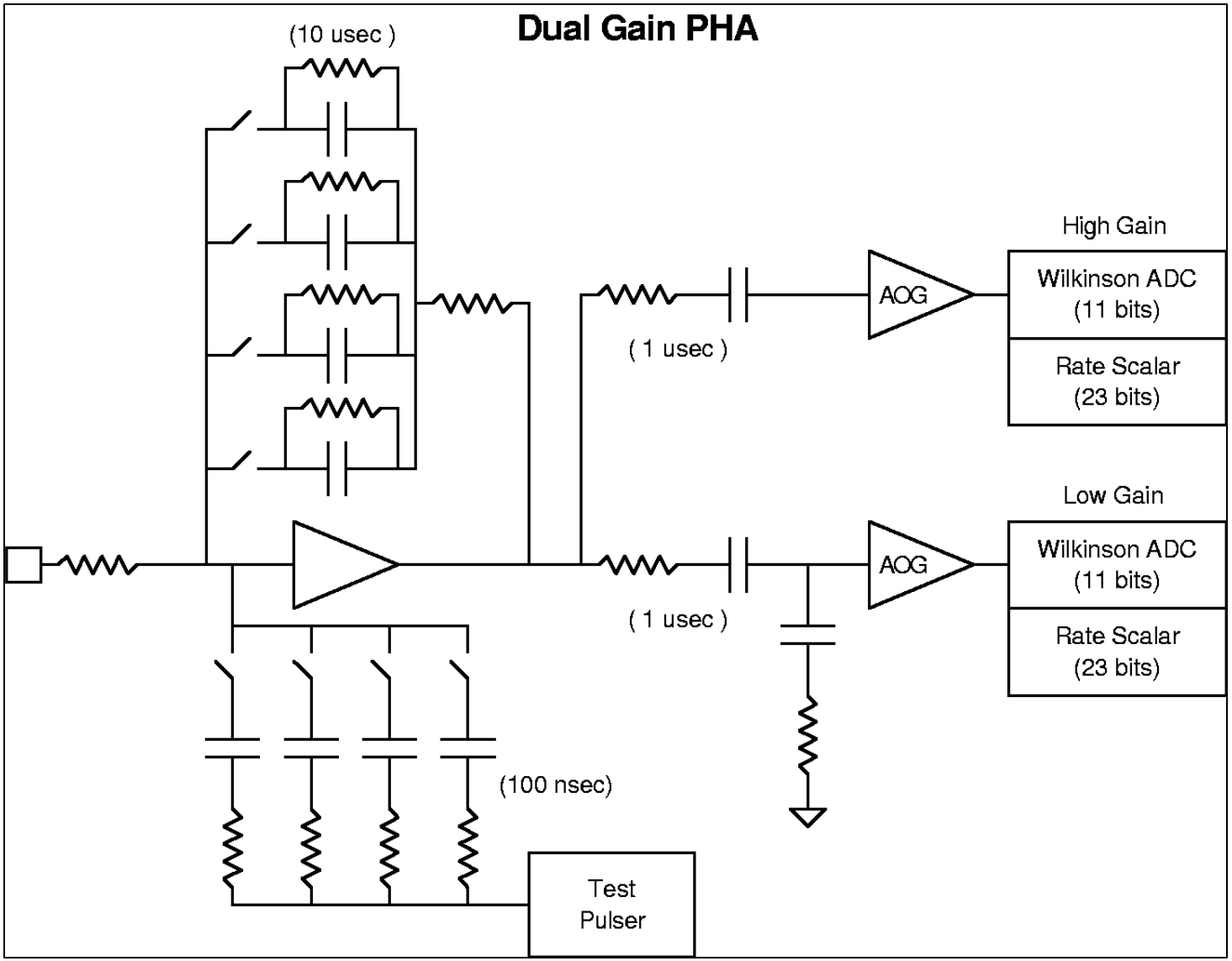
- Simple processor designed to embed within FPGA.
- Dual Stack architecture by Chuck Moore, designer of RTX2010 and inventor of FORTH.
- Adapted to small instrument controller needs at Caltech by inclusion of prioritized vectored interrupts and “G-bus” for I/O.
- Power/performance ratio improved over RTX2010 system.
- Implemented in ACTEL 54SX72, using about 75% of resources, leaving ample room for application specific logic.
- Core design stable since Feb. ‘01.
- Used in PHASIC chip tester and HEFT balloon program.
- Routing concern dissipated after successful routing of over 20 FPGAs with various application specific configurations.
- Tested VHDL definition available from Bob Baker at GSFC.
- User manual available from Rick Cook at Caltech.

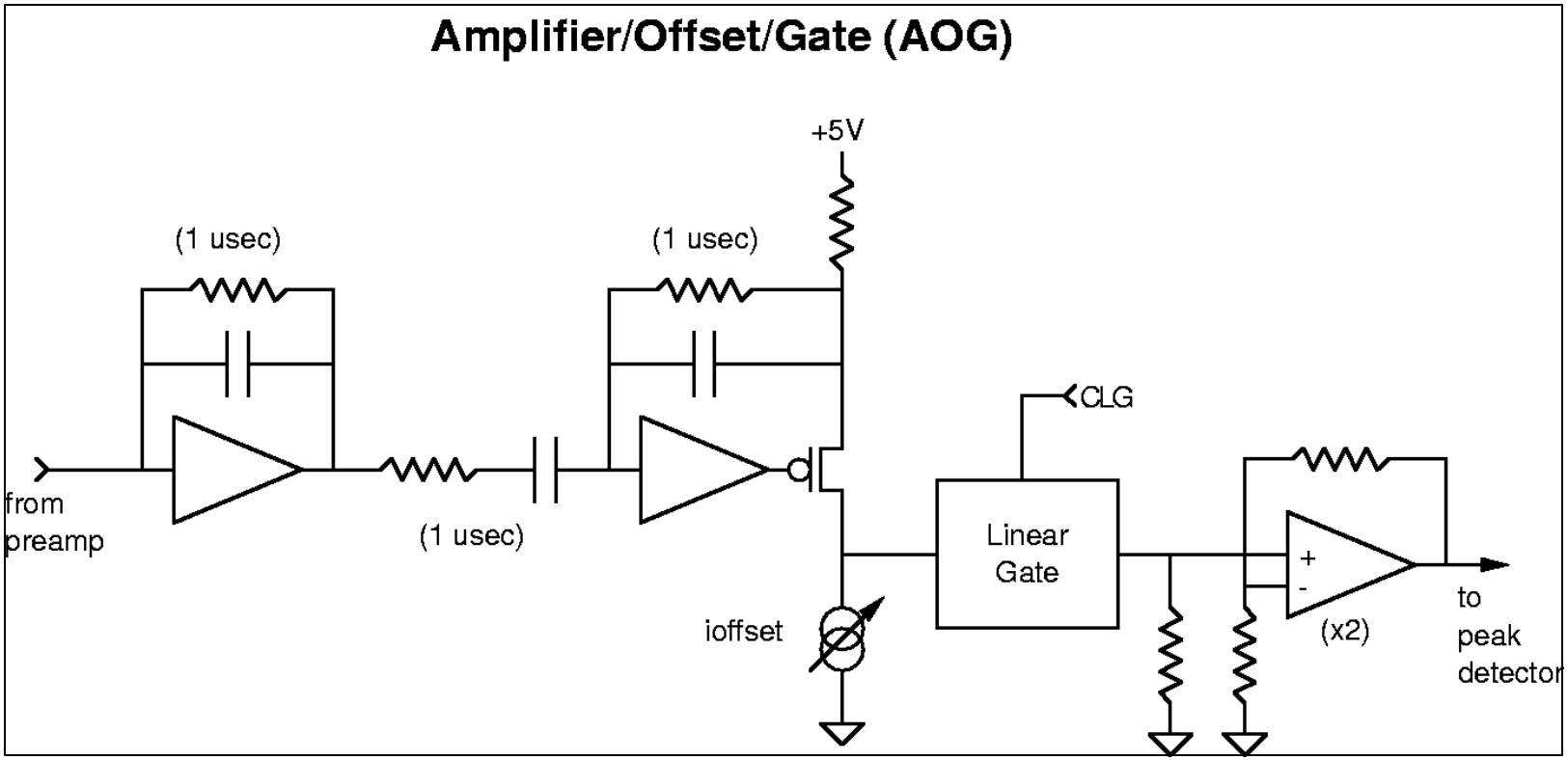

MISC ACTEL for LET
Reset
Frame Sync
Command
Rcv UART
Response
Send UART
Data
Send UART
PHASIC Data
PHASIC Control
Output Register
L1AOR, ... L3BOR
Event Controller
Tag Bits
Livetime Counter
Trigger Counter
Reset
Interrupt (0-6)
MISC Core
Gbus-in (0-23)
A0-17
Gbus-out (0-23)
D0-23
Timers

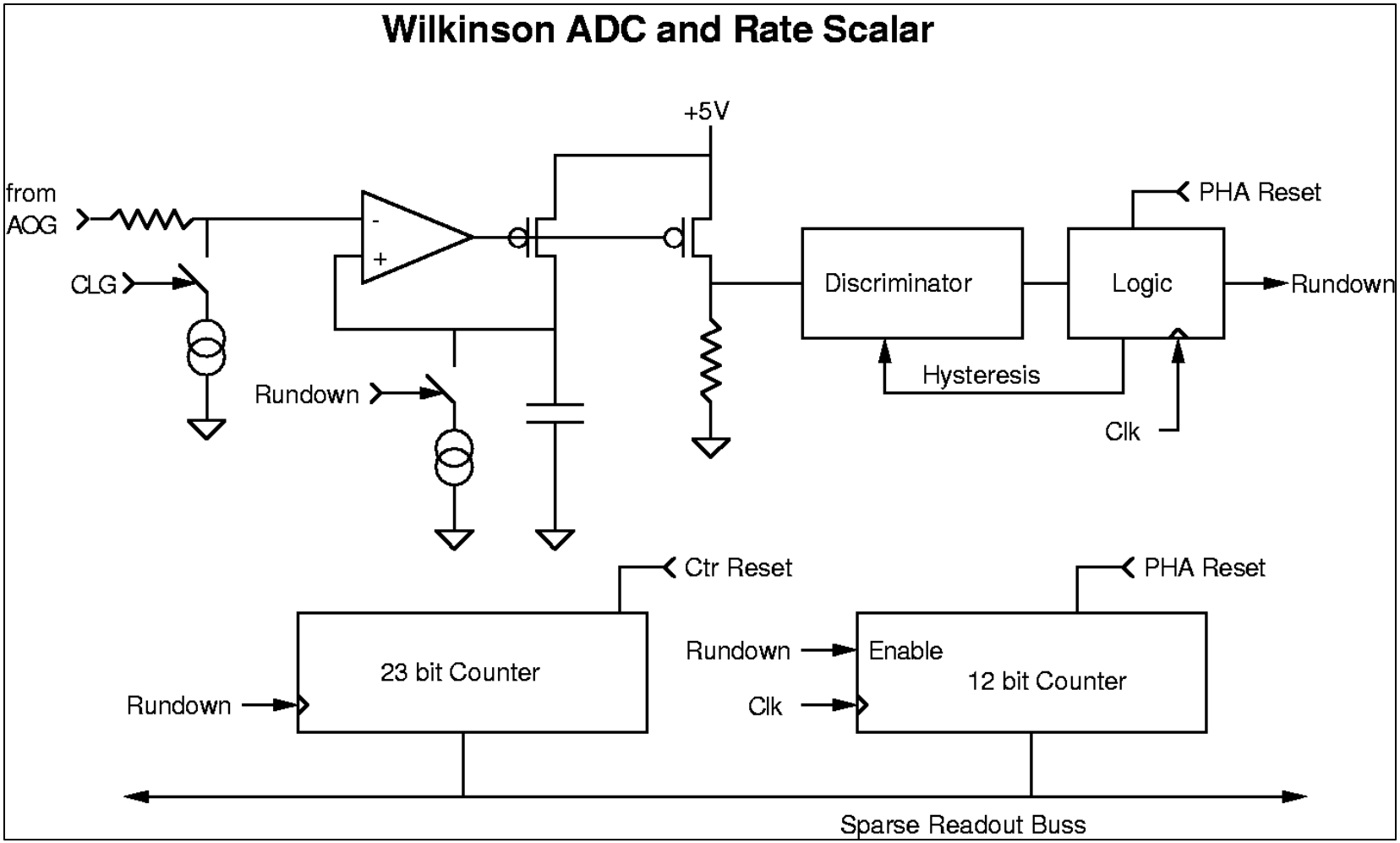

LET Event Controller Flow
Reset PHAs
Trigger ?
N
Inc. Livetime Counter
Y
Inc. Livetime Counter and ADCOR Counter
Wait 0.5 usec
Latch Tag Bits and Close Linear Gates
Wait for Rundowns
Valid Coinc. ?
N
Y
Interrupt MISC
Wait for PHA Readout

Caltech PHASIC (Pulse-Height Analysis System IC)

- **Complete front-end signal pulse processing for silicon detectors in LET and HET.**
- **Contains 16 dual-gain PHAs, each with:**
  - **Preamplifier configurable to various detector capacitances, signal amplitude ranges, and leakage currents.**
  - **Two (shaping amplifier-linear gate-11 bit Wilkinson ADC) chains, with combined dynamic range of 10,000 (full scale / threshold).**
  - **Programmable thresholds.**
  - **Bias switching to enable or disable power.**
  - **23-bit scalar for counting triggers.**
- **Architecture due to J. Howard Marshall III, with 30 years development/use in numerous space instruments.**
- **Evolved from ASIC developed for ACE:**
  - **Most components now on chip; dynamic range extended from 2000 to 10,000; Max ADC conversion time reduced from 256 to 64 usec; Power consumption reduced from 40 to 9 mW/PHA. Density increased.**


Dual Gain PHA
(10 usec)
(1 usec)
AOG
High Gain
Wilkinson ADC
(11 bits)
Rate Scalar
(23 bits)
(1 usec)
AOG
Low Gain
Wilkinson ADC
(11 bits)
Rate Scalar
(23 bits)
(100 nsec)
Test
Pulser

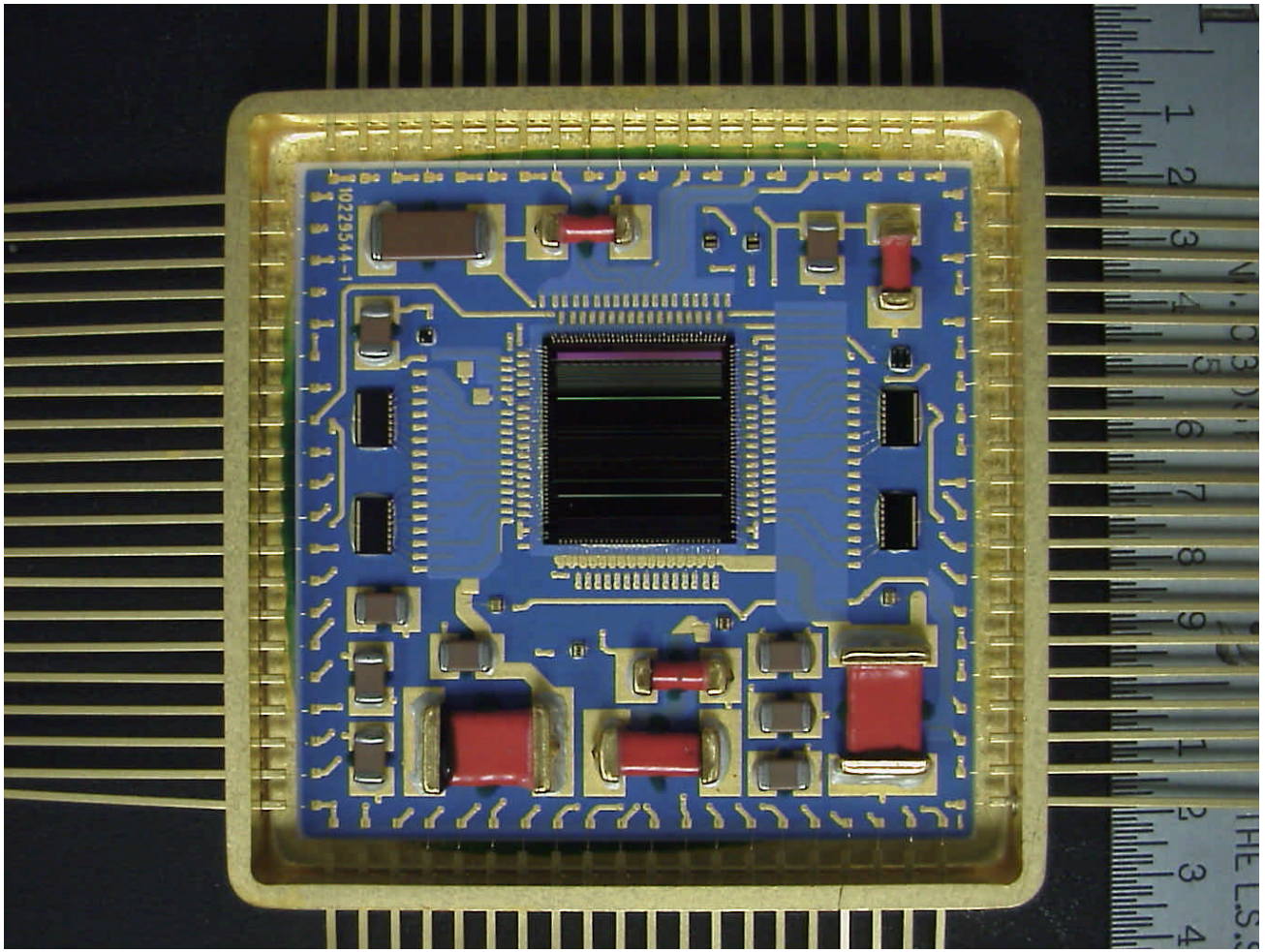

Amplifier/Offset/Gate (AOG)
+5V
(1 usec)
(1 usec)
(1 usec)
CLG
from
preamp
Linear
Gate
+
-
(x2)
to
peak
detector
ioffset


Wilkinson ADC and Rate Scalar
+5V
from
AOG
CLG
Rundown
Discriminator
Logic
PHA Reset
Rundown
Hysteresis
Clk
Ctr Reset
PHA Reset
23 bit Counter
Rundown
Rundown
Enable
12 bit Counter
Clk
Sparse Readout Buss

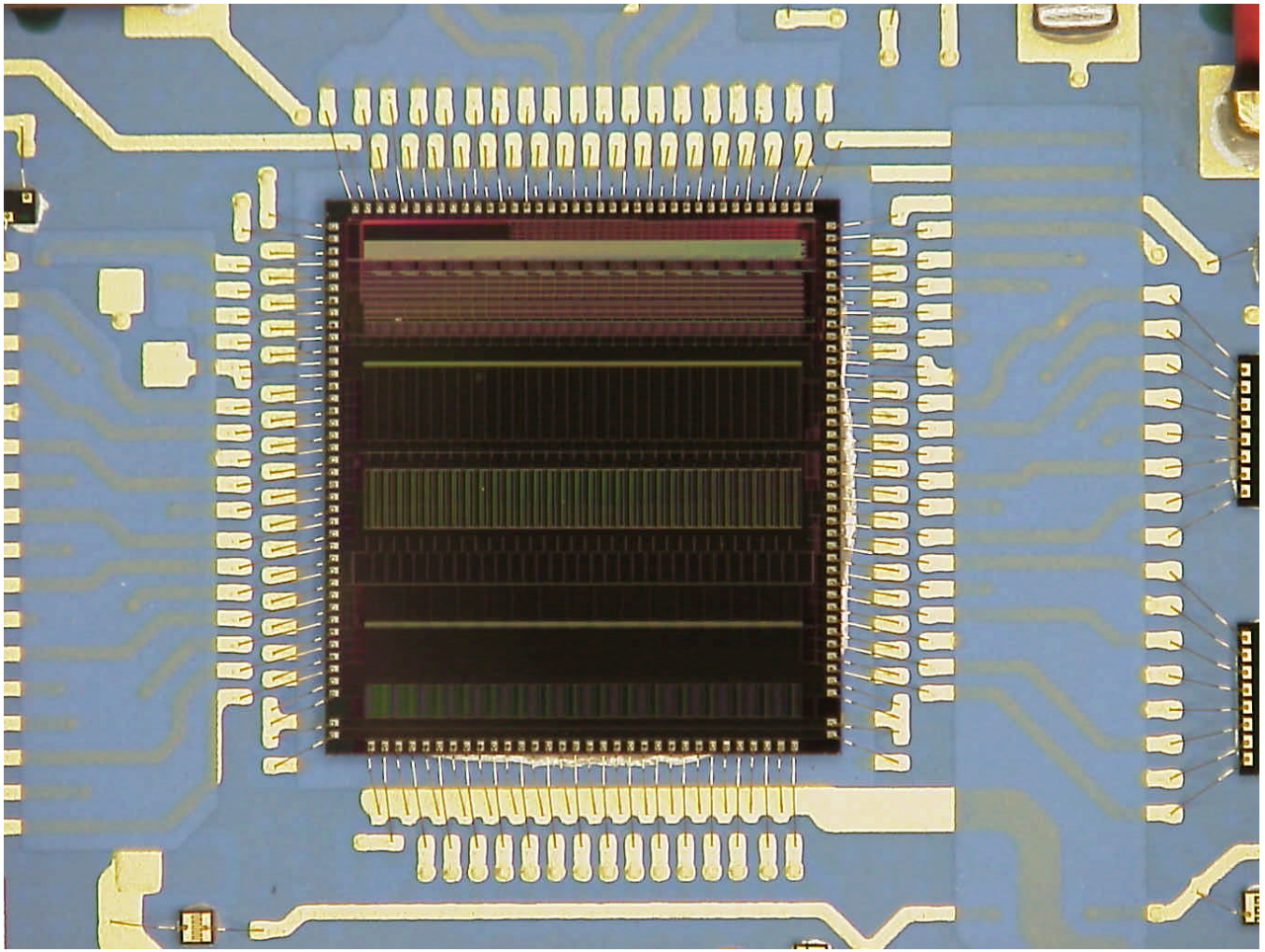
VLSI Development Status

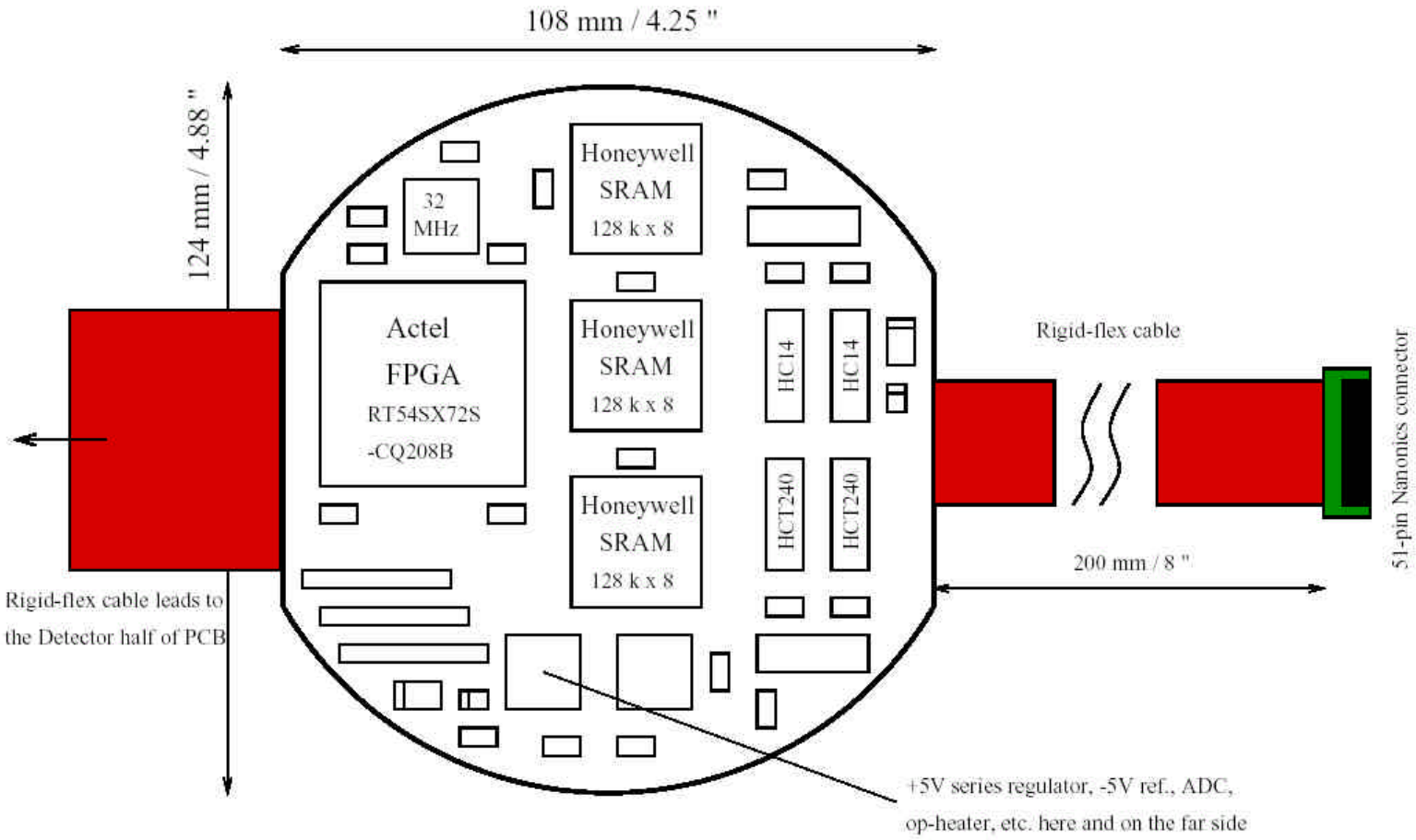
- **Full Flight Chip (PHASIC) fabricated at AMIS.**
  - **Functional, but glitch at linear gate re-opening necessitated re-spin.**
  - **Chip-level tester shipped from Caltech to GSFC, March 2002.**
  - **Linearity, noise, and dynamic range as expected, cross-talk adequately low.**
- **Latch-up testing performed with Aerospace Corp. help shows no latch-up through 80 MeV/(mg/cm2).**
- **Total dose testing at Aerospace shows tolerance through 12 krad, failure at 20 krad. Will repeat with re-spin parts to assess spot shielding needs.**
- **Will not need to exercise UTMC radiation hardening option.**
- **Re-spin submission occurred two weeks ahead of schedule in late Sep. 2002. Expect flight die in Dec. 2002.**
- **First hybrid containing PHASIC chip tested and functional.**

Hybrid Containing Caltech PHASIC Chip



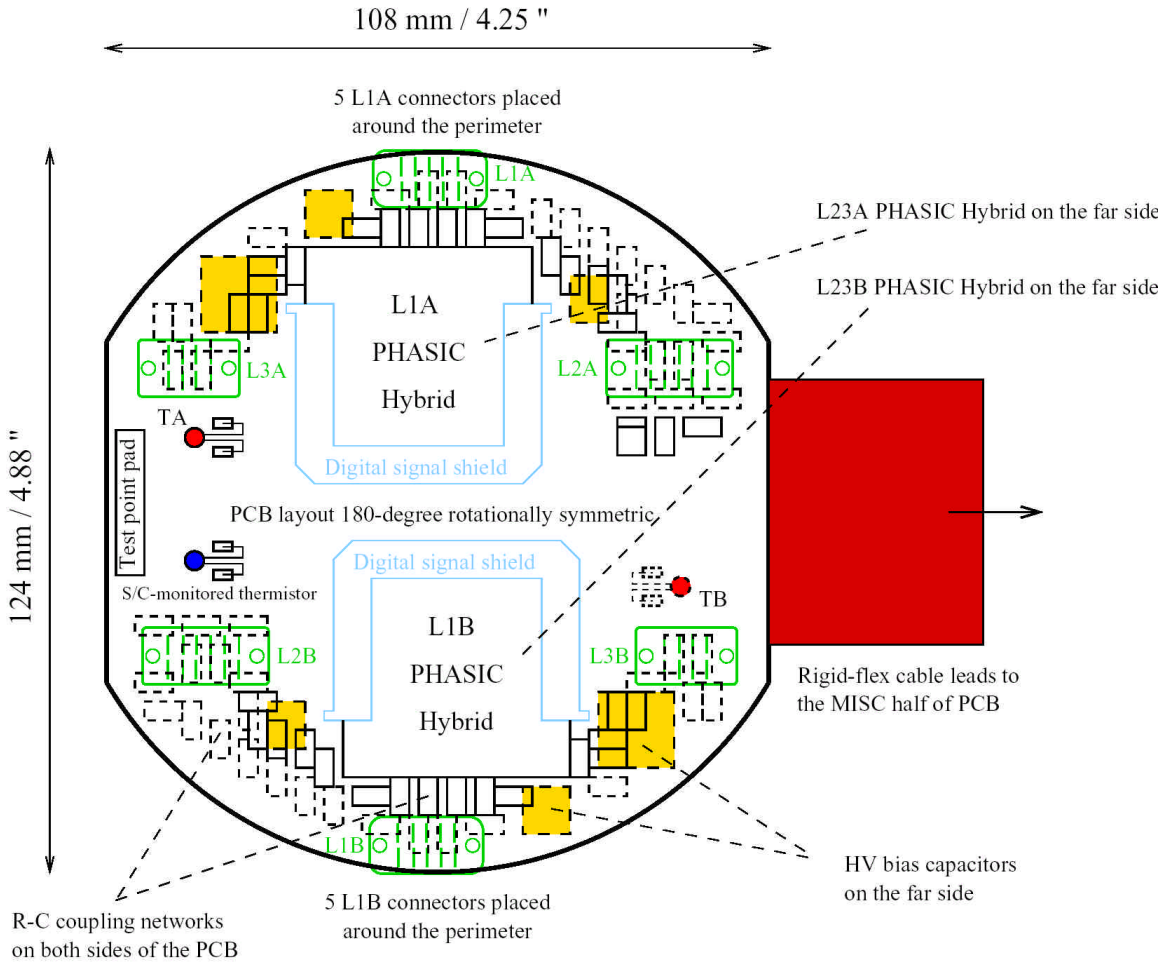
Caltech PHASIC Chip





LET Board Layout Assessment - MISC Half

BK 11/6/02



LET Board Layout Assessment - Detector Half

BK 11/11/02

LET resources: 11/12/02

	PDR	CDR
Mass [g]		
LET det. & housing	515	565
LET electronics	235	306
----------	------	------
Total:	**750**	**871**
Power [mW]		
PHASIC hybrids	486	486
+5V reg, -5V ref, etc.	N/A	217
HK ADC	65	6
MISC @ 8 MHz	223	230
----------	------	------
Total:	**774**	**939**
Data rate [bit/s]		
Science	348	556.8
Housekeeping	N/A	0.5
Beacon	N/A	6.1
----------	------	------
Total:	**348**	**563**

Parts/Materials Status

- **Parts**
  - Parts list delivered & approved
  - Complying with GSFC-311-INST grade 2 requirements
  - Monitoring GIDEP alerts
  - Actel RT54SX72S procured via Project common buy
  - Other long lead-time EEE parts on order/in stock
  - Parts for PHASIC hybrid stored in dry nitrogen at JPL
  - Found HV capacitor substitute for discontinued ACE vendor
  - Using custom ACE database for parts inventory and kitting

- **Materials**
  - Materials and Processes list delivered & undergoing review
  - Using JPL D-8208 material selection guidelines
  - Consulting with Project & JPL contamination control engineers

Transportation Issues

- **Container properties**
  - Custom design, metal construction
  - Built-in shock absorbers
  - Hermetically sealed
  - Purge & vent ports with manual control
- **In transit**
  - Use double bag inside container and both bag and container backfilled with dry nitrogen
  - In a sealed container OK without purge for ~24 hours
  - Buy container an economy-class ticket on airline
  - Concerned about getting through airport security
- **ESD & contamination control**
  - Load/unload the container on ESD-safe clean bench
  - Apply double-bagging and extra purge at testing sites

SEP Central Electronics

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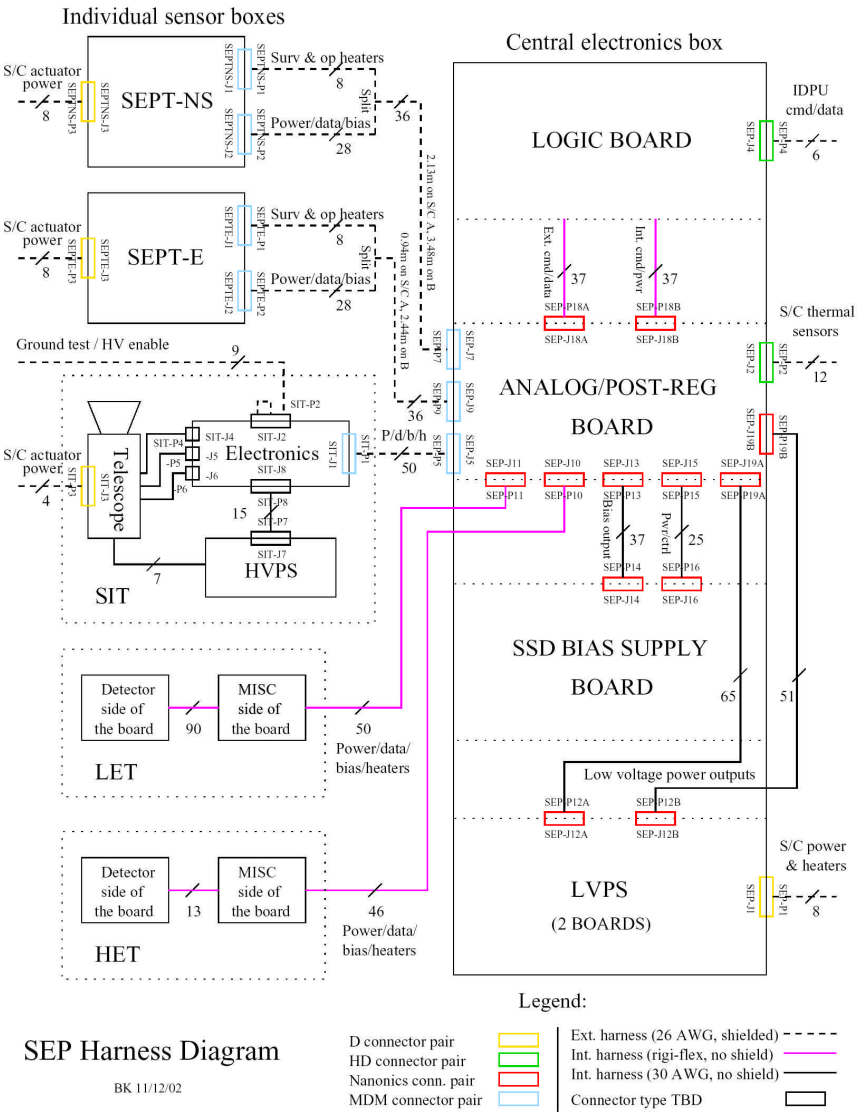
STEREO SEP Block Diagram



Interfaces to S/C

- **Electrical**
  - Main & operational/survival heater power from S/C
  - S/C-monitored thermistor located inside box
  - Connected to S/C chassis via conductive strap, material TBD
- **Mechanical**
  - Mounted directly to S/C
  - Supports LET on a bracket and HET
  - Houses HET board, LVPS, SSD Bias Supply, Logic board, and Analog/Post-Reg board
- **Thermal**
  - Mounted to S/C via non-conductive bushings, material TBD
- **Purge**
  - One swage lock connector for SIT/HET/LET (various flow rates)

Low Voltage Power Supply 11/12/02

- Design and fabrication by UC Berkeley.
- Voltage & load requirements defined.
- Outputs include:
  - +2.6V, +3.4V, +5.1V, +5.3V, -5.2V (digital)
  - +5.6V, +6V, -6V, +13V, -13V (analog)
- Connector type and size selected. Pin assignments defined.

SEP LVPS Voltage & Nominal Loads [mW] 11/12/02

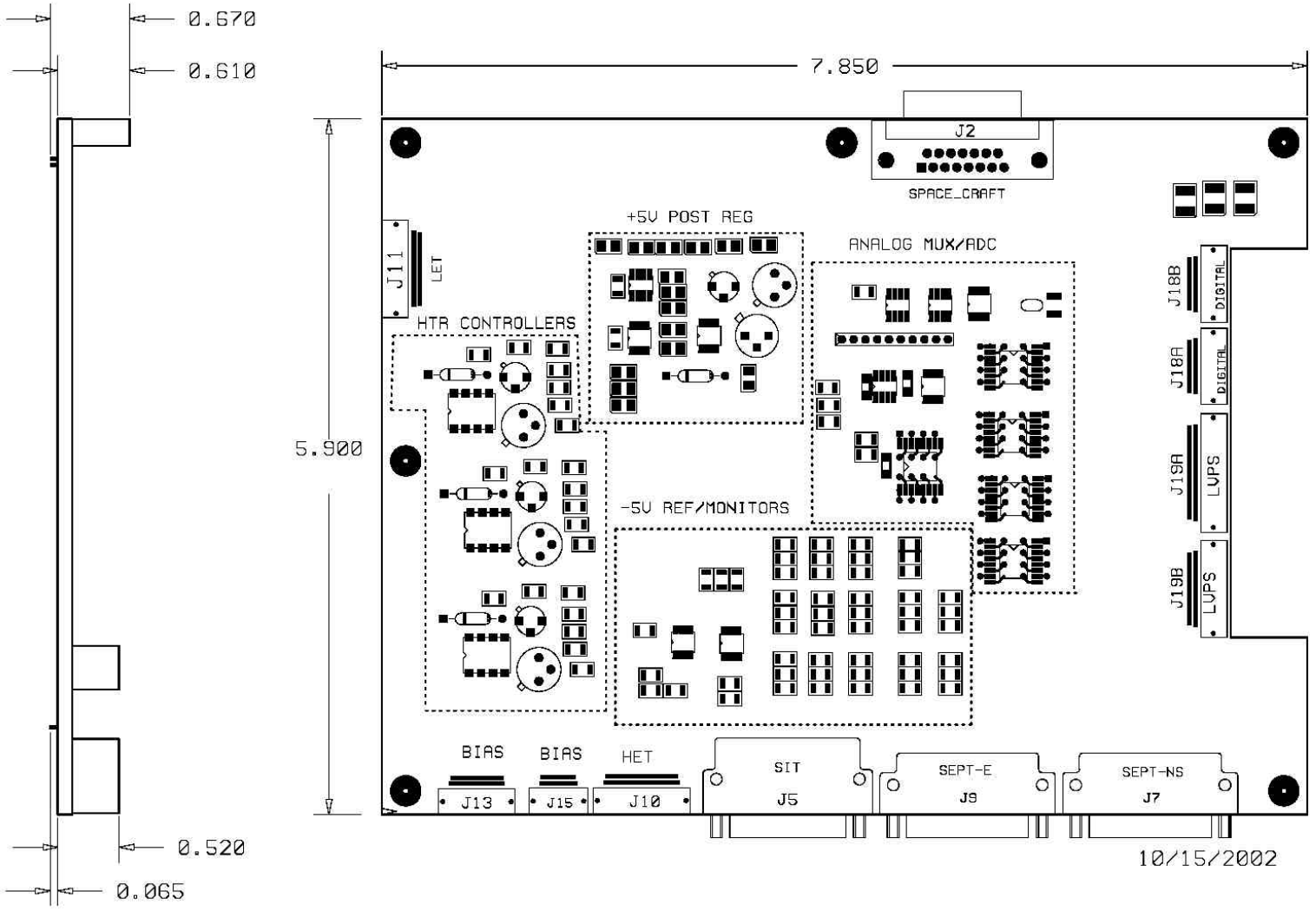
Voltage	Type	SEPT	SIT	LET	HET	Central	Totals
2.6 V[1)]	Digital	52	57	44	44	26	**223**
3.4 V	Digital		170	186	186	98	**640**
5.1 V	Digital		57	5	5	27	**94**
5.3 V[1)]	Digital	128					**128**
-5.2 V	Digital		560				**560**
5.6 V[1)]	Analog	806					**806**
6.0 V	Analog		295[2)]	588	80	50	**1013**
-6.0 V	Analog		46	4	4	6	**60**
13.0 V	Analog		160	48	48	145	**401**
-13.0 V	Analog		19	64	35	52	**170**
		------	------	-----	-----	-----	------
Sensor subtotals:		**986**	**1364**	**939**	**402**	**404**	**4095**
LVPS consumption @ 65% efficiency:							**2205**
SEP nominal power consumption:							**6300**

1) Actually multiple outputs.
2) Includes regulated power at 5.1 V.

Analog/Post-Reg Board

- **Functions:**
  - **Distribution of low voltage power**
  - **Regulation of SIT analog 5.1V**
  - **Routing of interface signals**
  - **Housekeeping ADC**
  - **Heater control for SEPT and SEP Central**
- **Design and fabrication by Space Instruments, Inc., with close Caltech supervision.**
- **Electrical design complete.**
- **Mechanical interface is defined, with connector locations specified.**

Analog/Post-Reg Board Layout Assessment

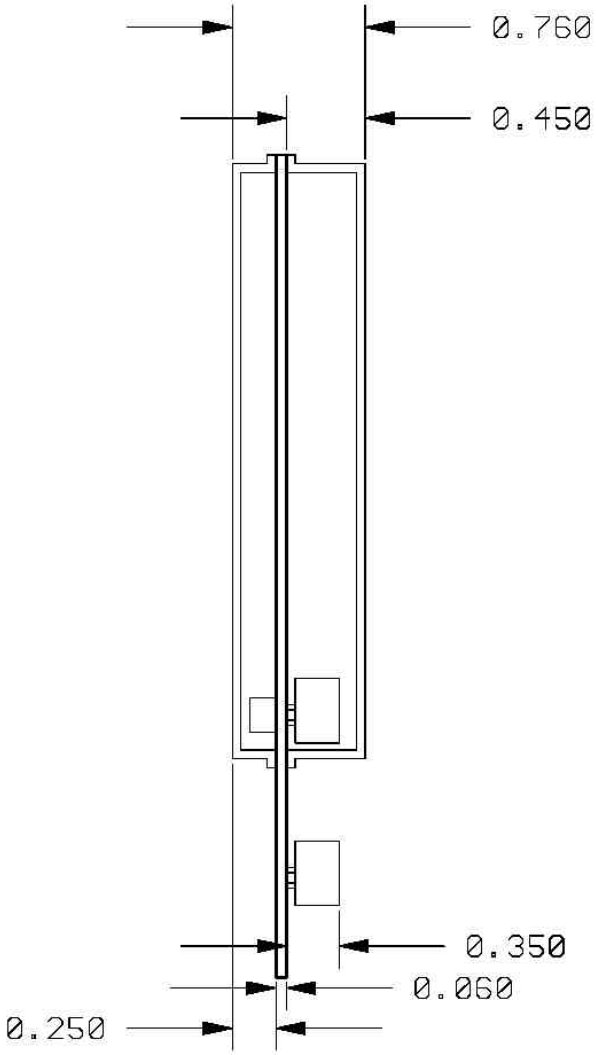


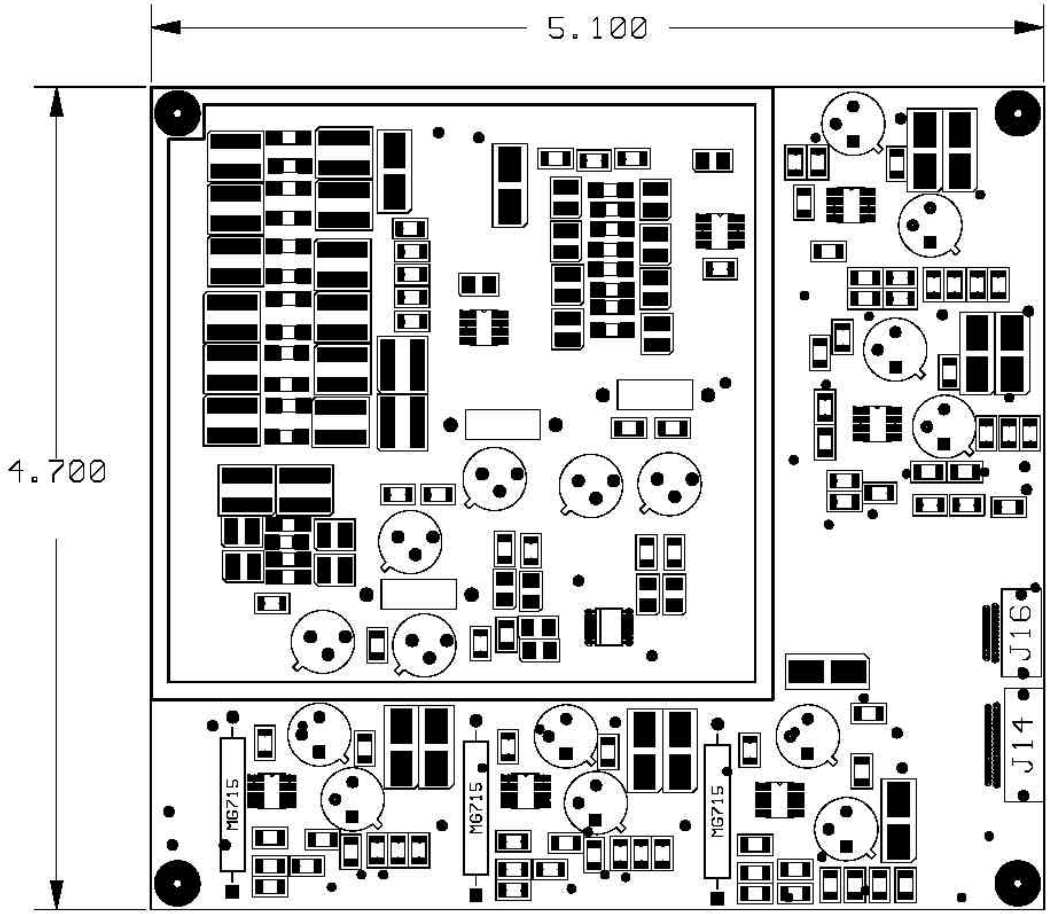
SSD Bias Supply Requirements

Tap	Bias Signals	Nominal Voltage	Voltage Range	EOL uA at 40C	Current Limit (uA)
100V	LET L1	10	2 to 30	148	281
100V	LET L2	30	5 to 50	19	102
300V	LET L3 & HET H1-6	250	50 to 250	193	610
200V	SIT SSD	160	150 to 200	15	20
-100V	SEPT	-80V	-30 to -80	67	107

- Two separate charge pumps, one positive (multi-tap) and one negative
- Five series regulators with output voltages fixed by resistor selection
- Series regulator current limits selected to tolerate detector leakage currents plus any worst-case single detector short
- Ripple < 2 mV pp; spikes < 5 mV pp
- Design and fab by Space Instruments, Inc.

SSD Bias Supply Layout Assessment

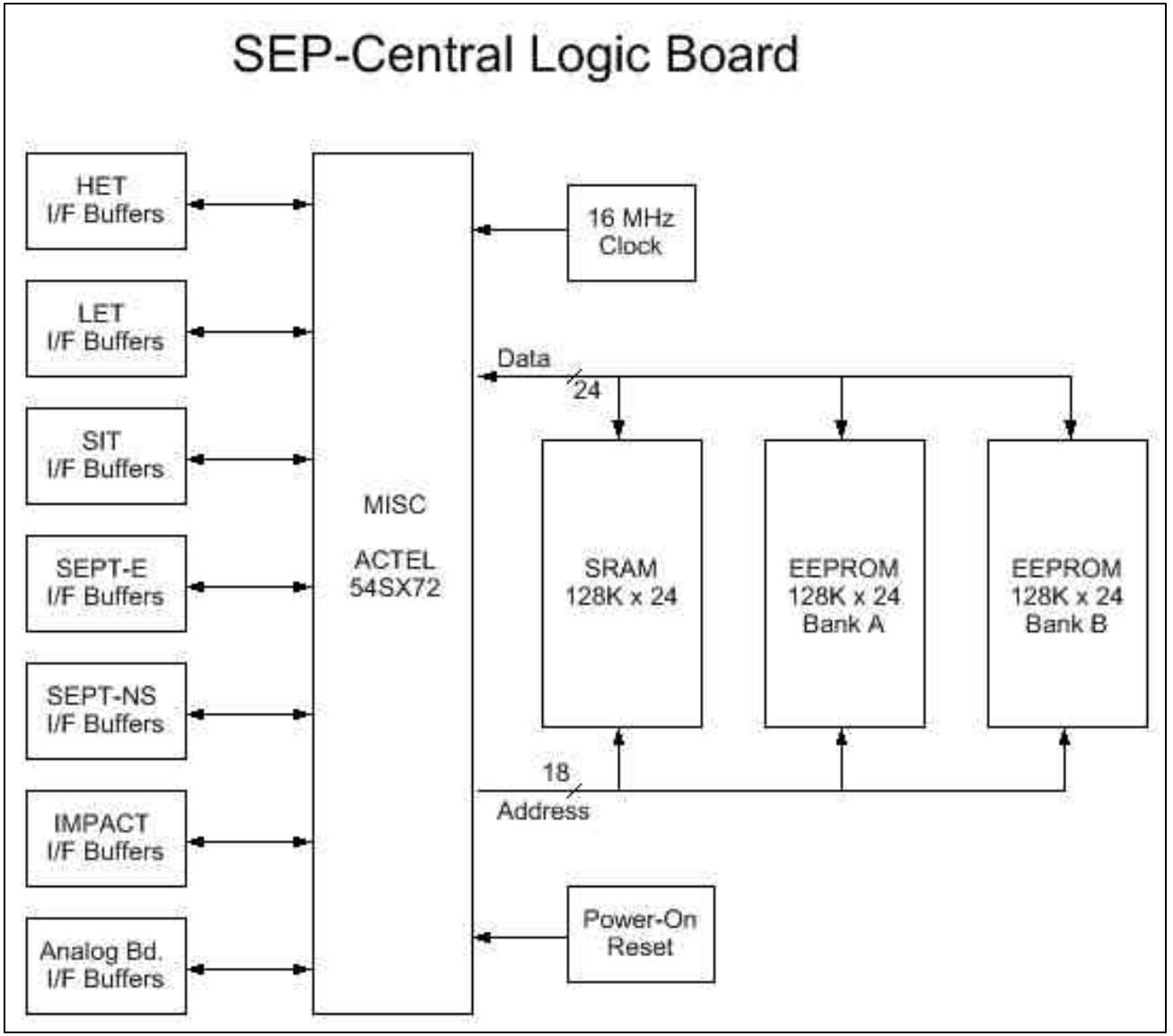


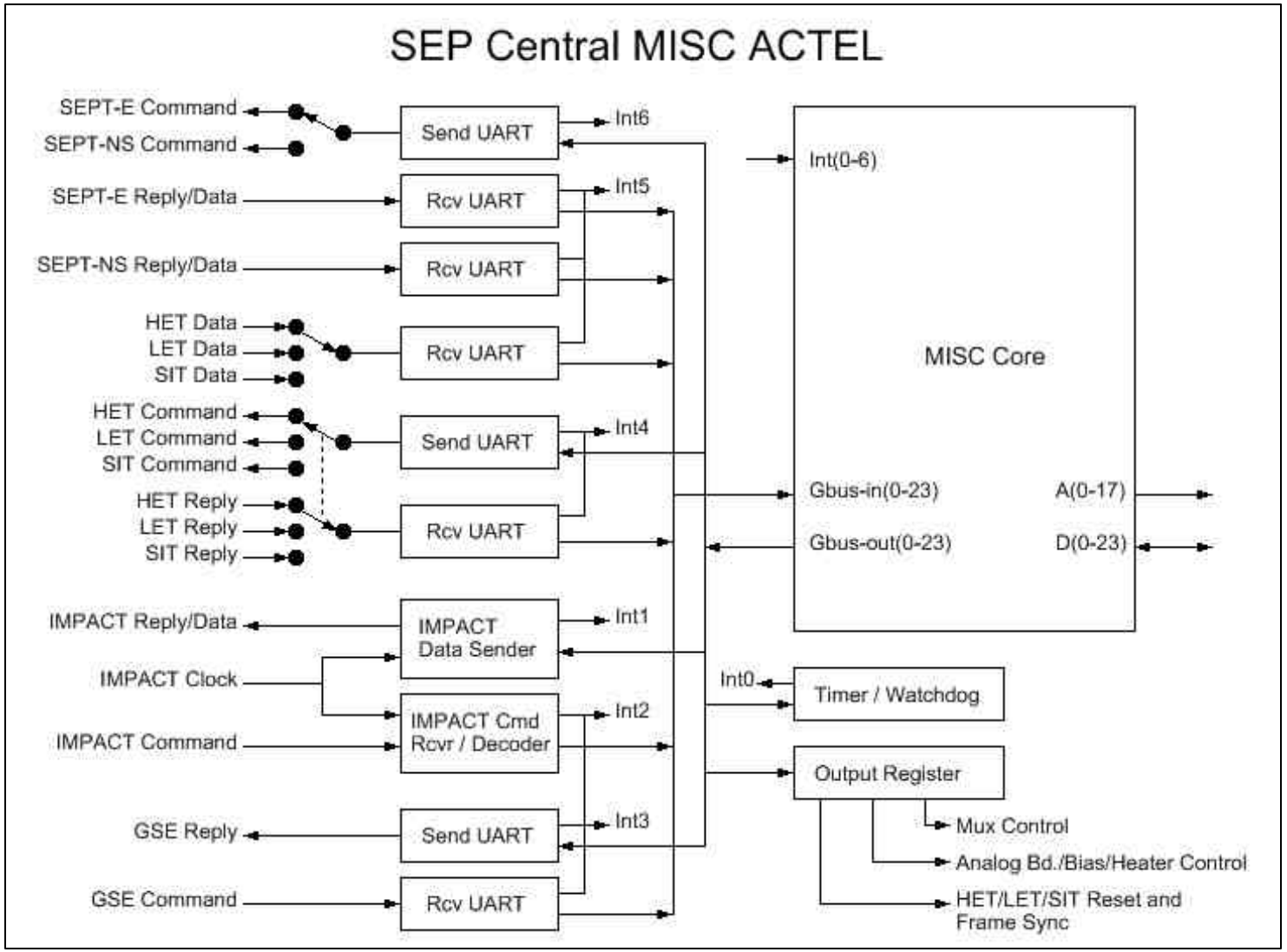


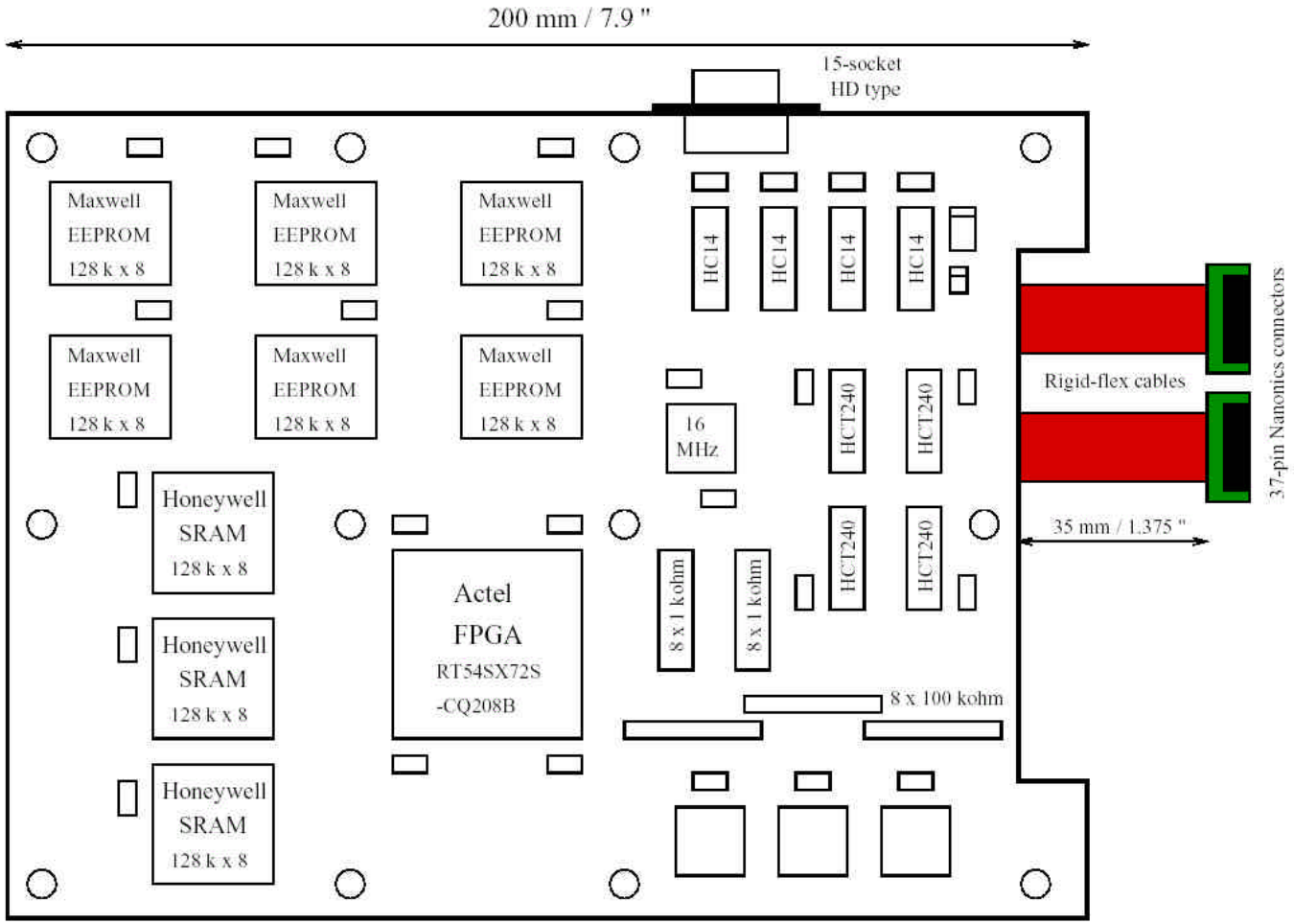
Logic Board (SEP DPU)

Contains:

- **MISC processor with 128k x 24 SRAM and 256k x 24 EEPROM**
- **Digital interfaces with SIT, HET, LET, SEPT and IMPACT IDPU (defined by ICDs)**
- **Interface with HK ADC.**
- **On/off control of SSD bias supplies**
- **Operational heater control**
- **Mechanical interface TBD, approx. size: 15 x 20 cm**


SEP-Central Logic Board
HET I/F Buffers
LET I/F Buffers
SIT I/F Buffers
SEPT-E I/F Buffers
SEPT-NS I/F Buffers
IMPACT I/F Buffers
Analog Bd. I/F Buffers
MISC
ACTEL 54SX72
16 MHz Clock
Data
24
SRAM 128K x 24
EEPROM 128K x 24 Bank A
EEPROM 128K x 24 Bank B
18
Address
Power-On Reset


SEP Central MISC ACTEL
SEPT-E Command
SEPT-NS Command
Send UART
Int6
SEPT-E Reply/Data
Rcv UART
Int5
SEPT-NS Reply/Data
Rcv UART
HET Data
LET Data
SIT Data
Rcv UART
HET Command
LET Command
SIT Command
Send UART
Int4
HET Reply
LET Reply
SIT Reply
Rcv UART
IMPACT Reply/Data
IMPACT Data Sender
Int1
IMPACT Clock
IMPACT Cmd Rcvr / Decoder
Int2
IMPACT Command
GSE Reply
Send UART
Int3
GSE Command
Rcv UART
Int(0-6)
MISC Core
Gbus-in(0-23)
A(0-17)
Gbus-out(0-23)
D(0-23)
Int0
Timer / Watchdog
Output Register
Mux Control
Analog Bd./Bias/Heater Control
HET/LET/SIT Reset and Frame Sync



SEP Logic Board Layout Assessment

BK 11/5/02

Parts

- Logic:
  - RT54SX72S - Actel FPGA
  - HLX6228 - Honeywell SRAM, 128k x 8
  - 28LV010RP – Maxwell Technologies with Hitachi EEPROM, 128k x 8
  - HCS14KMSR - interface receiver with Schmitt trigger inputs
  - HCTS240KMSR - interface driver
  - Q-TECH 16 and 32 MHz clock oscillators
- Discrete:
  - Will use grade 2 or better. Spare ACE parts available (parts with cavity require re-screening).
- Custom VLSI:
  - PHASIC chips from AMIS, used in hybrids built at JPL per MIL STD 883 Class H.

Connectors and Harness

- Rigid-flex used internally to minimize # of connectors.
- Nanonics for internal cables, MDM, D and HD for external.
- Have redundant wires in all cables.
- SEPT digital lines additionally shielded within the main shield.
- 26 AWG on SIT power lines and returns.
- 28 AWG on all SEPT lines to save weight.
- Use composite EMI backshells to save weight.

SEP resources: Mass [g] 11/12/02

Component	PDR	CDR
SIT sensor & door	500	483
SIT elec. boards & wiring	370	518
SIT HVPS	160	260
SIT encl. & hdwr	200	200
SIT subtotal:	**1230**	**1461**
SEPT-NS	520	666
SEPT-E	520	666
SEPT subtotal:	**1040**	**1332**
LET det. & housing	515	565
LET electronics	235	306
LET subtotal:	**750**	**871**
HET det. & housing	500	500
HET electronics	160	239
HET subtotal:	**660**	**739**

SEP resources: Mass [g] cont. 11/12/02

Component	PDR		CDR	
Cent. elec. encl. & hdwr	1500		1575	
El. boards, shields, harness	1090		1354	
----------	------		------	
Central electr. subtotal:	**2590**		**2929**	
SEPT-NS bracket	270		270	
LET bracket	600		600	
----------	------		------	
SEP subtotal:	**7140**		**8202**	
		26 AWG		28 AWG
SEPT-NS Ahead harness	185	@ 1.7 m	186	@ 2.13 m
SEPT-NS Behind harness	293	@ 2.9 m	290	@ 3.48 m
SEPT-E Ahead harness	73	@ 0.4 m	94	@ 0.94 m
SEPT-E Behind harness	240	@ 2.3 m	210	@ 2.44 m
Thermal blankets	120		120	
SEP Ahead total:	**7518**		**8602**	
SEP Behind total:	**7793**		**8822**	

SEP resources: Power [mW] 11/12/02

Component	PDR	CDR
SIT HVPS & energy el.	473	332
TOF electronics	680	871
MISC @ 4 MHz & DAC	120	161
SIT subtotal:	**1273**	**1364**
SEPT-NS	502.5	493
SEPT-E	502.5	493
SEPT subtotal:	**1005**	**986**
PHASIC hybrids	486	486
+5V reg, -5V ref, etc.	N/A	217
HK ADC	65	6
MISC @ 8 MHz	223	230
LET subtotal:	**774**	**939**

SEP resources: Power [mW] cont. 11/12/02

Component	PDR		CDR	
PHASIC hybrids	63		63	
+5V reg, -5V ref, etc.	N/A		103	
HK ADC	65		6	
MISC @ 8 MHz	223		230	
----------	-----		-----	
HET subtotal:	**351**		**402**	
Analog/Post-Reg	208		181	
Logic (MISC @ 4MHz)	120		124	
SSD Bias Supply	202	@ +20 C *	99	@ +20 C *
----------	-----		-----	
Central electr. sub.:	**530**		**404**	
SEP subtotal:	**3933**		**4095**	
LVPS (@ 65% eff.)	**2118**		**2205**	
----------	-----		-----	
SEP total:	**6051**		**6300**	

* SSD Bias Supply capable of consuming 195 mW @ +35 C & end of detector life.
If 5 unique detectors short-circuited, it consumes 320 mW @ +35 C & end of life.

SEP resources: Data rate [bit/s] 11/12/02

Component	PDR	CDR		
	Science	Science	HK	Beacon
SIT	243.6	417.6	1.2	3.2
SEPT	69.6	69.6	2.4	5.9
LET	348	556.8	0.5	6.1
HET	139.2	208.8	1.2	3.7
Central electronics	0	0	3.2	0.3
SEP subtotal:	**800.4**	**1252.8**	**8.5**	**19.2**
CCSDS packet header	N/A	52.8	0	0
SEP total:	**800.4**	**1305.6**	**8.5**	**19.2**

SEP resources: Data rate [bit/s] cont. 11/12/02

- **Science data**
  - **2088 bits/packet (w/o packet headers)**
  - **36 CCSDS packets/minute distributed as follows:**
    LET - 16, SIT - 12, HET - 6, SEPT - 2

- **Housekeeping data**
  - **64 bytes/minute**
  - **1 message/minute. Bytes/minute distributed as follows :**
    LET - 4, SIT - 9, HET - 9, SEPT - 18, SEP Central - 24

- **Beacon data**
  - **144 bytes/minute**
  - **1 message/minute. Bytes/minute distributed as follows:**
    LET - 46, SIT - 24, HET - 28, SEPT - 44, Status - 2

Parts/Materials Status

- **Parts**
  - Parts List delivered & approved
  - Complying with GSFC-311-INST grade 2 requirements
  - Monitoring GIDEP alerts
  - Actel RT54SX72S procured via Project common buy
  - Other long lead-time EEE parts on order/in stock
  - Found HV capacitor substitute for discontinued ACE vendor
  - Using custom-made ACE database for parts inventory and kiting

- **Materials**
  - Materials and Processes List delivered & undergoing review
  - Using JPL D-8208 material selection guidelines
  - Consulting with Project & JPL contamination control engineers

Transportation Issues

- **Container properties**
  - Custom design, metal construction
  - Built-in shock absorbers
  - Hermetically sealed
  - Purge & vent ports with manual control
- **In transit**
  - Use double bag inside container and both bag and container backfilled with dry nitrogen
  - In a sealed container OK without purge for ~24 hours
  - Buy container an economy-class ticket on airline
  - Concerned about getting through airport security
- **ESD & contamination control**
  - Load/unload the container on ESD-safe clean bench
  - Apply double-bagging and extra purge at testing sites