

## LET Solid-State Detectors

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## LET Detector Responsibilities

- **JPL**

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**Beverley Eyre**  
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**Jon DePew**

**overall management**  
**silicon thinning**  
**software support**  
**hardware support**

- **Caltech**

**Allan Labrador**  
**Sven Geier**

**detector testing**  
**detector testing**

- **GSFC**

**Tycho von Rosenvinge**  
**Sandy Shuman**  
**Bert Nahori**

**oversight**  
**mount design**  
**detector testing**

- **Micron Semiconductor**

**detector fabrication**

## LET Detector Designs

- Detector technology: Ion-implanted silicon
- 3 detector designs used in LET

Designation	Sensitive Thickness	Active Area	Elements	Number of Devices (one S/C)
L1	20 mm	2.0 cm <sup>2</sup>	3	10
L2	50 mm	13.6 cm <sup>2</sup>	10	2
L3	1000 mm	19.7 cm <sup>2</sup>	2	2

- L2 and L3 are conventional designs and are routine to fabricate
- L1 is a new development (discussed below)

## L2 and L3 Detector Specifications

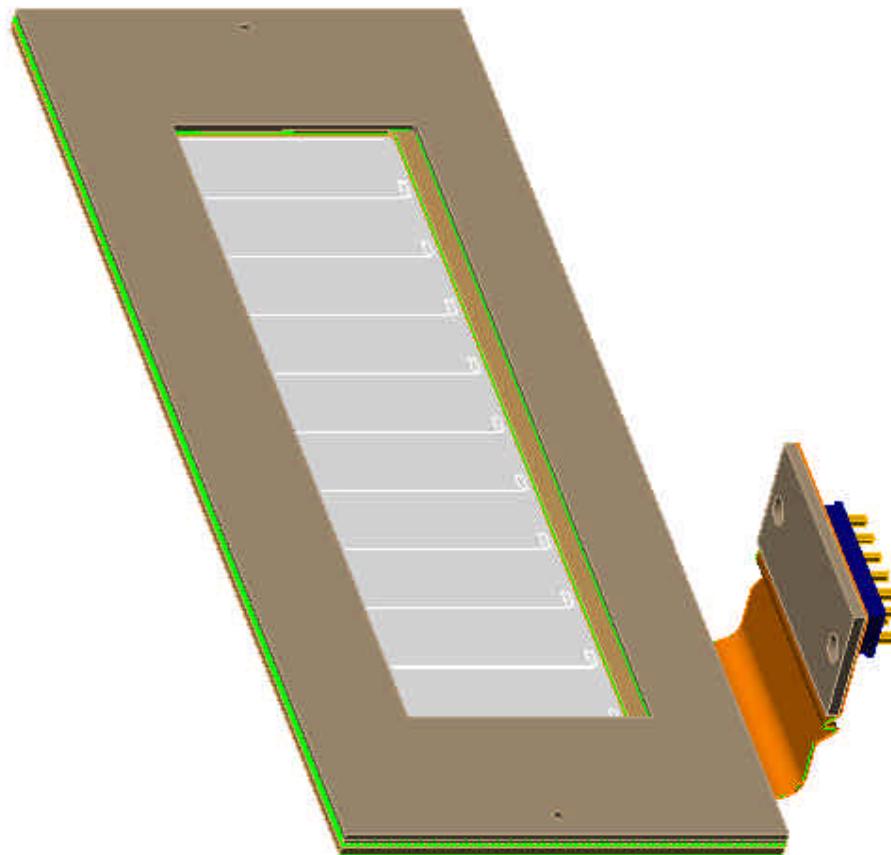
1	Detector Identification	L2	L3
2	Shape	Rectangular	Rectangular
3	Active Area Dimensions (cm)	$6.4 \times 1.6$	$7.8 \times 2.0$
4	Overall Area Dimensions (cm)	$6.8 \times 2.0$	$8.2 \times 2.4$
5	Average Thickness ( $\mu\text{m}$ )	$50 \pm 5$	$1000 \pm 50$
6	Max. Thickness Nonuniformity ( $\mu\text{m}$ )	5	25
7	Offcut Min. Dimensions (cm) *	2 each @ $6.4 \times 0.3$ 2 each @ $1.6 \times 0.3$	2 each @ $7.8 \times 0.3$ 2 each @ $2.0 \times 0.3$
8	Active Junction-Surface Contacts	10	3
9	Geometry of Junction-Surface Contacts †	linear array of 10 contacts, each 0.64 cm $\times$ 1.6 cm	linear array of 3 contacts, center contact 2.4 cm long and outer contacts each 2.7 cm long
10	Contact Spacing ( $\mu\text{m}$ )	$20 \pm 5$	$40 \pm 10$
11	Junction Surface Connections	wire bonds	wire bonds
12	Ohmic Surface Connections	wire bonds	wire bonds
13	Max. Depletion Voltage (Volts)	20	200
14	Min. Breakdown Voltage (Volts)	50	250
15	Max. Leakage Current ( $\mu\text{A}$ )	0.5	2.
16	Max. Alpha Resolution (keV FWHM)	100	100

Notes:

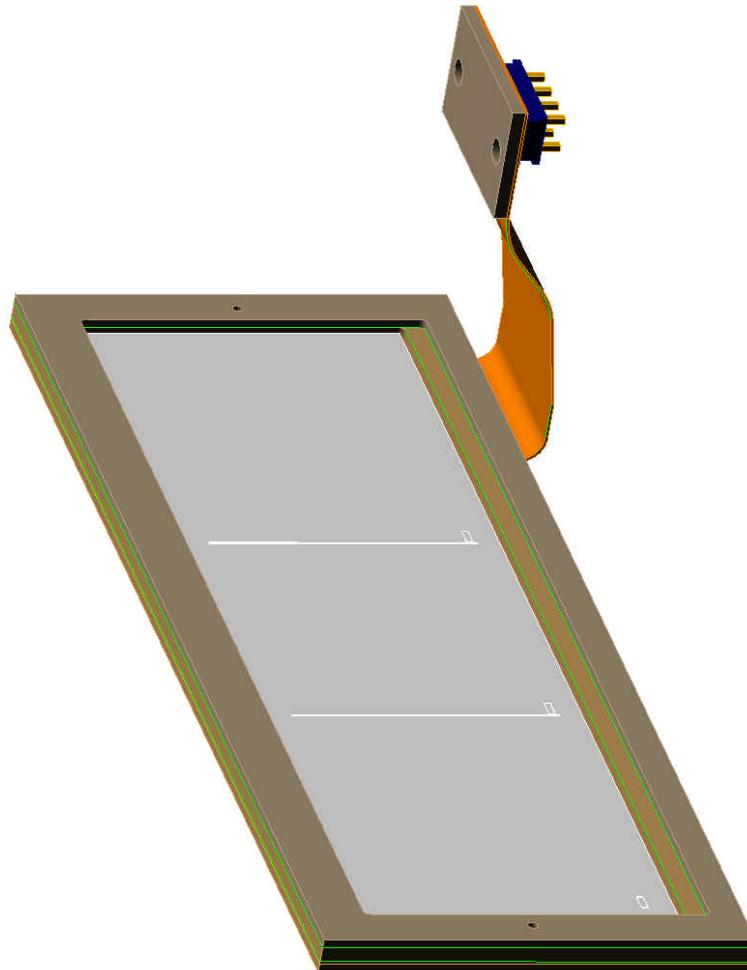
\* The number and size of offcuts are to be treated as goals.

† In the multi-contact designs, contact dimensions given include the metallization area plus half the gaps between adjacent contacts.

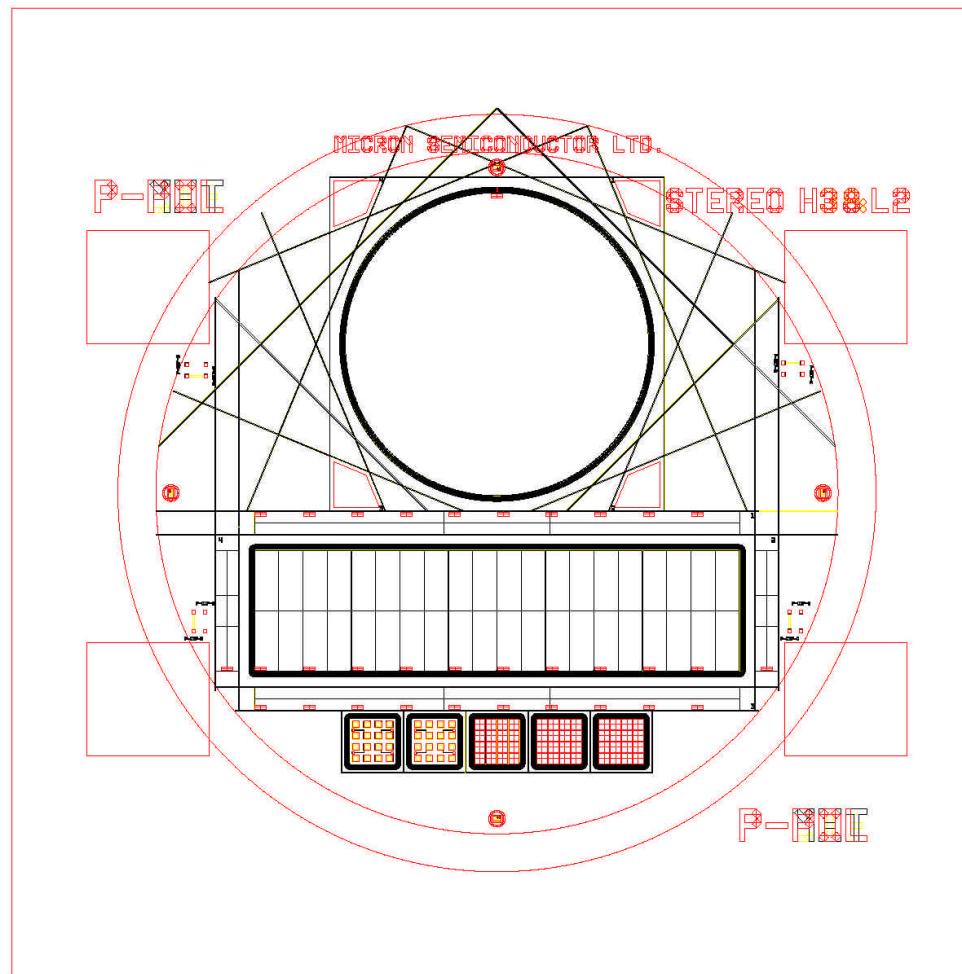
## L2 Detector Assembly



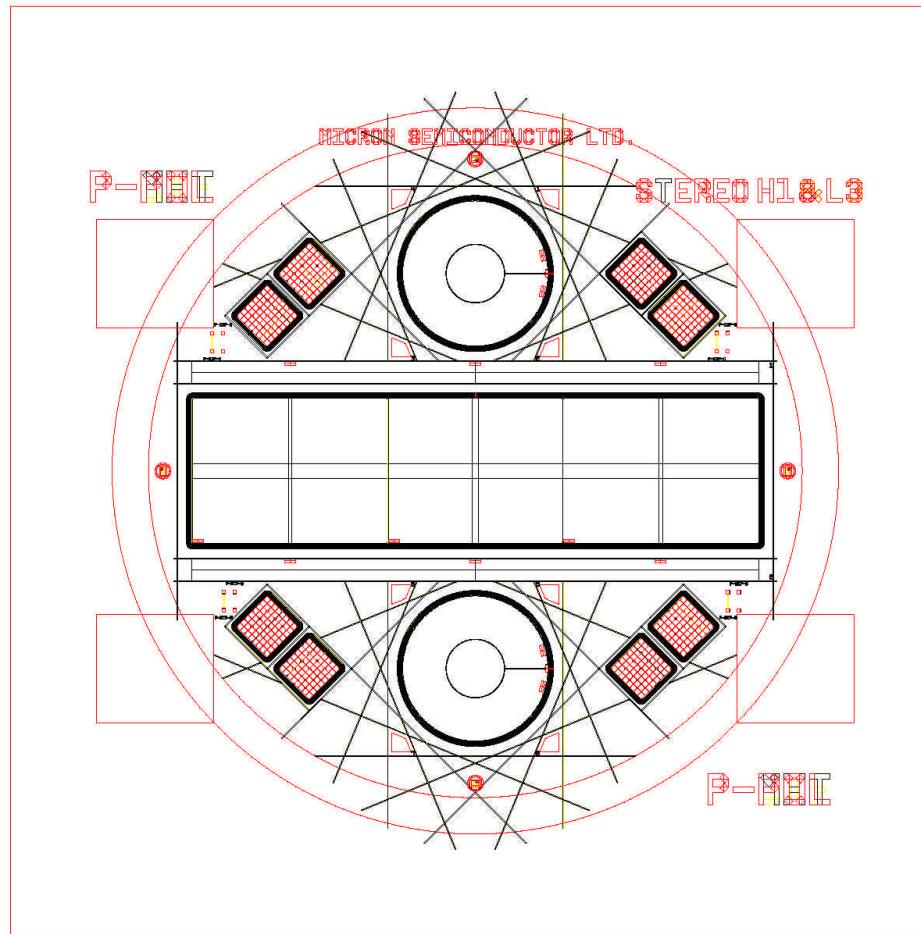
## L3 Detector Assembly



## L2 Design: Photolithography (combined with H3)



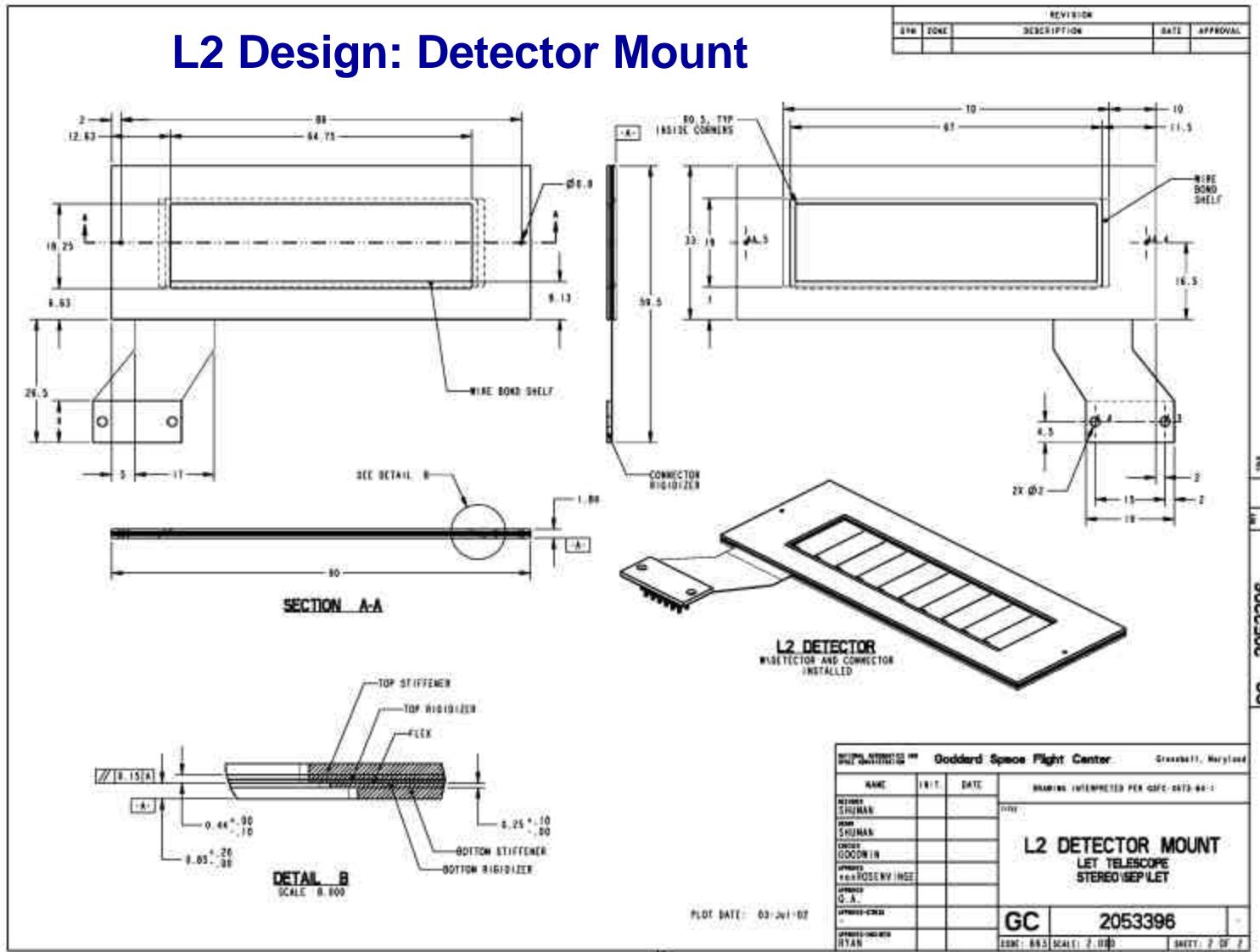
## L3 Design: Photolithography (combined with H1)



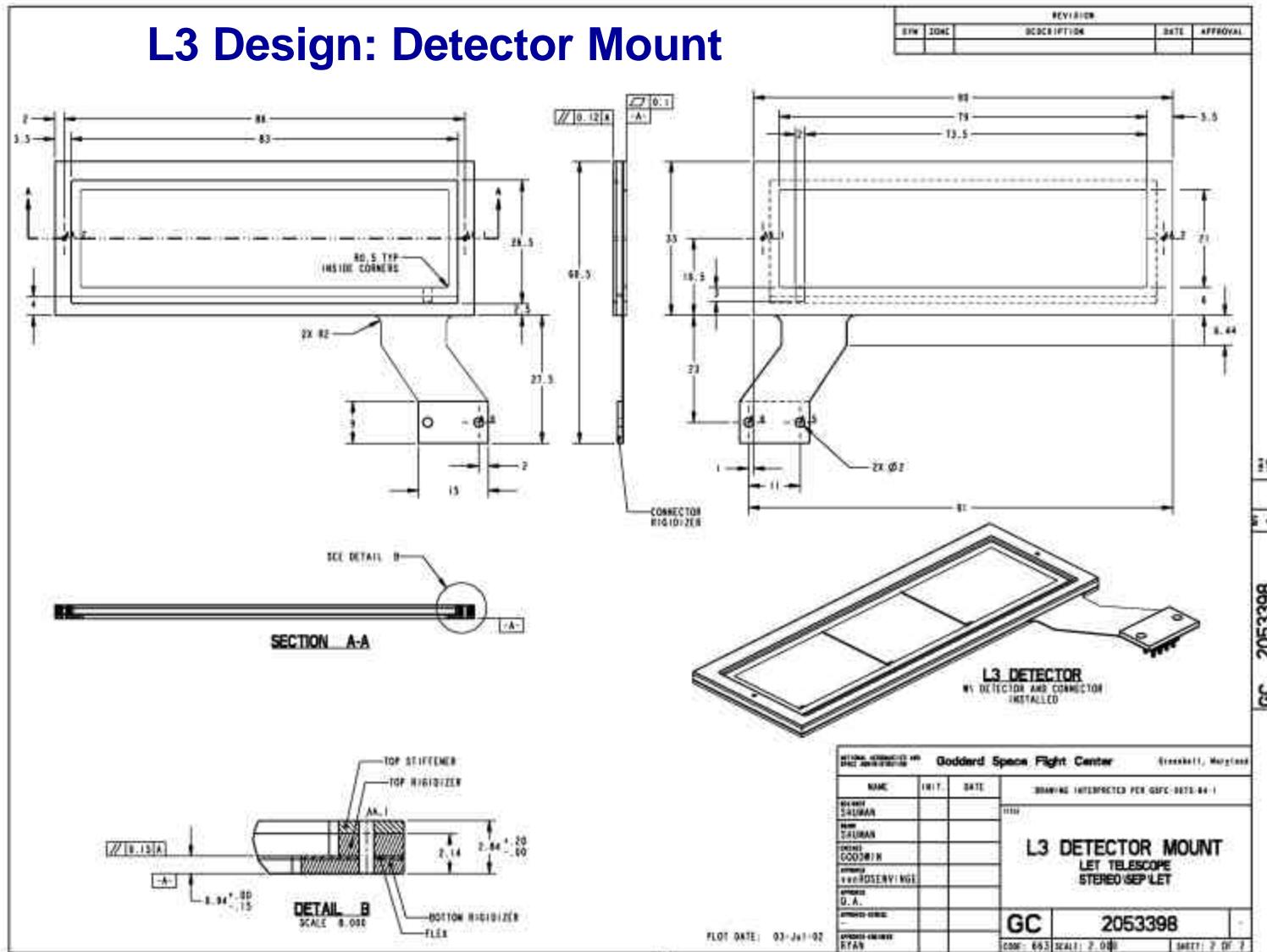
# STEREO IMPACT

## Critical Design Review 2002 November 20,21,22

## L2 Design: Detector Mount



## L3 Design: Detector Mount



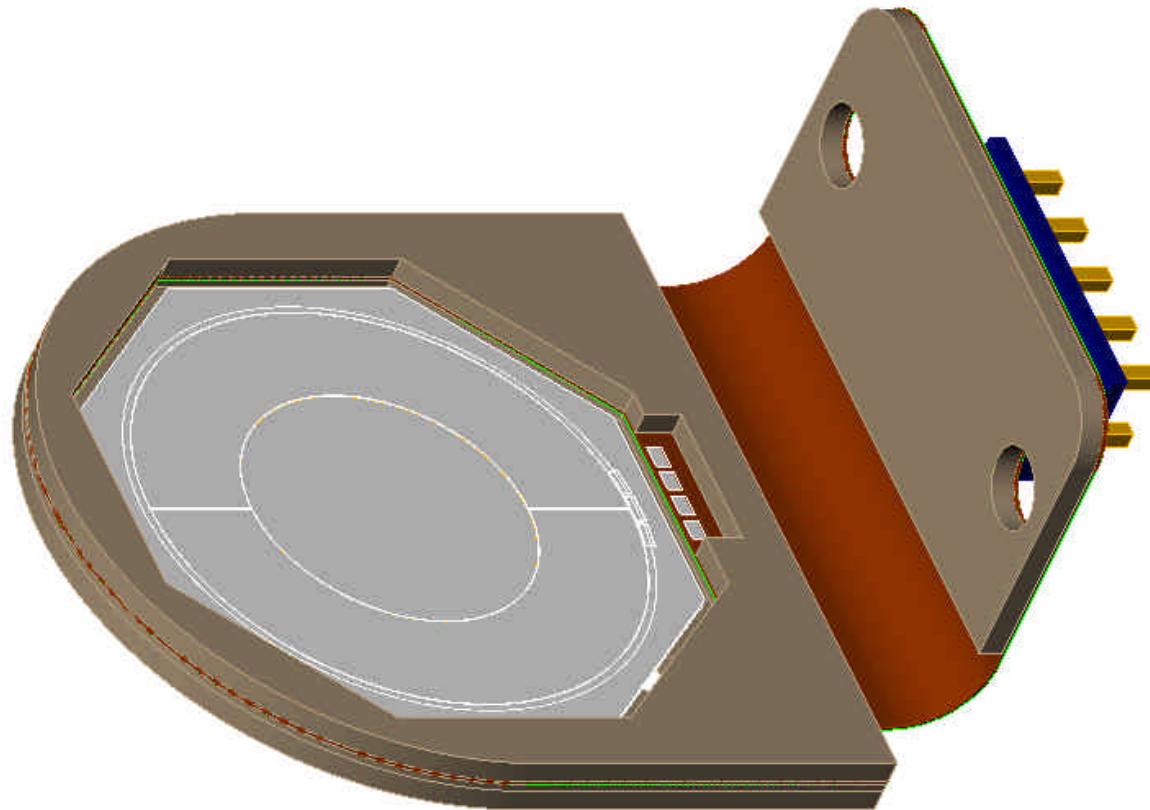
## L2 & L3 Prototype Development Status (6 Nov 2002)

- All mask sets fabricated
- Wafers with prototype detectors fabricated and probe tested
- Mounts being fabricated and inspected
- Detectors being cut out and mounted in preparation for testing by Micron
- Delivery expected November/December 2002

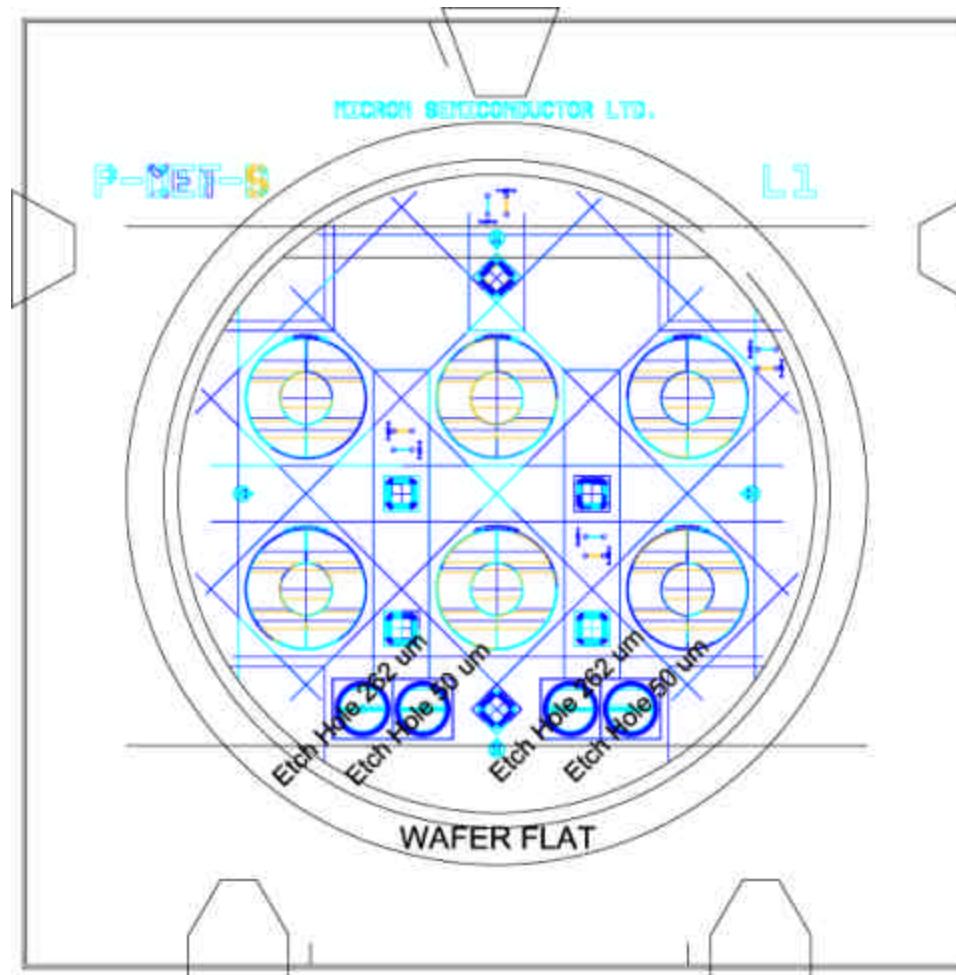
## LET L1 Detectors - Key Requirements

- **Very thin to allow low energy threshold for instrument**
- **Thickness uniformity sufficient for measuring He isotopes**
- **Segmented readout to accommodate high rate and reduce noise**

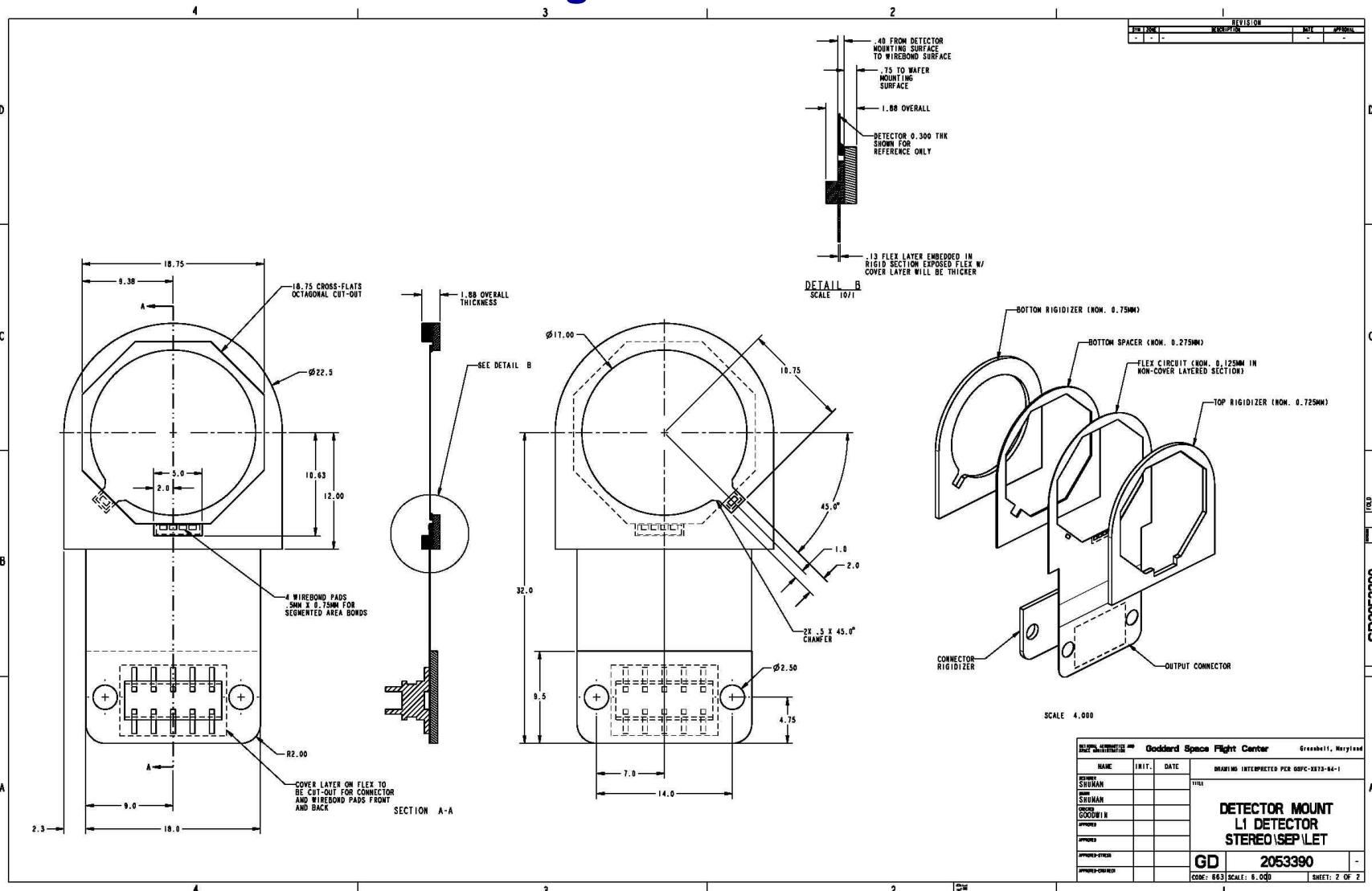
## L1 Detector Assembly



## L1 Design: Photolithography



## L1 Design: Detector Mount



## LET L1 Detectors: Possible Fabrication Approaches

Designation	Detector Thickness	Initial Wafer Thick-ness	Thinning Approach	Primary Advantages	Primary Disadvantages
Plan A	20 mm	140-300 mm	etch active areas in KOH	relatively rugged, best uniformity	unproven approach, more handling during fab
Plan B	20 mm	20 mm	lap & polish full wafer	similar to Micron conventional fab	fragile - uncertain yield, marginal uniformity
Plan A'	20 mm	140-300 mm	etch active areas in TMAH	relatively rugged, approach has been used, can all be done by Micron	marginal uniformity
Plan B'	30 mm	30 mm	lap & polish full wafer	proven technology, better resolution	higher instrument threshold

## LET L1 Detectors: Prototyping Status

Details of R&D work in Document “Thin Silicon R&D Summary” (STEREO-CIT-014.A)

### All Plans

- **mounts fabricated and delivered to Micron**

### Plan A

- **masks have been fabricated**
- **front-side patterning of wafers has been done**
- **etch tests of unprocessed wafers successfully completed**
- **etching of front-side-patterned wafers in progress**
- **problems of etch attacking front-side pattern being addressed**

### Plan B

- **masks have been fabricated**
- **wafers with prototype detectors fabricated and probe tested**
- **two prototypes delivered – tests are in progress**

## LET L1 Detectors: Prototyping Status (cont.)

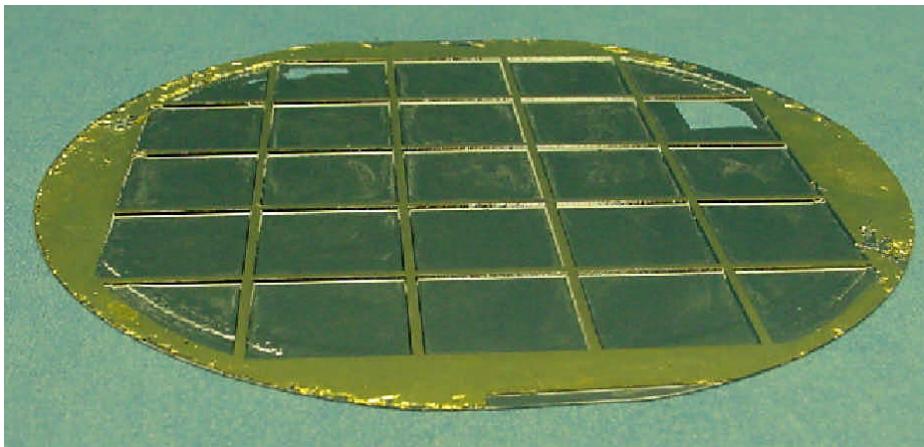
### Plan A'

- being tried by Micron with company resources
- thinned wafers with prototype detectors fabricated and probe tested
- six prototypes delivered – too thick, poor uniformity

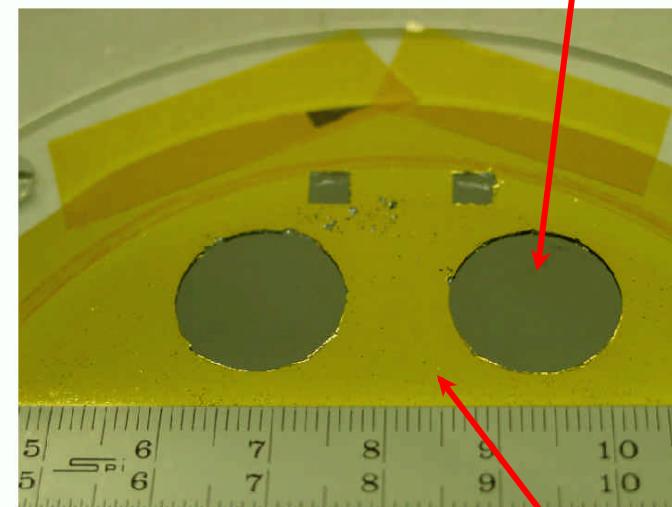
### Plan B'

- not presently being pursued
- no additional masking, fixturing, or mounts required
- available as a fall back

## Etching of 4" Silicon Wafers: Test Sample (left) & L1 (right)



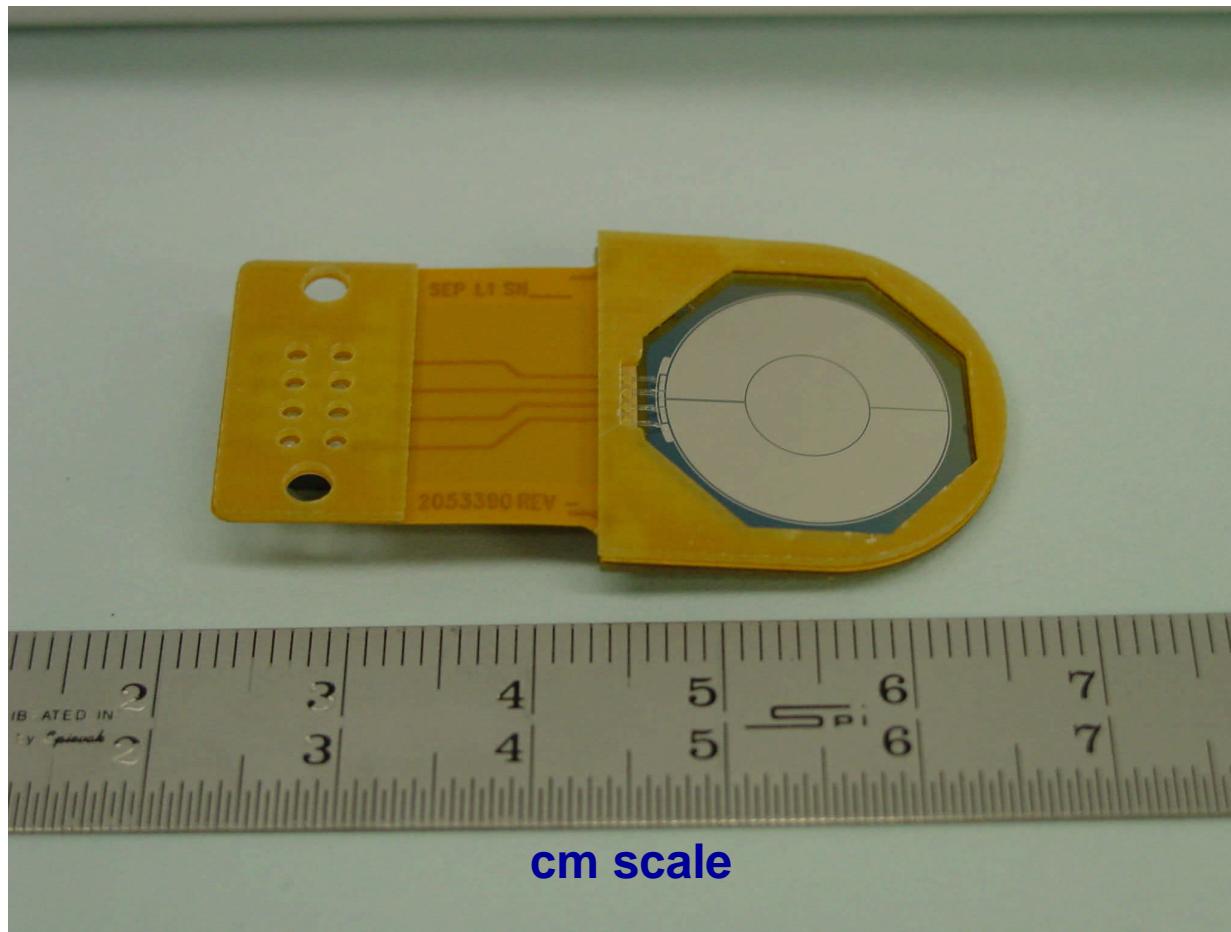
300 mm wafer thinned to ~16 mm



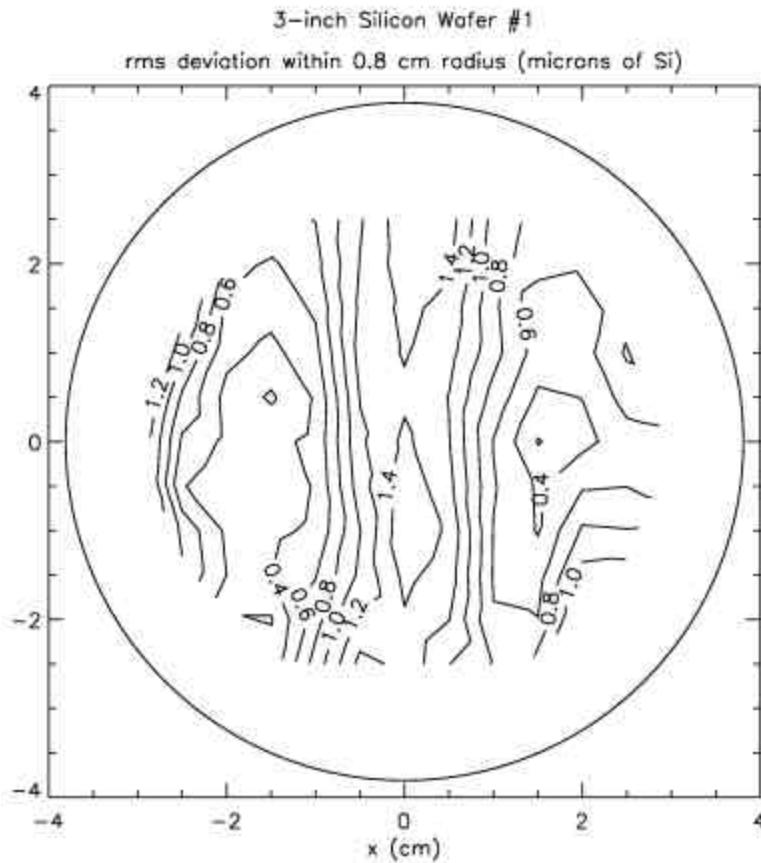
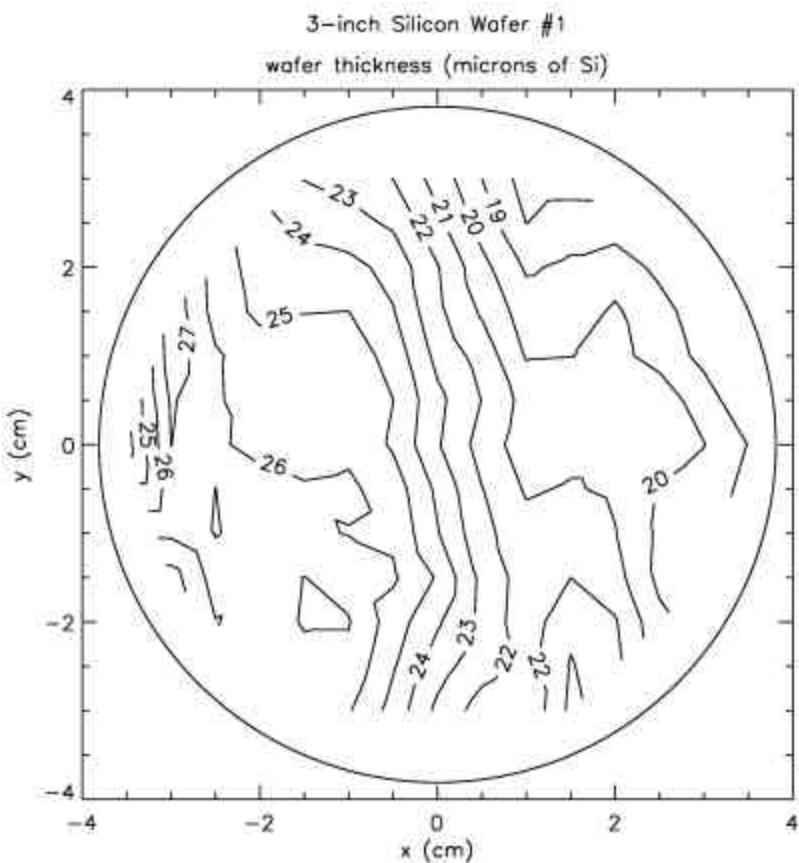
cm scale

300  $\mu$ m wafer  
Masked w/gold

## Prototype L1 Detector: $20 \text{ mm} \times 2 \text{ cm}^2$



## Plan B Wafer Thickness Maps



## Thickness Distribution of L1 Prototype

