Low Energy Telescope (LET) Overview

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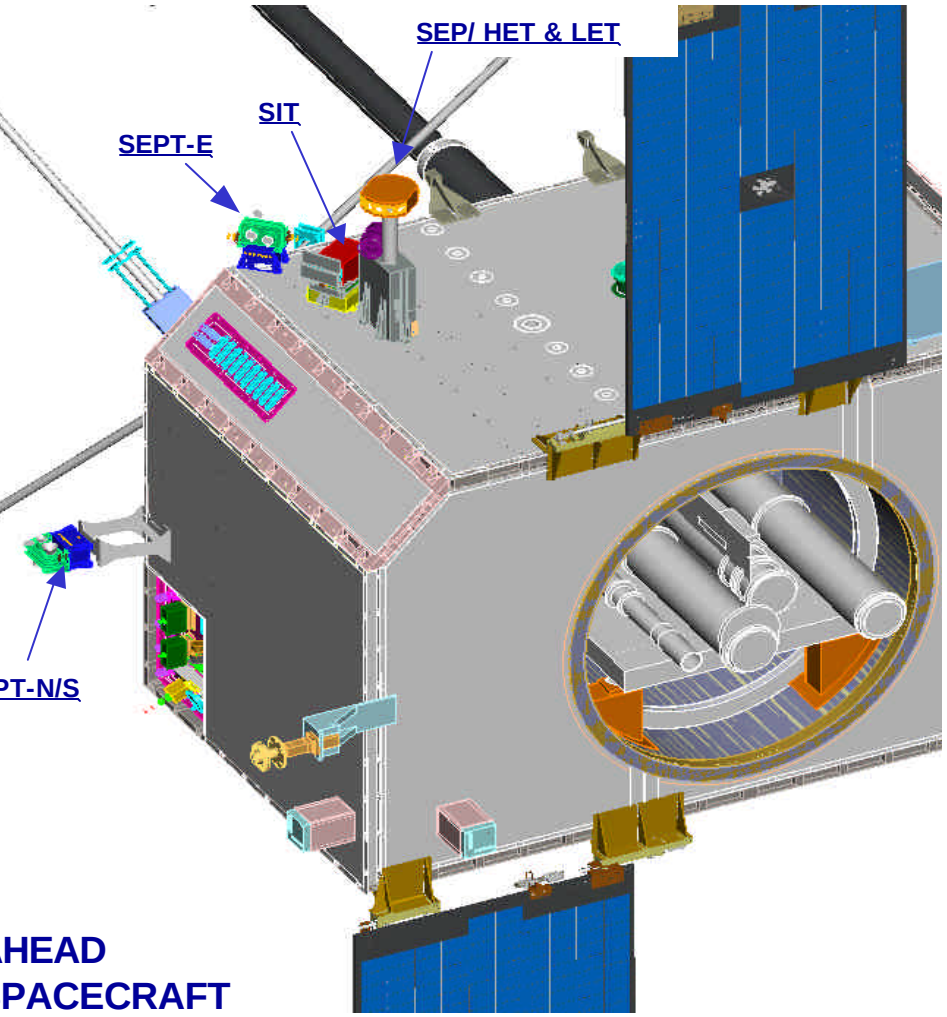
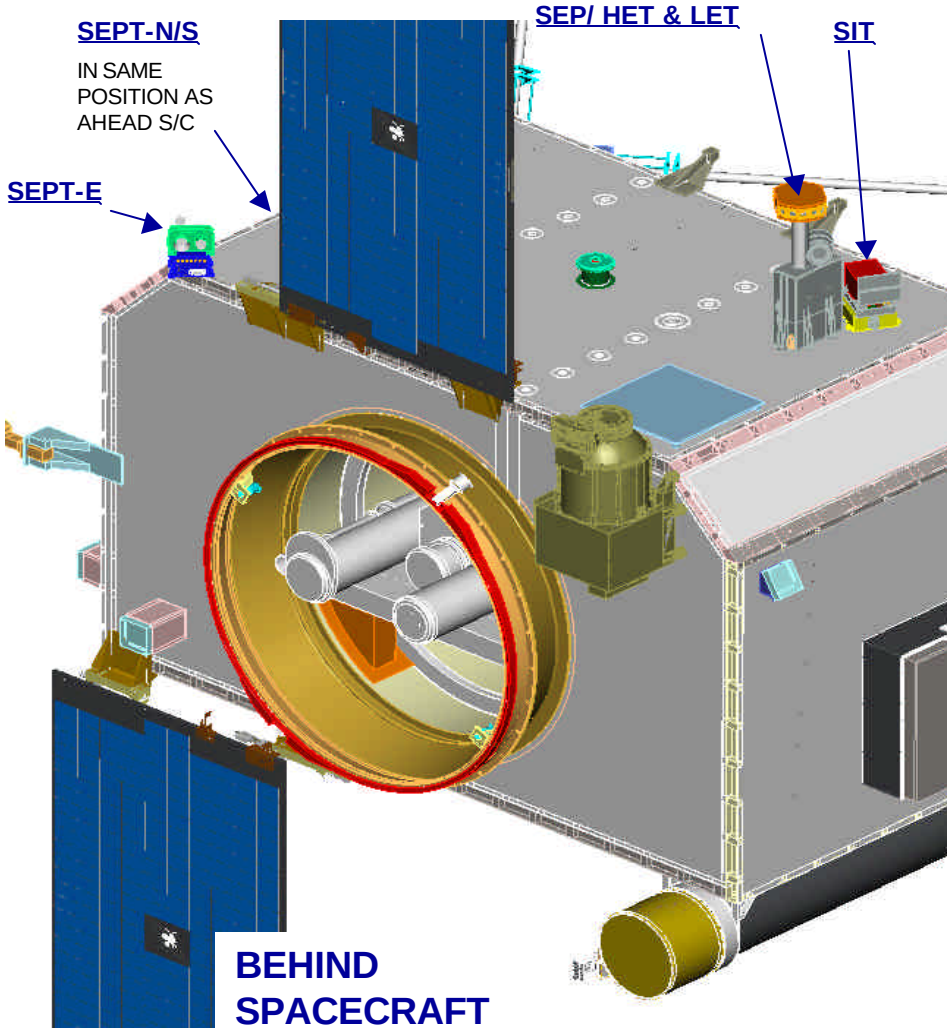
SEP Instrument Suites



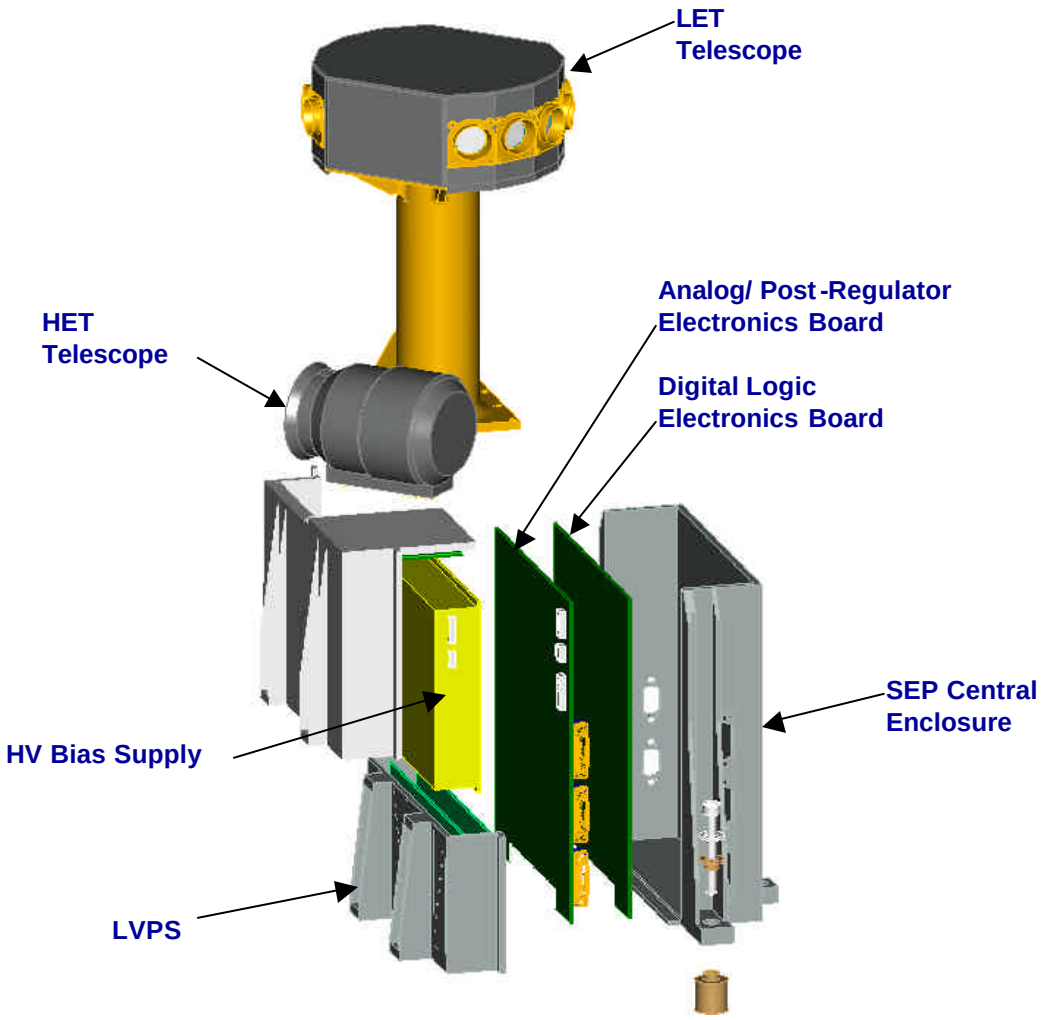
AHEAD SPACECRAFT



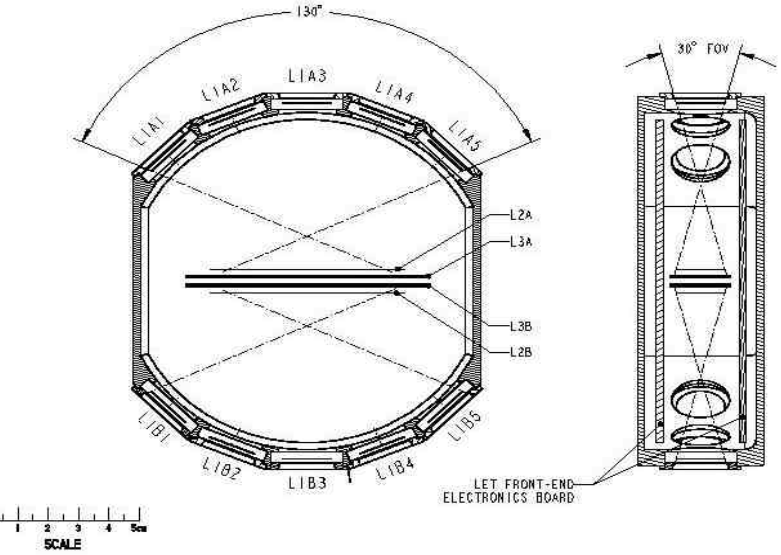
BEHIND SPACECRAFT

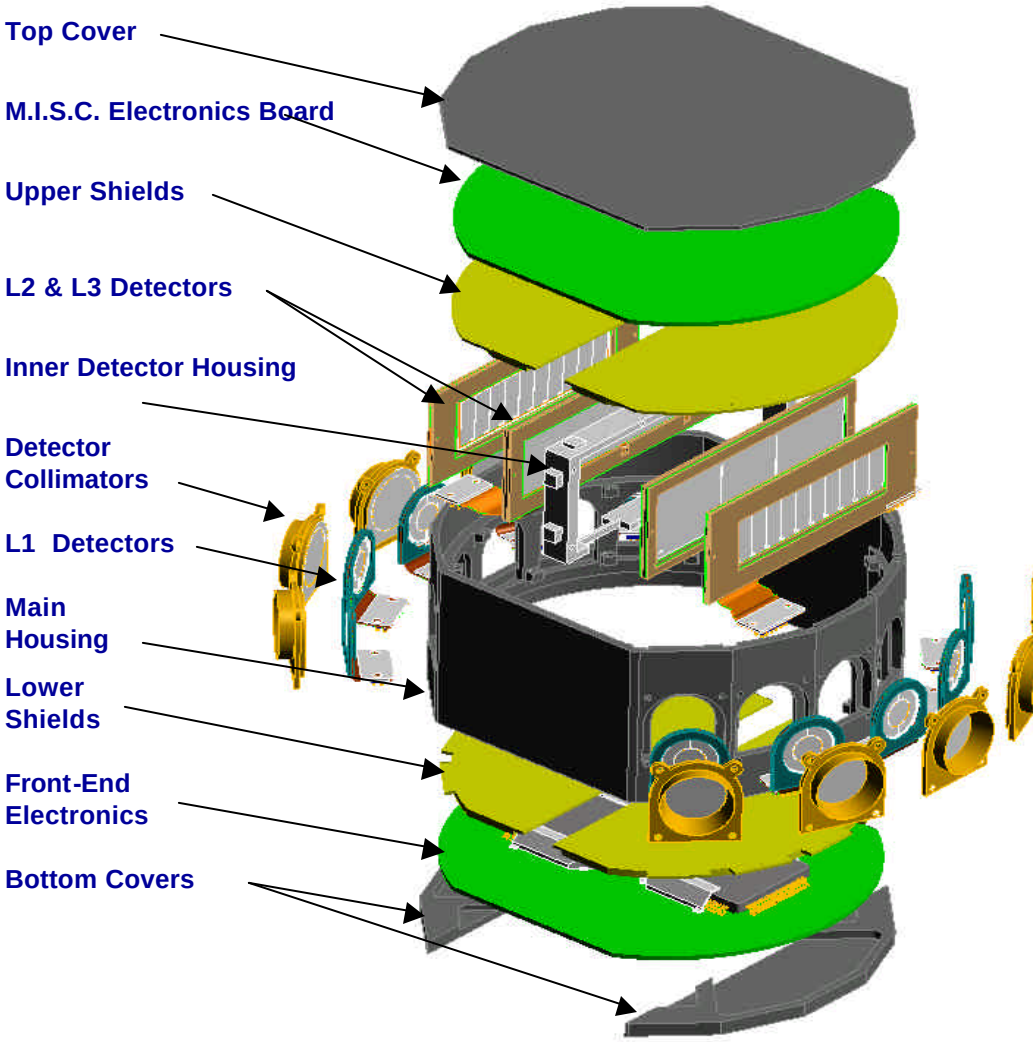
Main SEP Assembly

•Behind S/C configuration shown



Low Energy Telescope (LET) Schematic

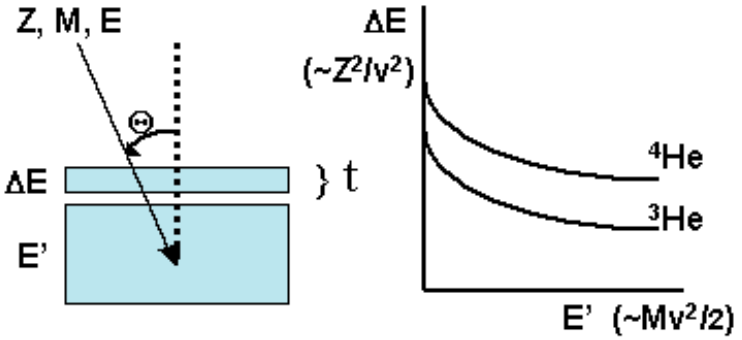




LET System

- dE/dX vs. E particle identifier
- Sensors (on each spacecraft)
  - Ten L1 Si ion-implanted detectors, 20 um x 2 cm^2 circular with 3 active areas, arranged in two sets of 5 around a "ferris wheel" (A side and B side form two identical telescopes)
  - Two L2 Si ion-implanted detectors, 50 um x 6.4 cm x 1.6 cm rectangular with 10 active areas, one for A side and one for B side
  - Two L3 Si ion-implanted detectors, 1 mm x 7.8 cm x 2.0 cm rectangular with 2 active areas, one for A side and one for B side
- 4 Pulse-Height Analysis System Integrated Circuit (PHASIC) chips packaged in 4 hybrids; each contains 16 channels of analog to digital signal processing
- One minimal instruction set computer (MISC) implemented in an Actel gate array
- SRAM
- Detector bias supply (shared, in SEP Central)
- Low voltage power supply (shared, in SEP Central)
- Analog/Post-regulator (shared, in SEP Central)
- Mechanical housing & bracket

Method of Element and Isotope Identification

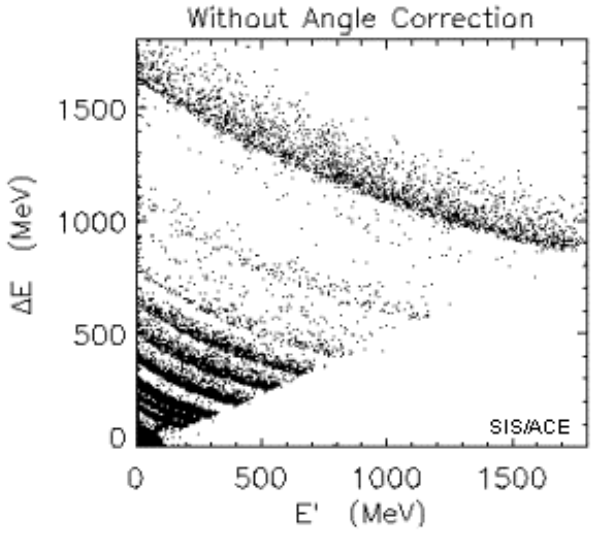


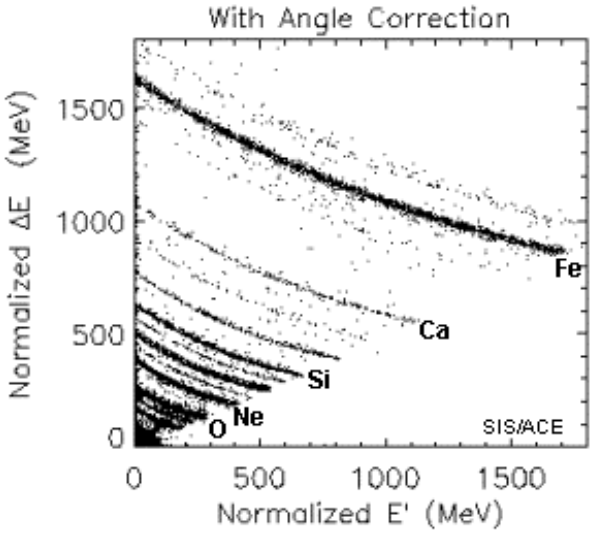
$R(E,M,Z) = (M/Z^2)R_p(E/M)$

$R(E',M,Z) = R(E,M,Z) - t \cdot \sec\theta$

Solving for M:

$M = Z^2 \cdot t \cdot \sec\Theta / [R_p(E/M) - R_p(E'/M)]$





LET Responsibilities

- Caltech
  - Low Energy Telescope development/test (lead)
  - Detector procurement
  - Flight software, including on-board algorithms (lead)
  - Electronics, including PHASIC and MISC
  - SEP integration & test
  - Scheduling
- JPL
  - LET development/test (assist)
  - GSE development
  - L1 detector testing
- GSFC
  - LET mechanical design and fabrication (e.g., detector mounts, telescope, and bracket)
  - LET thermal design
  - On-board algorithms (assist)
  - L2, L3 detector testing
- Space Instruments
  - Detector bias supply
  - Analog/Post-regulator
- U. C. Berkeley
  - Low voltage power supply

LET Personnel

- Tycho von Rosenvinge, SEP Coordinator, GSFC, tycho@lheamail.gsfc.nasa.gov
- Dean Aalami, Bias supply & analog/post-reg boards, SI, dean@spaceinstruments.com
- Jill Burnham, Layout support, Caltech, jill@srl.caltech.edu
- Rick Cook, Lead Electronics Engineer, Caltech, wrc@srl.caltech.edu
- Alan Cummings, Project Manager at Caltech, Caltech, ace@srl.caltech.edu
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- Mark Wiedenbeck, Detectors & LET testing, JPL, Mark.E.Wiedenbeck@jpl.nasa.gov

Applicable Documents

- Phase A Study for the IMPACT Investigation on STEREO, Volume 1: Tech. Sect., dated July, 2000
- STEREO Mission Requirements Document
- STEREO EMI/EMC Control Plan, JHU/APL 7381-9030
- STEREO Contamination Control Plan, JHU/APL 7381-9040
- STEREO Environments Definition, Observatory, Component and Instrument & Test Requirements Document, JHU/APL 7381-9003
- STEREO IMPACT Interface Control Document, JHU/APL 7381-9011
- STEREO Mission Risk Management Plan
- STEREO IMPACT Performance Assurance Implementation Plan (PAIP)
- STEREO IMPACT Configuration Management Plan
- LET-SEP_Central Interface Control Document, STEREO-CIT-009.A
- LET and SEP_Central Software Development Plan, STEREO-CIT-001.J
- LET and SEP_Central Software Requirements, STEREO-CIT-002.E
- LET Level 1 Data Format, STEREO-CIT-004.B
- LET Science Telemetry Data Frame Format, STEREO-CIT-003.4-2
- P24 MISC Microprocessor Users Manual, STEREO-CIT-005.A
- LET Functional Test Plan, STEREO-CIT-006.A
- SEP Sensor Suite Commanding and Users Manual, STEREO-CIT-007.A
- Caltech STEREO PHASIC Design Document, STEREO-CIT-013.A
- Documents and schematics are available at ftp://mussel.srl.caltech.edu/pub/stereo/docs , ftp://mussel.srl.caltech.edu/pub/stereo/CDR , or http://sprg.ssl.berkeley.edu/impact/dwc/

LET Reviews and Action Item Status

- STEREO IMPACT SEP/MAG Peer Review, 4/19/01
- STEREO IMPACT Project Site Visit to Caltech, 7/26/01
- STEREO IMPACT System Peer Review, 8/2/01
- Preliminary Design Review, 9/11/01
- Software Design Review, 4/30/02
- Contamination Peer Review, 10/24/02
- Responded to all action items from these reviews

EMC/Contamination/Environmental

Bias supply not synchronized

- Waiver EMC3A submitted and approved

Contamination

- SEP contamination control plan not received from Project as of 13 November 2002
- Project-supplied contamination control engineer visited and made informal recommendations
- JPL contamination control engineer visited, measured particulate counts in our assembly lab (room 5 Downs -> class 100K+) and on clean benches (Class 0), and made recommendations
- Plan is to use similar techniques, but with more attention to contamination issues, to assemble and test LET as were used on ACE SIS & CRIS which were largely assembled and tested in our lab
- LET L1 detectors will be stored in dry nitrogen and testing primarily done in a controlled room (clean room garments required for entry) – same as on ACE
- GSFC will do testing on L2 and L3 detectors in a clean environment
- LET flight units will be kept on clean benches; clean benches to be roped-off to cut down on foot traffic in the area – same as on ACE
- Personnel will use gloves and clean room garments – same as on ACE
- Will bag and purge during operations off the clean bench, e.g., accelerator testing, vibration, etc.
- Considering use of a clean tent if bagging for transfer between clean benches is frequent
- Will do bake outs according to Contamination Control Plan
- Will do final clean of exterior surfaces (to get from expected 500A level to 300A for delivery to JHU/APL)

EMC/Contamination/Environmental (continued)

- **Contamination (continued)**
  - **Incoming flight sensor assemblies (HET, SIT, and SEPT) will be unpacked on clean bench**
  - **JPL contamination control engineer will inspect external surfaces to establish incoming cleanliness**
  - **Will have 4 clean benches to handle all flight assemblies**
  - **Final clean of all may be necessary to get to 300A level for delivery**
- **Bake out of assemblies after sensors installed must be done at relatively low temperature (<35-40 C)**
  - **For LET & HET we are doing contamination test of detector & mount in next few weeks to assess outgassing of the sensitive detectors in their mounts**
  - **May have to pre-bake out the mounts before detectors are installed**
  - **Other parts can be baked out at higher temperatures before installing flight detectors**
- **Environmental**
  - **Test program defined by STEREO Environments Definition, Observatory, Component and Instrument & Test Requirements Document, JHU/APL 7381-9003 and by LET Verification Matrix**

LET Verification Plan

- **Detectors:**
  - L1's tested at Micron/Caltech/JPL; L2's & L3's tested at Micron/GSFC
  - Tests at Micron prior to delivery include random vibration and thermal cycle
  - Tests at Caltech/JPL/GSFC include noise & breakdown, thermal vacuum, and alpha particle response
  - Also will mockup housing/bracket and do acoustics & vibration tests
  - Thickness of L1 detectors will be measured with alphas
- **Hybrids (containing PHASIC chip):**
  - Electrical tests at room temp, hot, and cold
  - Radiation tests on prototype
  - Leak tests, etc. per Class H
- **Detector/MISC board:**
  - Originally two boards but now one single rigid-flex board
  - Board will be electrically tested over temperature

LET Verification Plan (continued)

- **Windows:**
  - **Vibration, acoustics, and thermal cycle in mockup**
- **LET System:**
  - **Many tests per Verification Matrix**
  - **Environmental tests will be in conjunction with HET & SEP Central**
  - **EMC/EMI at UCB**
  - **Thermal vac, acoustics, and vibration at JPL**
  - **End-to-end test at accelerator**
  - **Functionality testing with pulsers and alpha particles**
  - **Simulation of instrument response**

LET Verification Matrix

Verification Matrix for STEREO/IMPACT/SEP/LET

Revision Date: 11/08/02

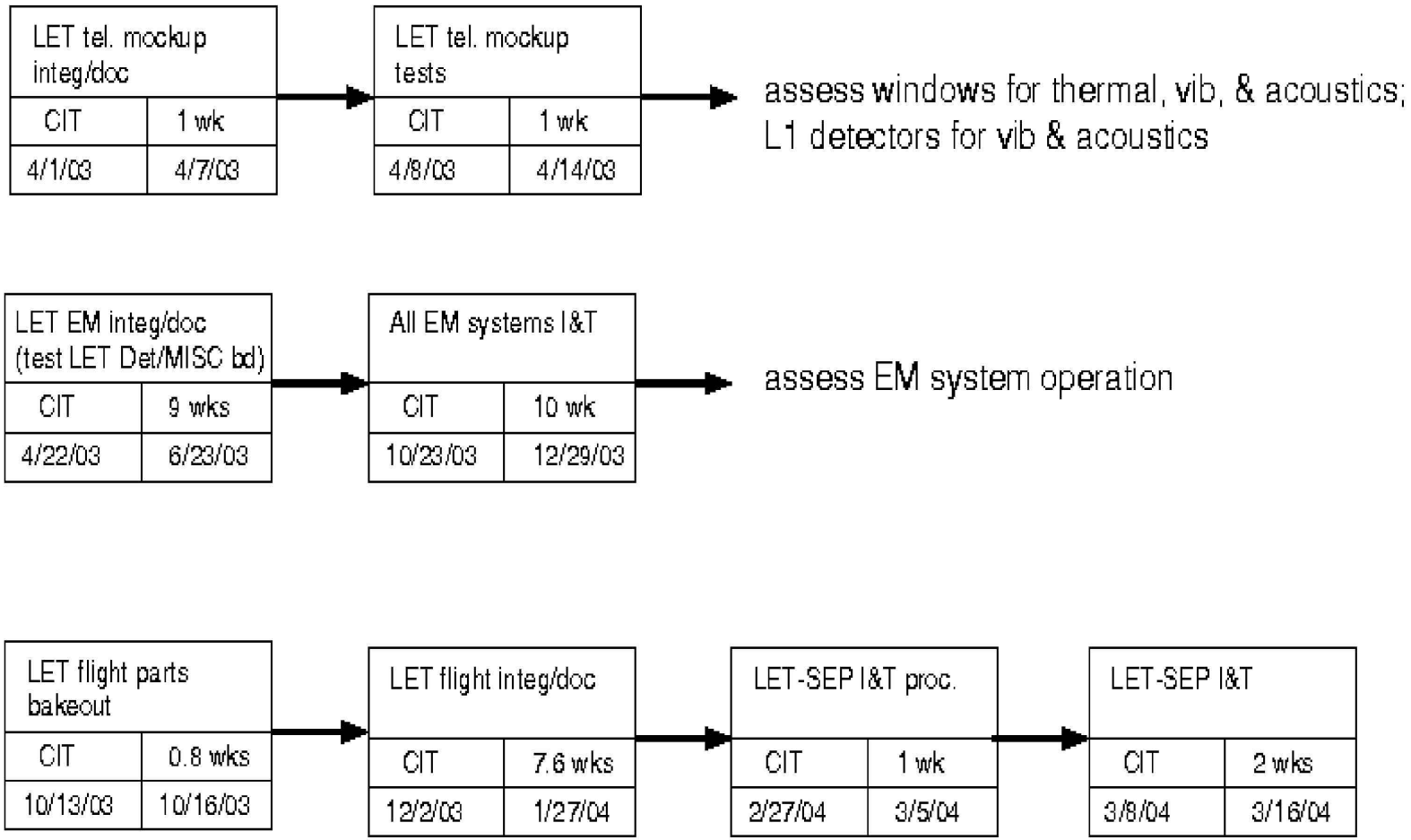
Revision Number: 5

Hardware Description		Tests																				
Level of Assembly	Item	Noise & Brkdown	Thermal vacuum	Alphas &/or particle accelerator	Elect. test, rm. Temp	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Pressure change	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Radiation	Leak	Bakeout	Contamination	Comments
C	Detectors, PT	X	X	X	X	X	X		X		X			X								X	Acoustics in BB with windows
C	Detectors, F	X	X	X	X	X	X		X					X									
C	Hybrids, PT				X	X	X												X				
C	Hybrids, F				X	X	X									X				X		X	Also standard class H tests
C	LET detector/MISC board, EM				X	X	X						X										
C	LET detector/MISC board, F				X																X	X	
C	Connectors, F																					X	
C	Windows, BB								X		X			X									Include L1 detectors for vib & acoustics
I	Instrument, F1		H	X	X	X	X	H	H	A	X	A	X		X	X	H	H			X	X	Protoflight levels for vib; full EMC at suite
I	Instrument, F2		H	X	X	X	X	H	H	A	X	A	X			X	H	H			X	X	Acceptance levels for vib; workmanship for EMC

Legend:

Level of Assembly	Unit Type		X =	Test required	
			A =	Analysis	
C = Component	BB =	Breadboard	H =	test at a higher level of assembly	
I = Instrument	EM =	Engineering Model			
	PT =	Prototype			
	PF =	Protoflight			
	F =	Flight			
	F1 =	Flight unit #1			
	F2 =	Flight unit #2			

LET Integration & Test Flow



Outline of LET Functional Test

- **The following functional test modules have been designed for use in ground and possibly in-flight testing (see LET Functional Test Plan, document no. STEREO-CIT-006.A).**
- **1) ADC Calibration**
  - **Use built-in test pulsers (5 values) and 8-bit DAC**
  - **Calibrate all 54 ADCs at 32 specified DAC levels**
  - **Takes 15 minutes at ~5 pulses/second**
- **2) Logic Test**
  - **Pulses detector combinations in specified patterns to test event identification, sorting, and prioritization for telemetry**
  - **Includes 1024 different detector combinations**
  - **Includes 64 pulse-height combinations from four DACs**
- **3) ADC Threshold Test**
  - **Measures all 108 ADC threshold levels by pulsing 256 selected levels and monitoring rate data**
  - **Also monitors noise performance**
  - **Takes ~10 minutes to run**

LET In-flight Livetime and ADC Calibration

These two tests can be run continuously in-flight and on the ground to monitor ADC stability and instrument livetime performance.

1) ADC STIM Mode

- **Completes full test of all 54 ADCs (32 DAC levels) in 8 hours**
- **Essentially same as ADC Functional Test but run at ~0.1 pulses/sec**

2) Livetime Monitor

- **Stimulates 12 different event types to at fixed rate of ~2/sec**
- **These events compete with normal rates for on-board analysis**
- **Monitors livetime to <0.3% accuracy per hour at "background" event rates up to 10^4/sec**

Risks, Issues, & Mitigations

- **L1 detector fabrication technique is new**
  - **Started a plan B approach as a backup using conventional fabrication method (with likely poorer performance)**
- **Windows covering L1 detectors on Sun-facing side may be thermally stressed**
  - **Thermal analysis indicates 60 deg temperature swing**
  - **Window is proposed to be 8 um Kapton with vapor deposited gold coating on inside and ITO silver conductive composite on outside**
  - **WIND EPACT instrument had nearly identical windows but it saw Sun only 50% of the time**
  - **ACE SIS stared at Sun (always within about 45 deg) but had larger-area, thicker, and additional windows (25 um, 8 um, and 8 um)**
  - **Telescope design will prevent rupture of one window from light contamination of other L1 or L2 detectors**
  - **Thermal tests of prototype windows will be conducted**
- **LET "Ferris Wheel" is on a bracket and may have problems with vibration**
  - **Vibration analysis underway**
  - **Vibration tests of mockup will be conducted**
- **PHASIC chip is no longer high risk item**
  - **2nd version in process**
  - **1st version good enough to keep design tasks and tests going; possibly could be used**
  - **1st version passed radiation tests**
  - **3rd run possible if 2nd version fails – not thought to be likely**

Risks, Issues, & Mitigations (continued)

- **Layouts might not fit in chosen board sizes**
  - **Schematics and layout assessments have been done but not actual layouts**
  - **Impact would be to make any affected housing slightly larger**
  - **Weight would increase accordingly**
  - **Should know by end of 2002 for questionable one**
  - **Schedule impact should not be major as final housing drawings are not complete**

LET Milestones

• CDR	11/22/02
• PHASIC version 2 chips received from vendor	12/31/02
• LET L1 detector decision date	1/31/03
• Flight hybrids tested and ready	3/25/03
• LET Detector/MISC EM board tested	6/23/03
• LET Detector/MISC flight boards tested	10/28/03
• LET detectors tested & selected	11/25/03
• EM sytems test complete (with SEP Central + others)	12/29/03
• LET flight mechanical parts ready	9/1/03
• LET telescope flight integration finished	1/27/04
• LET-SEP integration & test finished	3/16/04
• Remaining schedule addressed in SEP I&T section	

Open Issues/Concerns

- See Risks & Mitigations slide
- Schedule needs to be re-baselined
- Budget is tight with no reserve held at Caltech