HET/SIT Flight Software and GSE

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Relevant Documents

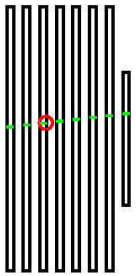
- STEREO HET CPU24 Flight Software Requirements Document
- STEREO SIT CPU24 Flight Software Requirements Document
- STEREO SEP LET and Central MISC Flight Processors Software Requirements Document
- STEREO SEP HET and SIT CPU24 Processors Flight Software Development Plan
- CPU24 MISC Documentation (Bob Baker)
- HET PHA Test Software (Tom Nolan)
- Serial Port Interface to TCP/IP (SPiT) Programmer's Reference (Tom Nolan)
- Caltech PHA ASIC User's Manual (Rick Cook)
- STEREO HET Telemetry Formatting (Don Reames)
- HET to SEP Central Interface Control Document (Caltech)
- SIT to SEP Central Interface Control Document (Caltech)
- SEP Sensor Suite Commanding and Users Manual (Caltech)
- STEREO MOC to POC and to STEREO Science Center ICD (APL)

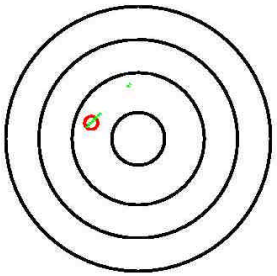
Relevant Documents … Cont'd

- **Many of the relevant documents and the PowerPoint presentations for the HET/SIT Software Requirements and Software Design Peer Review may be found at**

  http://epact2.gsfc.nasa.gov/STEREO/docs.html

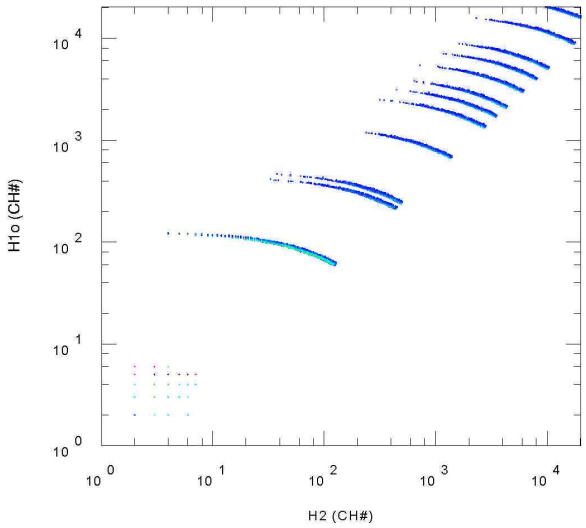
HET Simulations

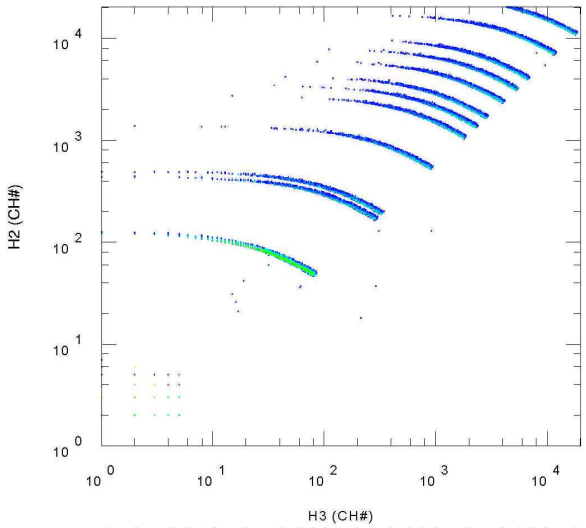


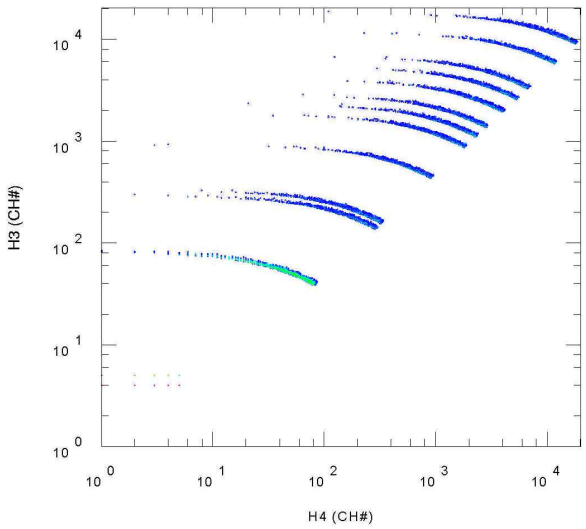


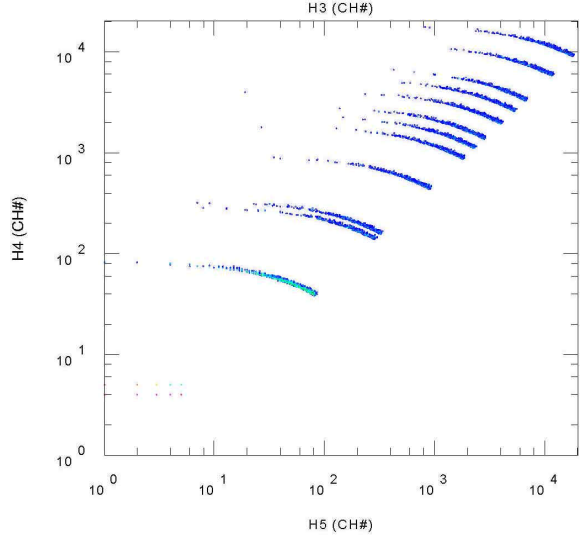
Particle= 5, Z= 2, A= 4, KE= 34.5 MeV/n
theta= 9.3 degrees
phi= 134.7 degrees
xa=-0.79 cm, ya=-0.16 cm, za= 0.00 cm
xb=-0.39 cm, yb=-0.57 cm, zb=-3.50 cm
Stops in H5a: xs=-0.24 cm, ys=-0.71 cm, zs=-4.76 cm

HET Response

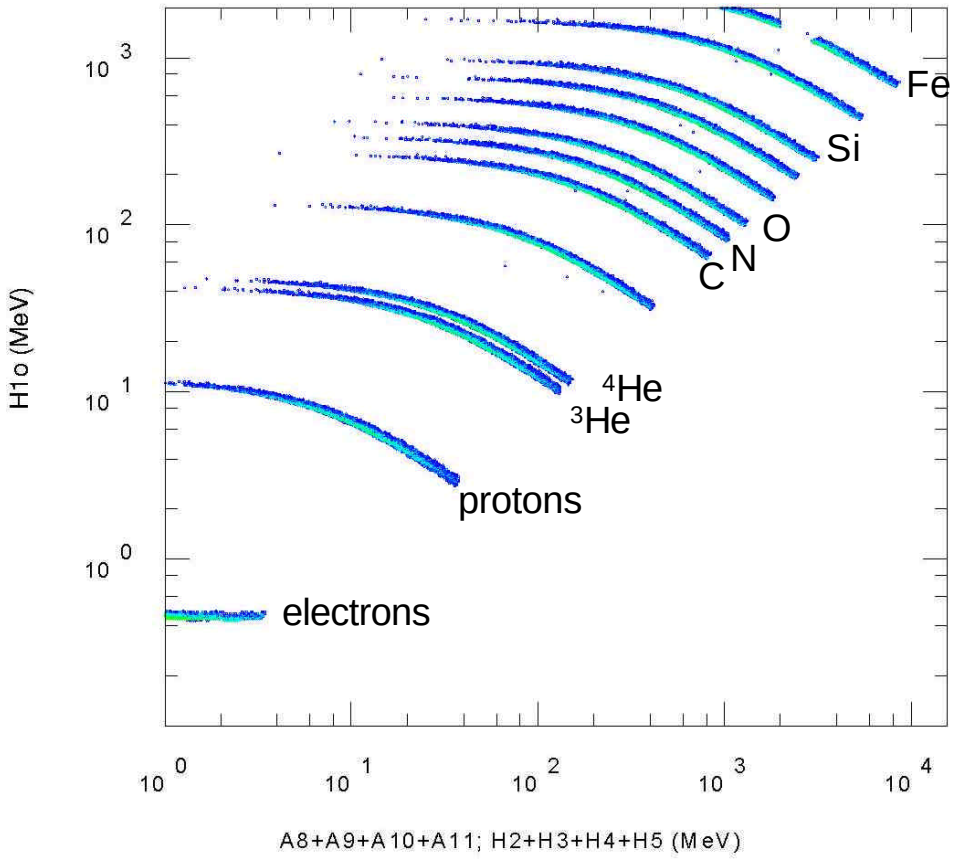




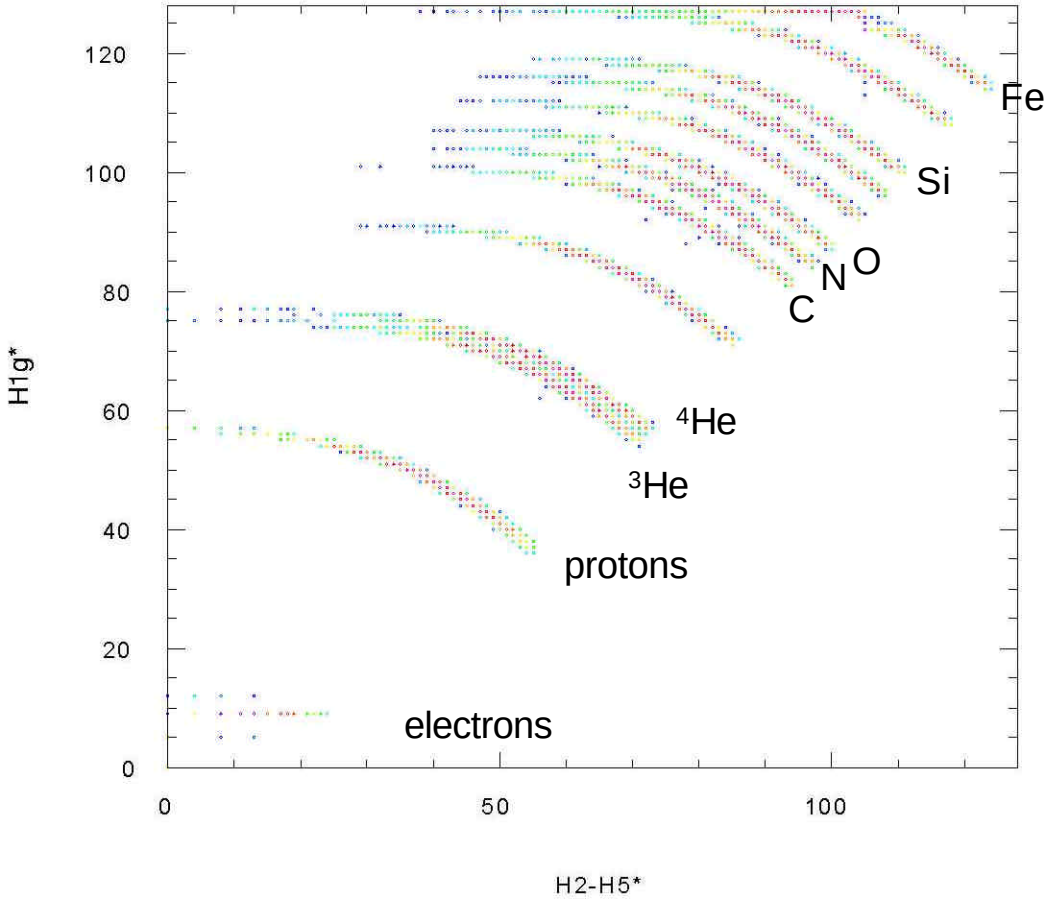




HET Composite Response



HET Composite Log Response



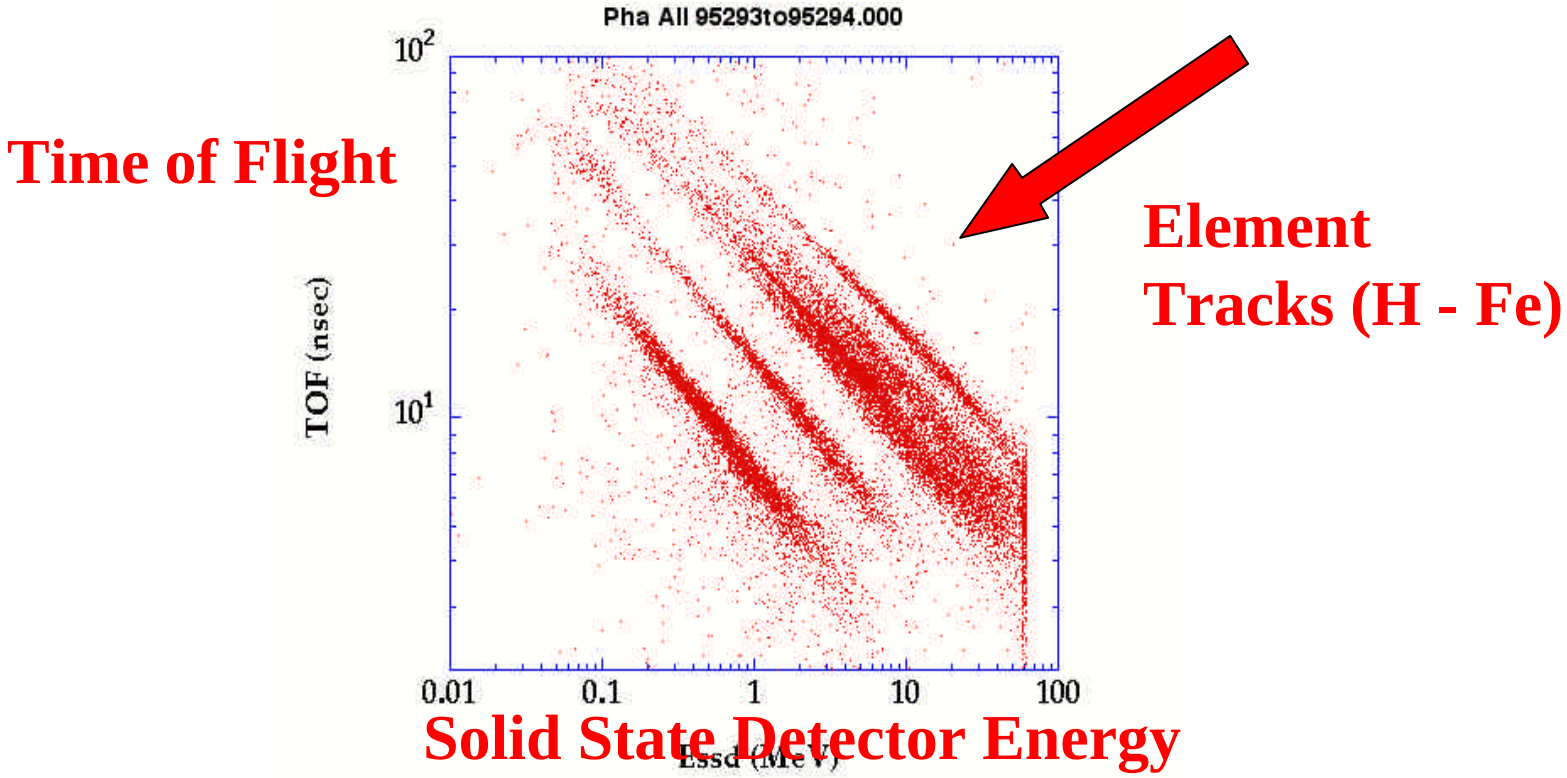


Figure 2. TOF versus the total kinetic energy for solar energetic particles, measured during the October 1995 event. The pulse height analysis (PHA) data are from the WIND/STEPS sensors. The SIT E scale values will extend up to about 160 MeV, considerably higher than in this figure.

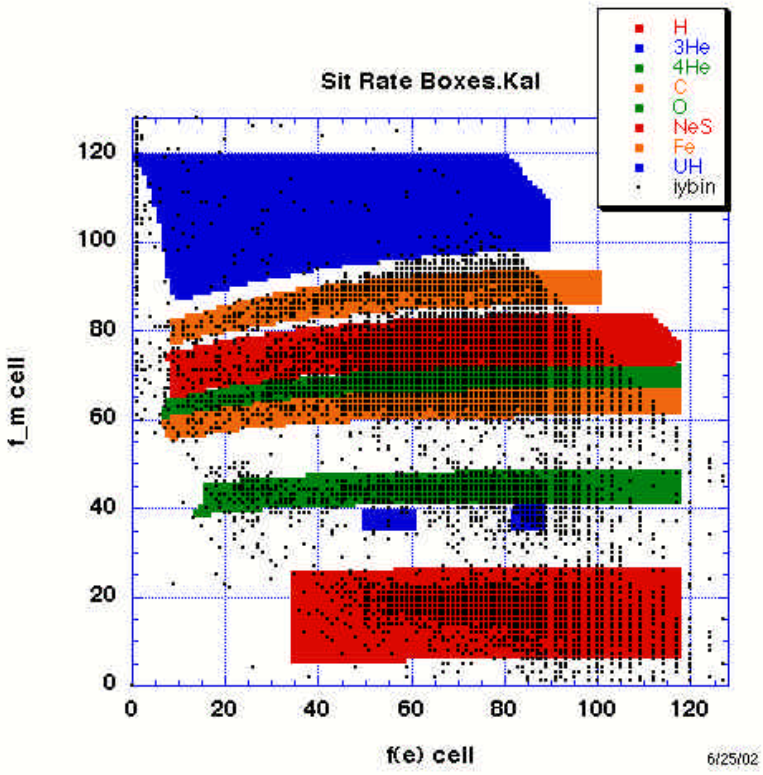


Figure 3. Valid Events (black dots) superposed on typical rate bin grid. Different elements have different colors; within each element are a number of separate rate bins corresponding to energy windows of width about 40%. Note: PHA data and bin alignment is not optimized in this figure; also SIT data will extend to higher f_e cells for heavy nuclei due to larger dynamic range on the solid state detector than seen with STEP instrument.

Matrix Rates

Caltech ASIC Test Chip

- **Testing of PHASIC for HET (Not Used By SIT)**
  - **Test bed supplied by Cal Tech includes ASIC and all support components, including CPU24 MISC, mounted on a PC board, but without the hybrid package**
  - **Software environment for testing is very flight-like (commands, data, interrupts) except no particle binning**

CPU24 Design Status

- CPU24 is the GSFC MISC
- CPU24 (v2) is based on Cal Tech MISC11 design
  - Data UART, live time counter, sync signal interface added
- Design coded in Verilog
  - Synthesized using Synplify Pro 6.2.4
  - P&R using Actel Designer 4.0.4.4
  - Usage: 81% of S cells, 65% of C cells of A54SX72A
- Running on Cal Tech Test Board
- Users Manual Written

Top Level Requirements for HET CPU24 Code (1)

- Boot up CPU24
- Download/decompress tables and CPU24 code from SEP Central EEPROM
- Receive Commands from SEP Central
  - Receive and handle commands to configure PH ASICS (846 bits each)
  - Receive and handle commands to patch RAM
  - Receive and handle TBD miscellaneous commands
  - Echo commands to SEP Central
- Read Hardware Rate Counters
- Read PH Events from ASICs
- Queue PH Events According to Types
- Process PH Events into Software Counters (on-board particle identification … described later)
- Identify High Rate Conditions (switch H1o to low gain only; switch back depending upon H1i rate; switch only on 1-minute boundaries)

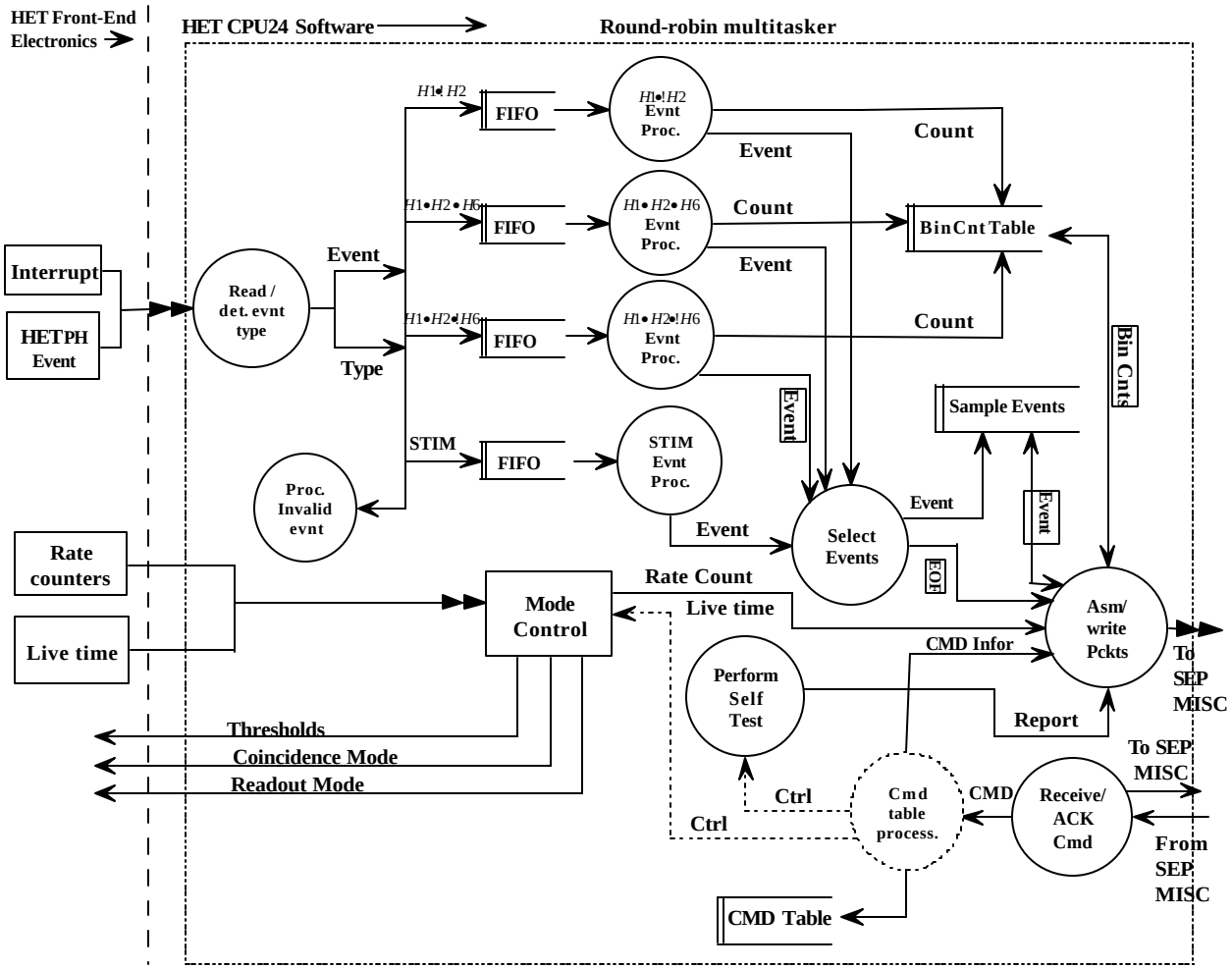
Top Level Requirements for HET CPU24 Code (2)

- Acquire Housekeeping Data and Readout to SEP Central
- Generate On-board Pulser Events (set STIM bit)
- Write Out Telemetry Packets Once Per Minute
  - Selected PHs (compress 23 bit ASIC pulse height to 16 bits)
  - Software Counter Rates (24 to 16 bit rate compression)
  - Hardware Rates (24 to 16 bit rate compression)
  - Housekeeping
  - Beacon Data
  - Include Checksum for Each Packet
- SEP Central expects HET Data Packets Only During 100 ms Windows Following 1- Second Timer Pulses 0, 3, 6, …, 57 of Each Minute (0 or more packets per window; preferably spread out over 1 minute interval)
- Control Operational Heater?

Top Level Requirements for HET CPU24 Code (3)

- **Background Tasks**
  - **STIM Pulser Sequence**
  - **Check checksums for on-board code and tables**
  - **Slow readout of on-board code and tables to the ground**
  - **Refresh PH ASIC command state once every minute**
  - **Monitor each preamp output voltage and adjust leakage currents as necessary to keep in specified range**
- **HET is assigned 6 data packets (272 bytes each, including 12 bytes of CCSDS header) for readout once per minute. In addition, Beacon Data, Command Echoes, and Housekeeping Data are combined into corresponding SEP Central packets.**
- **HET Beacon Data:**
  - **protons: 13-30 Mev**
  - **protons: 30-50 MeV**
  - **protons: 50-100 MeV**
  - **He: 13-30 MeV/n**

CPU24 Processing Flow



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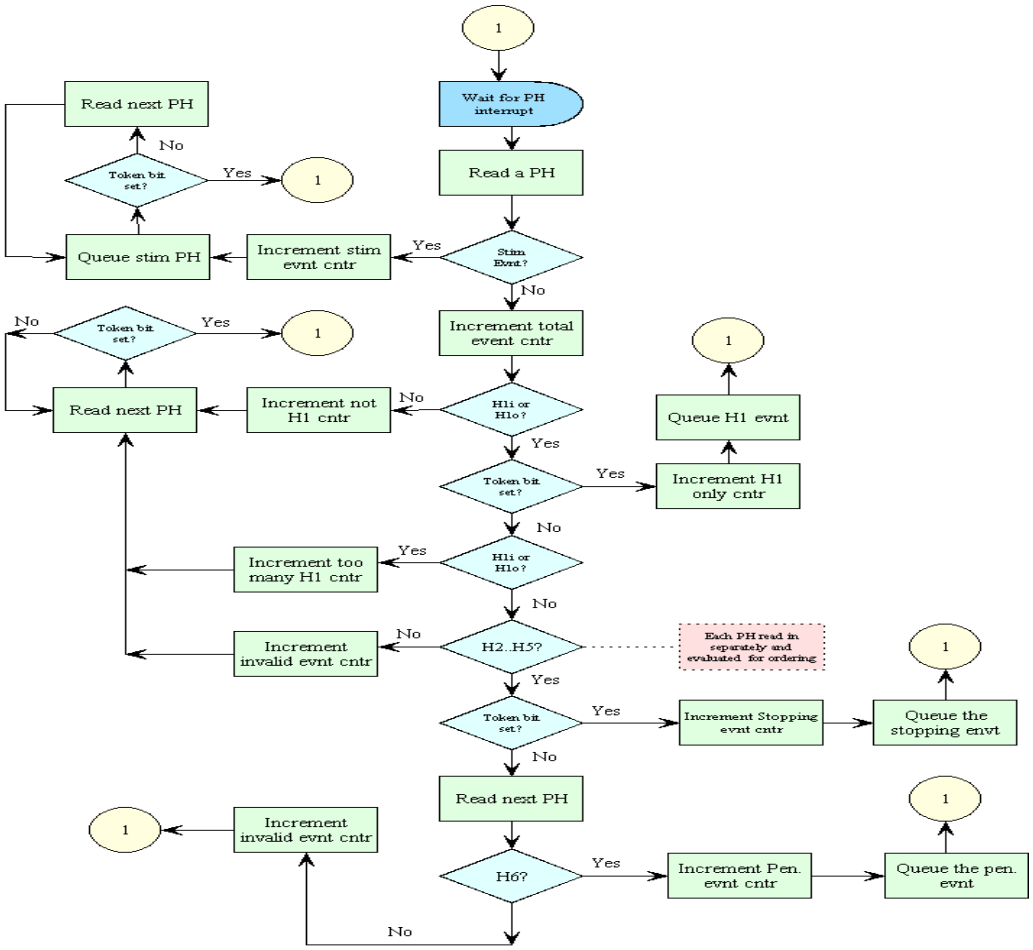
Science Data Acquisition: Pulse Height Events

- **Triggered by the PH interrupt**
- **PH events are queued into four different FIFOs:**
  - **Particles stopping in H1 (inner and outer)**
  - **Particles stopping in H2-H5**
  - **Particles penetrating all of HET**
  - **PH events created by the on-board pulser (STIM events)**
- **Count number of pulse height events read into CPU24**

HET Event Queuing Algorithm

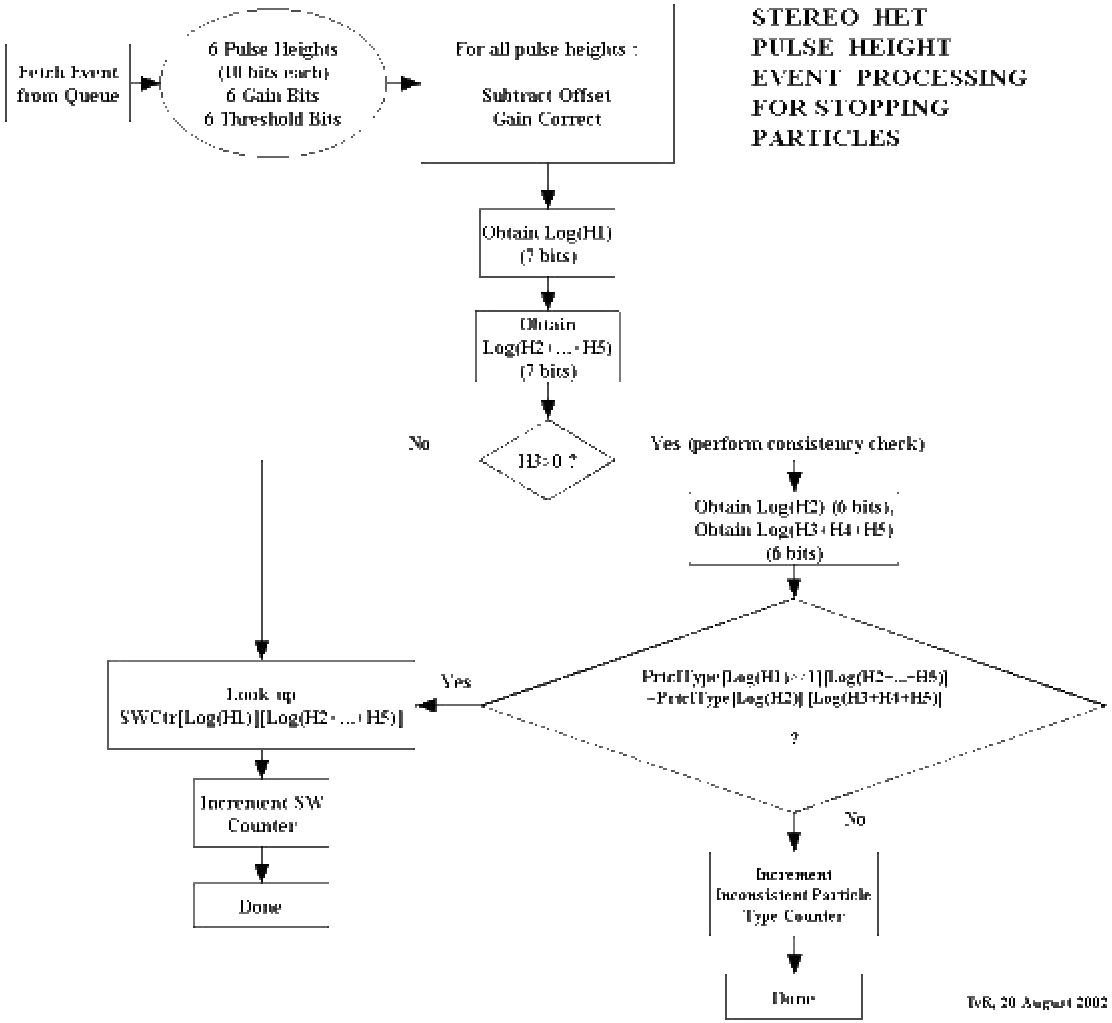
This algorithm has been successfully implemented in the HET CPU24



Science Data Processing

- **Select PH events from each class type queue**
- **Determine species and energy**
- **Increment the corresponding software rate counter**
- **Respond to the EOF reset**
  - **Reset software counters**
  - **Reset hardware counters**
  - **Clear event queues**

HET On-Board Pulse Height Processing



Rate Counter Categories

- Total events processed (STIM events not included)
- Queued H1 events (inner and outer)
- Queued stopping events (H2-H5)
- Queued penetrating events (H1-H6)
- Invalid events
  - No H1 (inner or outer)
  - Incorrect ordering of pulse heights
  - Duplicate H1s
  - H1i and H1o
- Inconsistent Particle Type Counter
  - consistency check for particles reaching at least H3
  - particle type should be same for H1 vs H2+H3+H4+H5 as for H2 vs H3+H4+H5
- Singles Rates (counted in ASIC)

HET Science Event Data Processing

- **Software count binning according to species and energy intervals**
- **HET: 2 log lookup tables**
  - **Delta E**
  - **Residual E**
- **Memory required**
  - **log tables: 1 Kwords**
  - **Processing and binning of each particle:**
    Stopping Particles: 20 KW
    Penetrating Particles: 4 KW

HET Stopping Particles
Species & Energy Intervals

MeV/n	H&^{4}He	^{3}He	C	O	Ne	Mg	Si	Fe
13-15	X							
15-	X							
17-	X	17-21						
19-	X							
21-	X	21-27						
24-	X							
27-	X	27-33	x					
30-	X		x	x				
33-	X	33-40	x	x	x			
36-	X		x	x	x			
40-		40-47	x	x	x	x	x	
45-			x	x	x	x	x	
52-			x	x	x	x	x	x
62-			x	x	x	x	x	x
74-				x	x	x	x	x
87-					x	x	x	x
98-						x	x	x
109-							x	x
119-								x
140-163								x
Bin-Count	20	5	8	8	8	7	8	8

electrons: 0.7-1.4, 1.4-2.8, and 2.8-4.0 MeV

78 Stopping particle bins total, including 3 background bins

SIT Science Data Processing

A preliminary version of the SIT particle identification algorithm has been successfully tested on a CPU24 MISC.

Software Development Approach

- Scientists provide algorithms in C code (HET) or FORTRAN (SIT)
- Scientists provide simulated data for testing on-board code
- Programmers translate C/FORTRAN to MISC assembly language
- Scientists/engineers/programmers test on-board software
- Test Plan/Problem Reporting and Tracking
  - See sections 3.7.2 and 3.7.4 of FSWDP
- Configuration Management (See section 3.7.3 of FSWDP)

On-Board Software Resource Requirements

EEPROM Requirements (HET):

- 25 KB tables
- 24 KB code
- ---
- 49 KB Total

EEPROM Requirements (SIT):

- 27 KB tables
- 24 KB code
- ---
- 51 KB Total

RAM Requirements(HET):

- 8 KW code
- 10 KW data
- 25 KW tables
- ---
- 43 KW Total

RAM Requirements(SIT):

- 8 KW code
- 10 KW data
- 20 KW tables
- ---
- 38 KW Total

Total CPU usage(HET and SIT): 18% at 1000 Hz event rate

60% at 5000 Hz event rate

HET/SIT GSE Configurations

- GSE to ASIC Test Board (GSFC)
- GSE to HET CPU24 (GSFC) or SIT CPU24 (U of MD)
- GSE (via TCP/IP or data file) to Caltech GSE to S/C simulator to IDPU simulator to SEP Central to HET/SIT CPU24 (Caltech)
- GSE (via TCP/IP or data file) to Caltech GSE to IMPACT POC A or POC B to MOC to S/C to IDPU to SEP Central to HET/SIT CPU24 (APL and Post-launch)

Top Level requirements for HET/SIT GSE Code

- Boot ASIC Test MISC (HET)
- Boot HET/SIT CPU24 in Absence of SEP Central
- Upload on-board tables and HET/SIT Code in Absence of SEP Central (or to SEP Central)
- HET Only: Provide User-Friendly Interface for Formatting ASIC Commands (846 bits each!)
- Send Commands via ASCII Hex; for HET, retain memory of current ASIC command state
- Display PH Data
- HET: Display STIM Event Data
- Display Rate Data
  - Decompress 16 bits to 24 bits

HET/SIT Software Status

- HET/SIT Software Requirements and Software Design Peer Review was held August 24, 2002.
- Responses have been provided to all RFAs from this review
- A preliminary version of the SIT on-board particle identification algorithm has been tested successfully against simulated particle events
- Preliminary telemetry formats have been defined for both HET and SIT
- MISC and GSE software has been completed for configuring and testing the performance of a sample PHA chip (PHASIC)
- The event-queuing portion of the HET on-board software has been written and tested
- The stopping-particle algorithm for HET has been coded in C and will shortly be transferred to MISC assembly code