STEREO IMPACT POWER SUPPLIES

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SPECIFICATION EXTRACT

Voltage	IDPU	mA	WATTS		SURGE		CAPACITANCE
12.8		15	0.19				
	SURGE	100			1.28	Watts	
-12.8		15	0.19				
	trimmable +50 to+140	0					
5		15	0.08				
-5		15	0.08				
5		**600**	3.00				
	SURGE	**700**			3.50	Watts	
	2.5	**40**	0.10				
			3.63	Watts	8.41	Watts w/ surge	

Voltage	SWEA	mA	WATTS		SURGE		CAPACITANCE
	trimmable +50 to+140	0					
+28		13	0.36				
+12		10	0.12				
	SURGE	100			1.20	Watts	
-12		8	0.10				
+5		12	0.06				
-5		12	0.06				
5		**20**	0.10				
	2.5	**40**	0.10				
			0.90	Watts	2.10	Watts w/ surge	

Voltage	PLASTIC	mA	WATTS		SURGE		CAPACITANCE
+12		414	4.97				25uF
-12		164	1.97				20uF
-5		170	0.85				20uF
+5		731	3.66				30uF
	2.5	105	0.26				25uF
			11.70	Watts	(includes test port)		

		Watts		Capacitance
+3500 V, sync		0.00		
Voltage	SEP mA			
+13.0	31	0.40		
-13.0	13.4	0.17		
+6.0	175	1.05		
-6.0	11	0.07		
-5.2	**108**	0.56		
5.1	**12**	0.06		
3.4	**189**	0.64		
2.6	**66**	0.17		
2.6	**10**	0.03		
5.3	**12**	0.06	SEPT NS	
5.6	72	0.40		
-5.1	0.5	0.00		
2.6	**10**	0.03		
5.3	**12**	0.06	SEPT E	
5.6	72	0.40		
-5.1	0.5	0.00		
		4.12	Watts	

CONTROLLING DOCUMENTS

- IMPACT/PLASTIC Power Converter Requirements

- Performance Assurance Implementation Plan

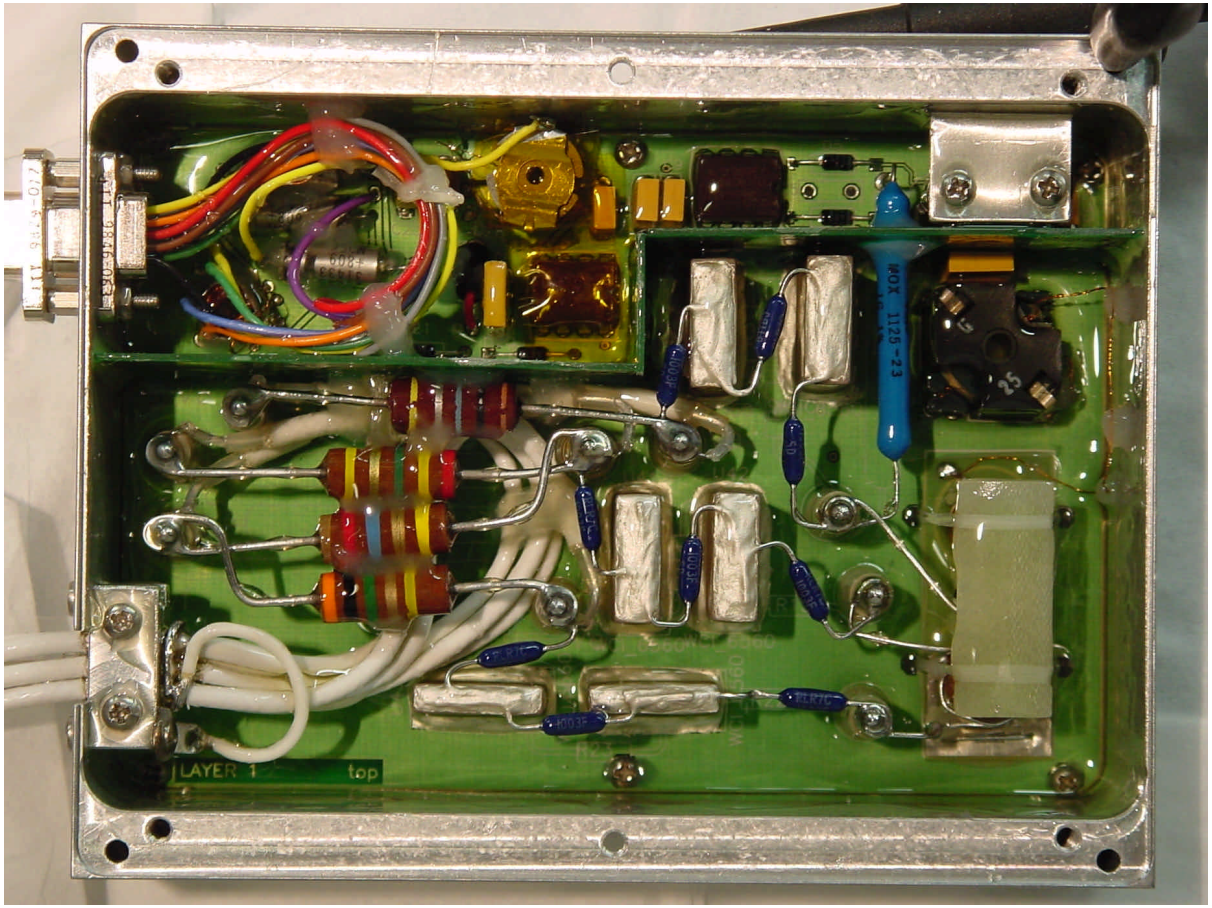
- STEREO EMC Control Plan and EMI PerformanceRequirements Specification, 7381-9030

MASS AND POWER ESTIMATES

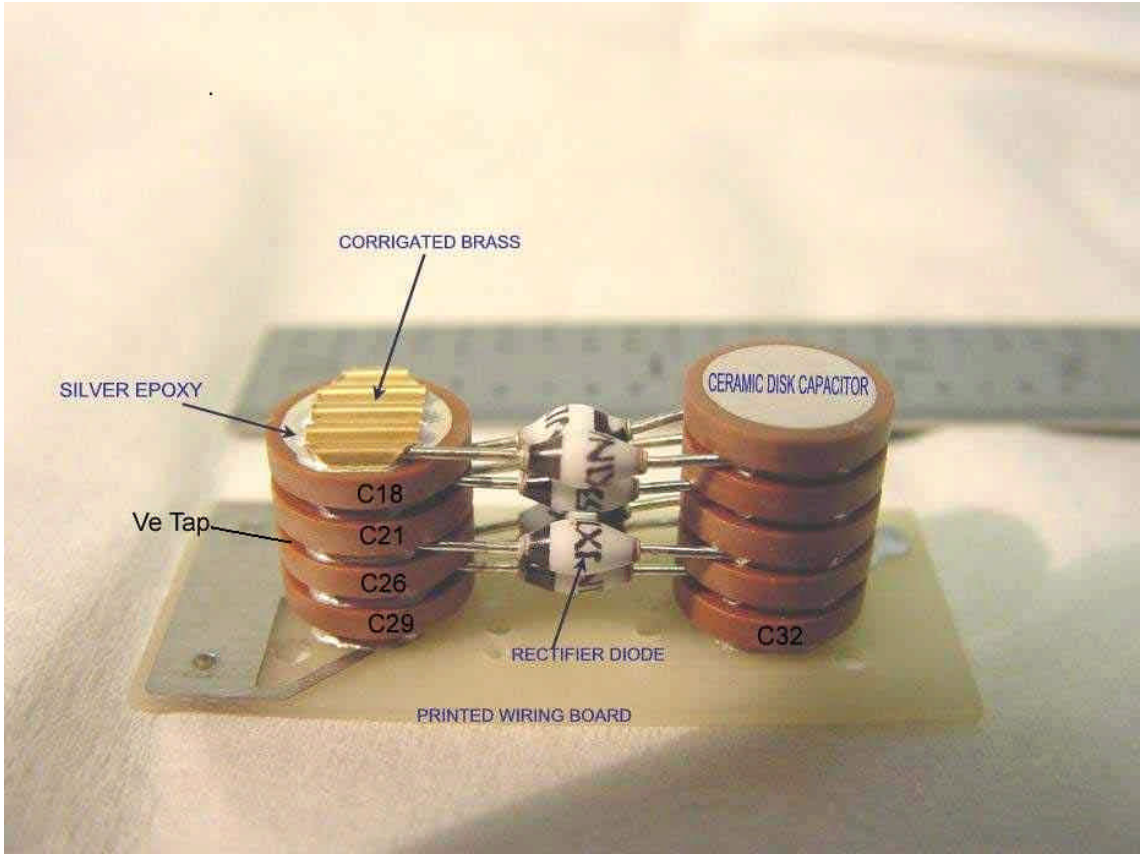
	IDPU	SIT HV	SEP	SWEA	PLASTIC
ASS EXTMATE, gm	400	330	480	350	200
OWER ESTIMATE, Watts incl surge	12	1	5.7	3	16.7

STEREO IMPACT HVPS (SIT)

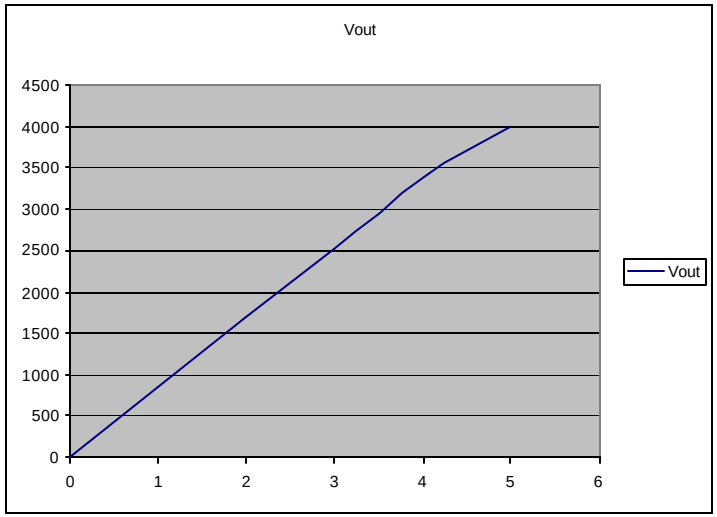
STEREO SIT HVPS ETU

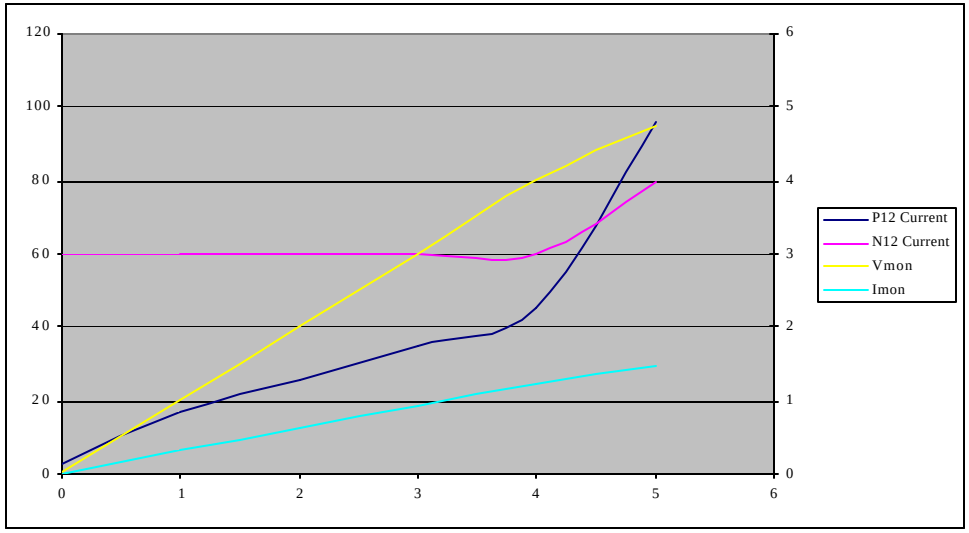


HVPS MULTIPLIER STACK

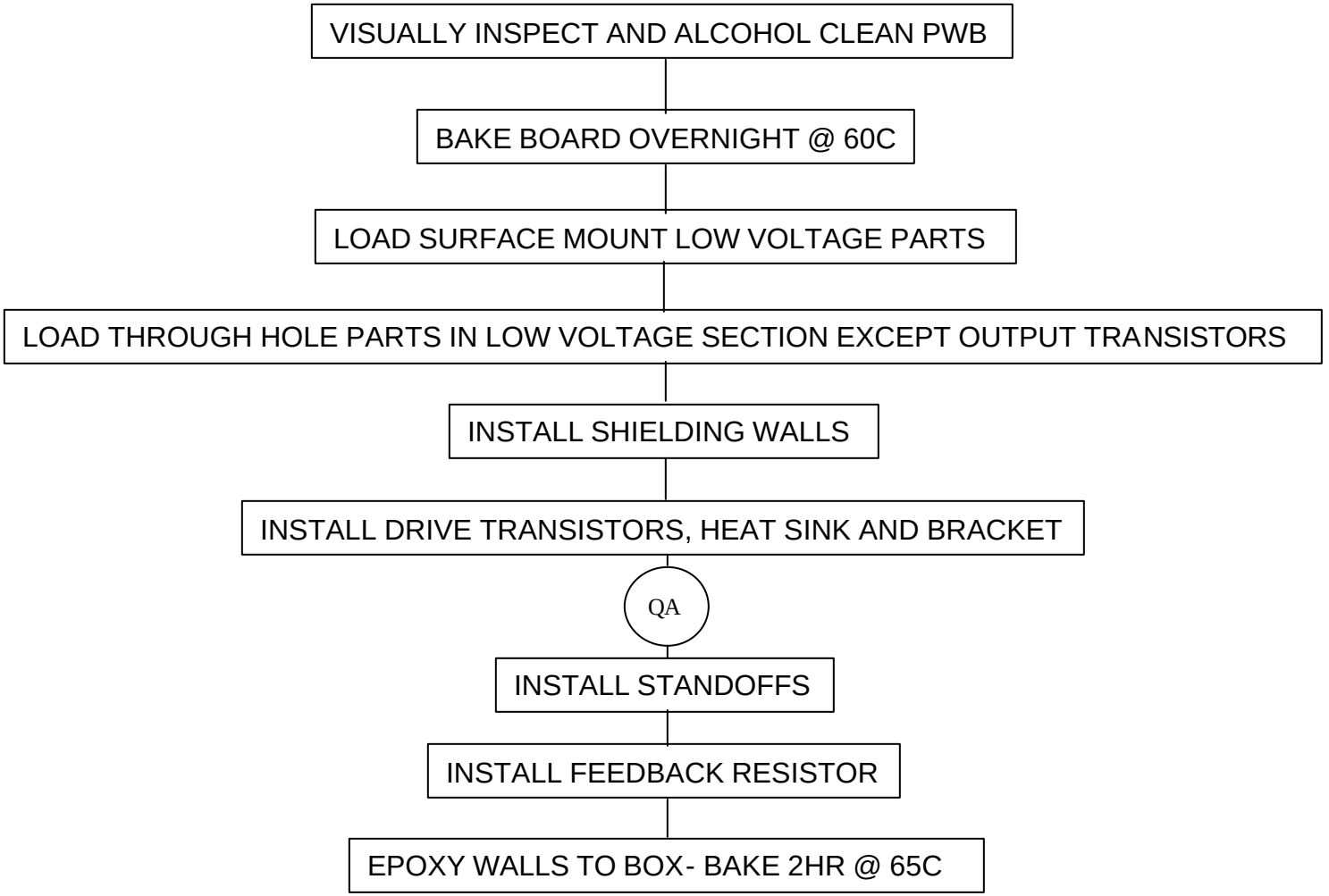


SIT HVPS ETU TEST DATA

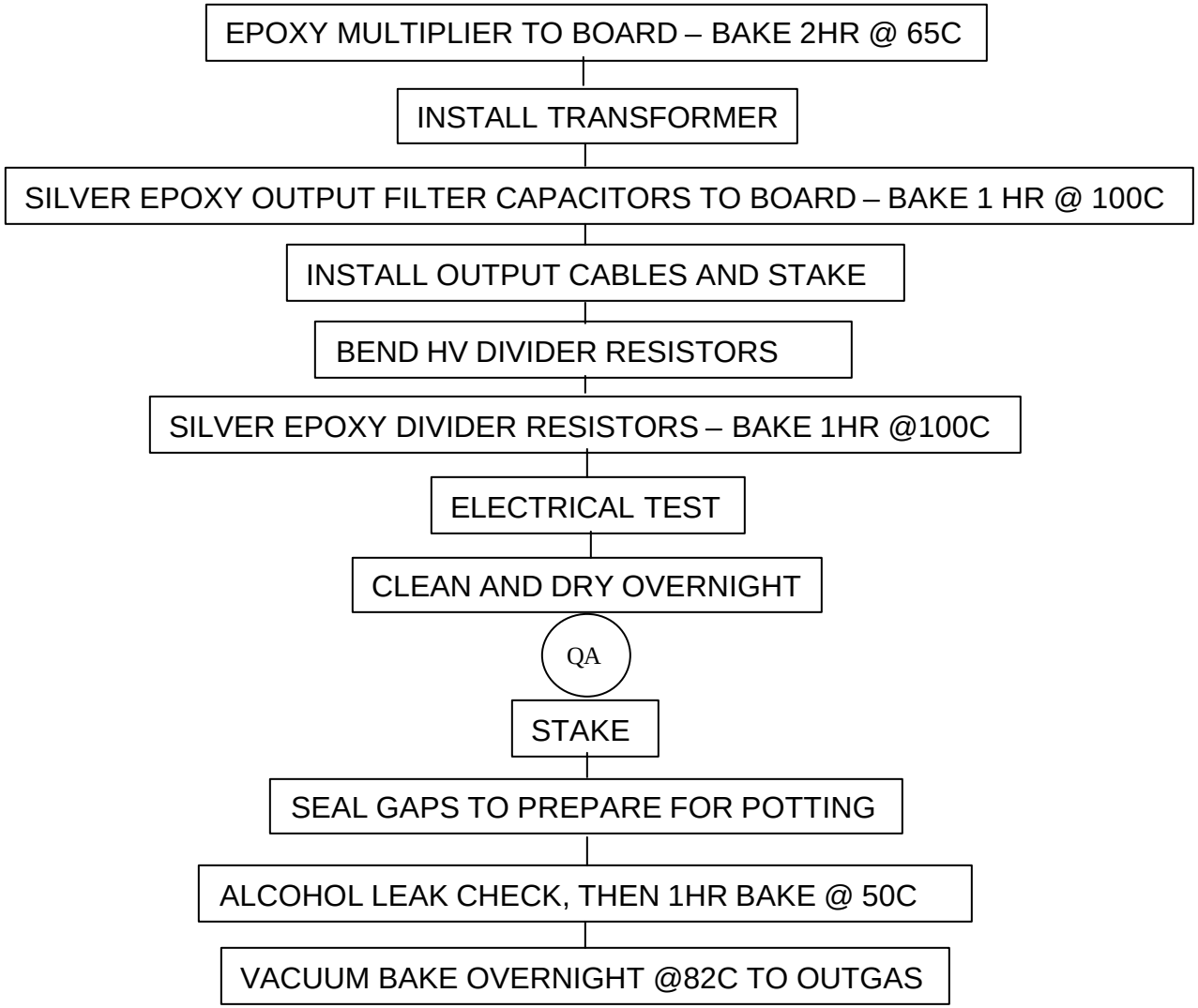




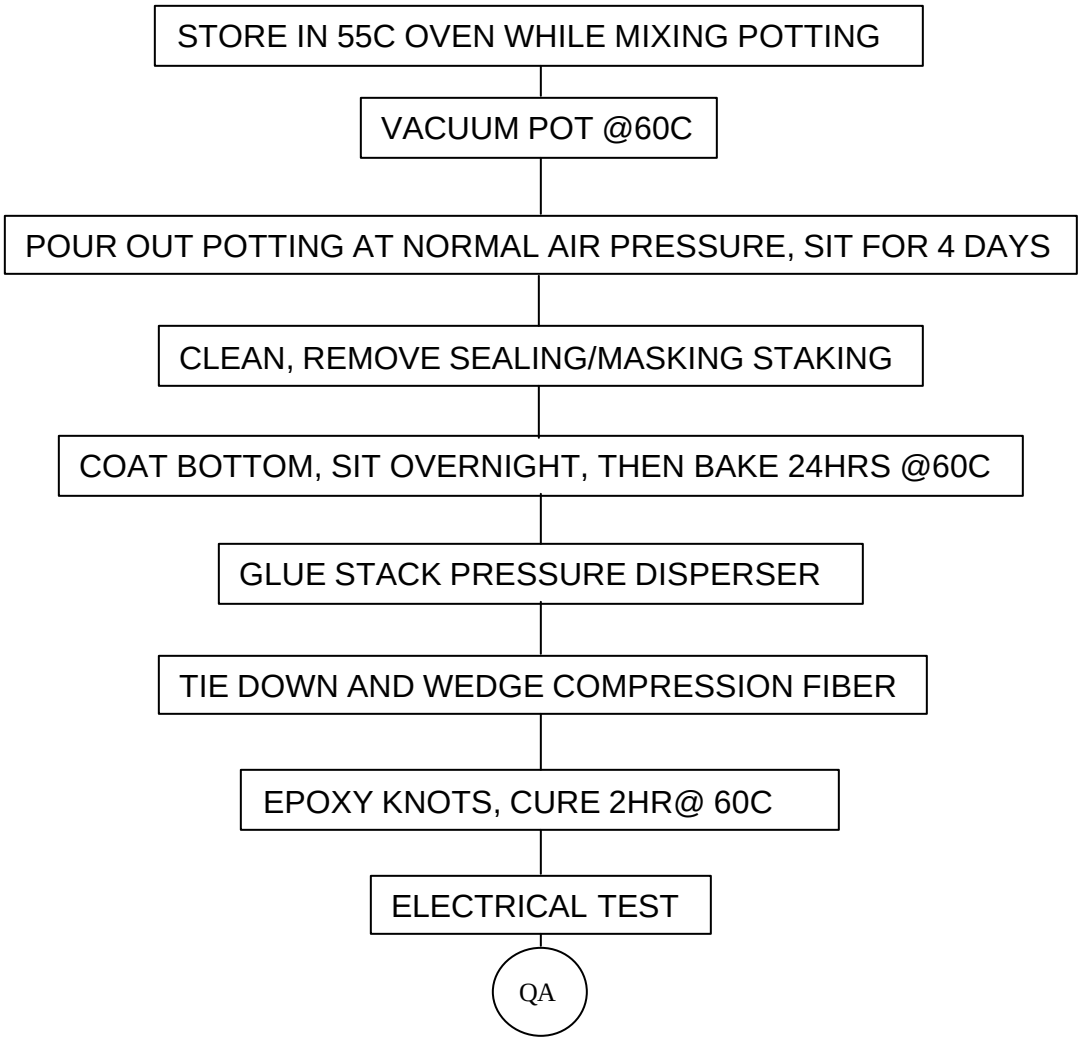
HIGH VOLTAGE MANUFACTURING FLOW



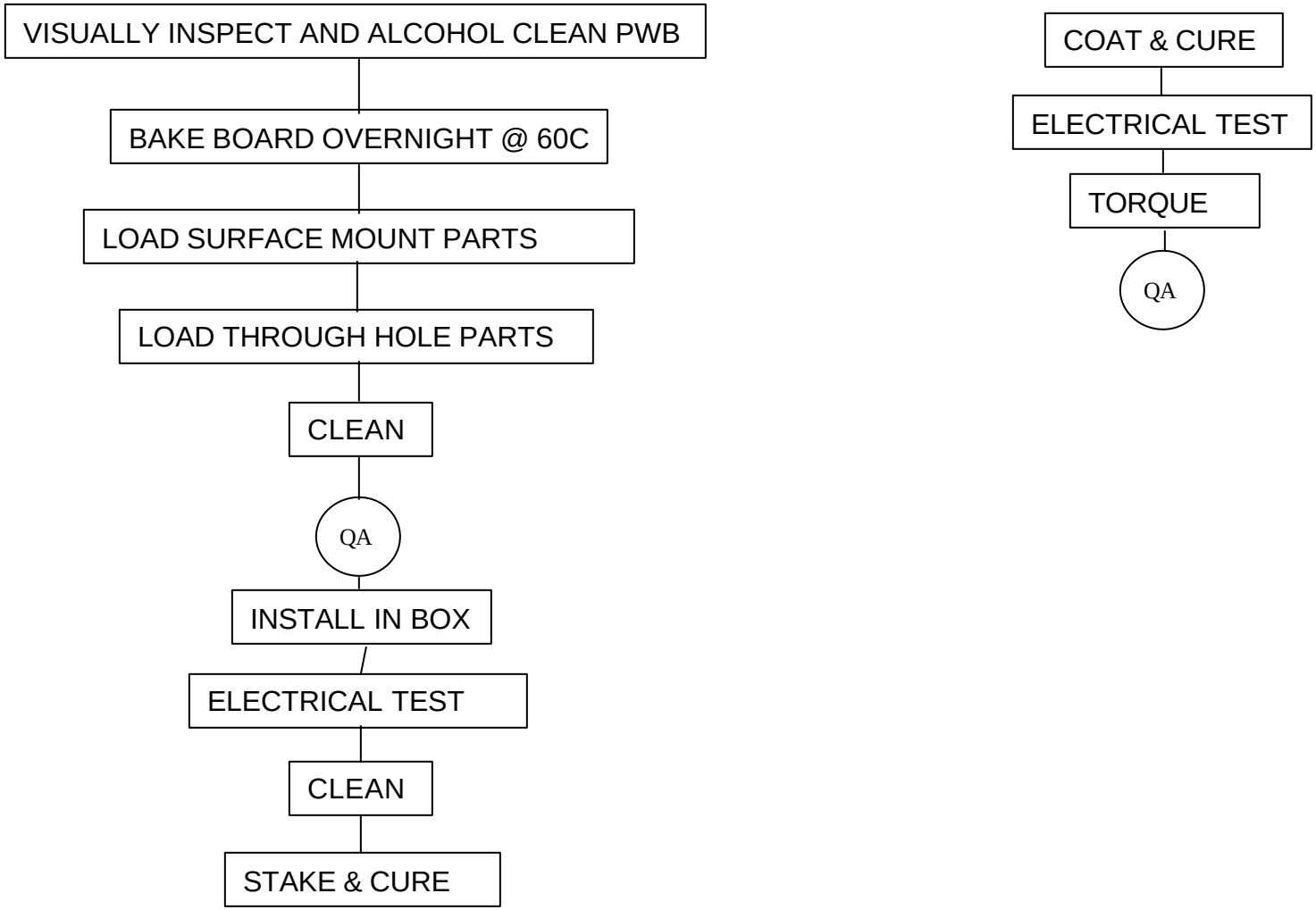
HIGH VOLTAGE MANUFACTURING FLOW



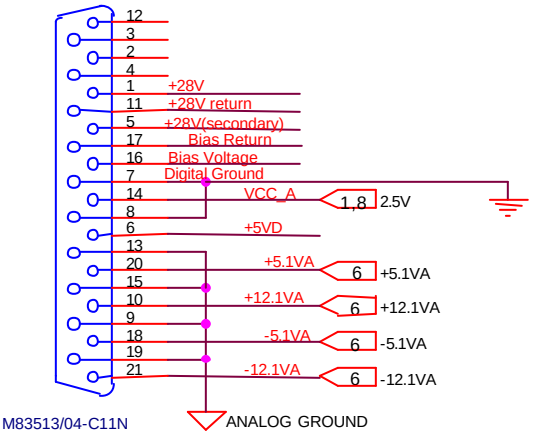
HIGH VOLTAGE MANUFACTURING FLOW



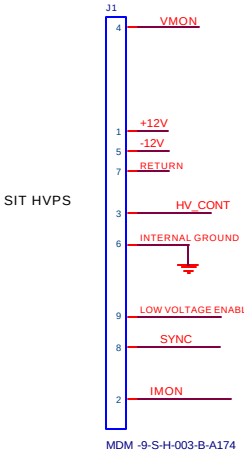
LOW VOLTAGE FLIGHT MANUFACTURING FLOW



INTERFACES

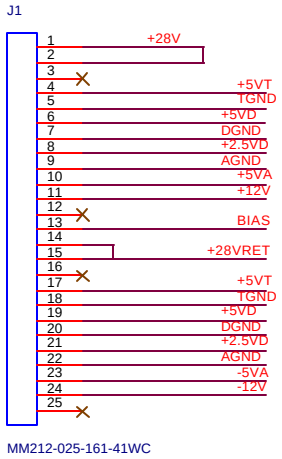


SWEA



SIT HVPS

SIT HVPS

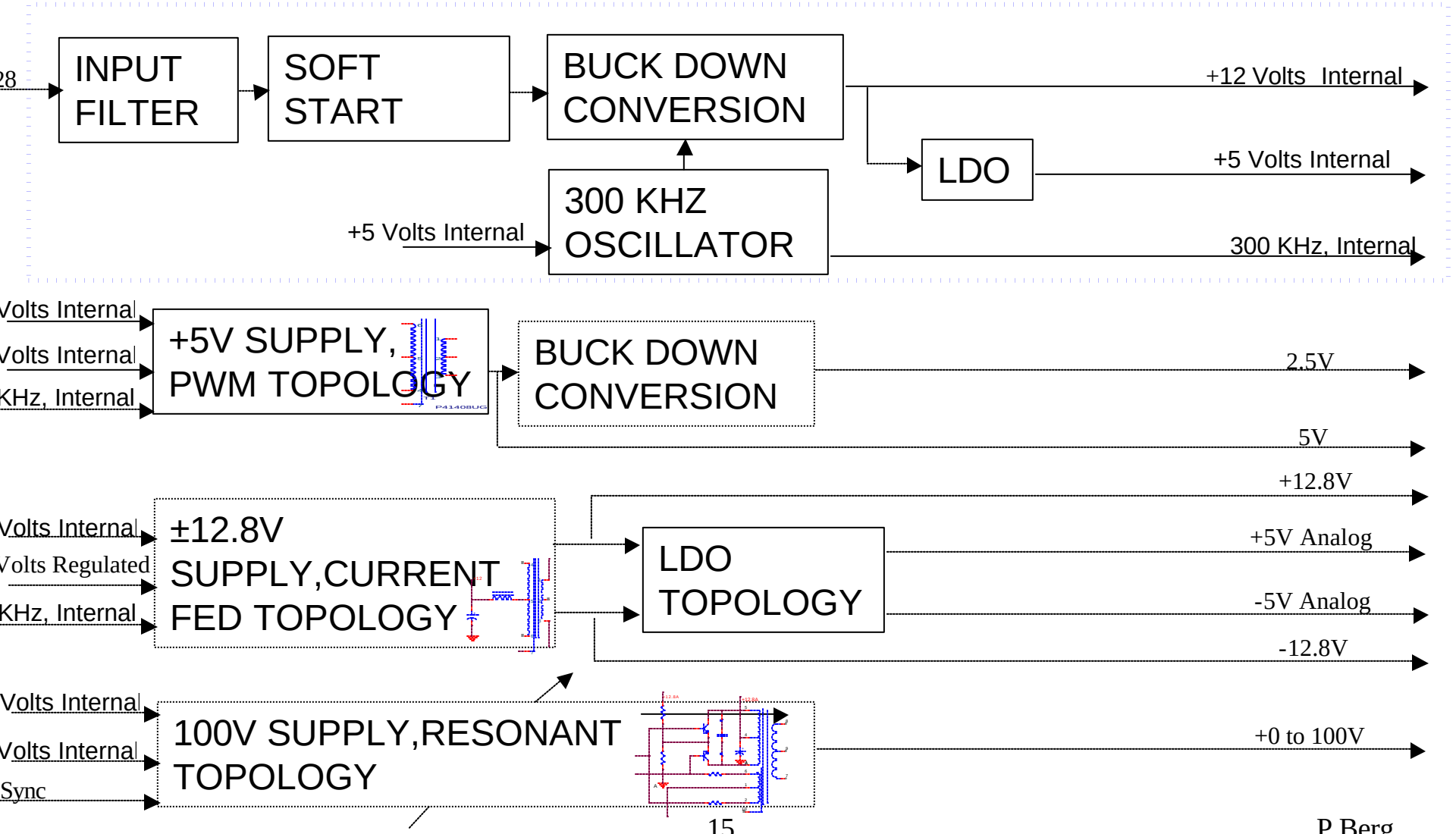


IDPU

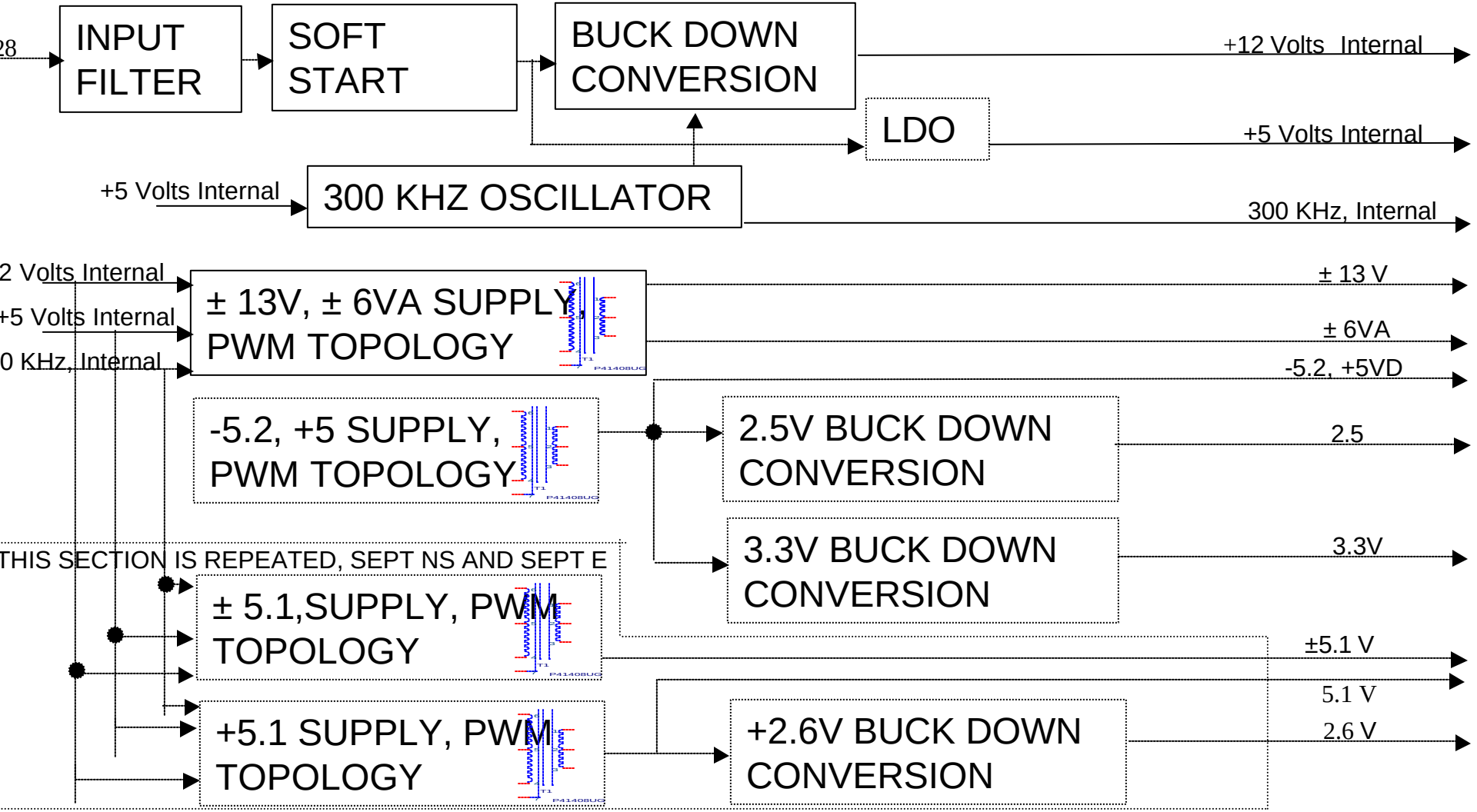
J12 A, LVPS OUTPUT	J1, SEP INPUT	J12 B, LVPS OUTPUT
PT-NS ANA RTN	1 Spare	1 LET PWR RTN
EPT-NS ANA RTN	2 +28V MAIN/OP HTR	26 LET PWR RTN
PT-NS +5.6A	3 +28V MAIN/OP HTR	2 LET +13A
EPT-NS +5.6A	4 Spare	27 LET +13A
re	5 +28V SURV HTR	3 LET +6A
are	6 +28V SURV HTR	28 LET +6A
PT-NS DIG RTN	7 Spare	4 LET -6A
EPT-NS DIG RTN	8 CHASSIS	29 LET -6A
PT-NS +2.6D	9 Spare	5 LET -13A
EPT-NS +2.6D	10 +28V MAIN/OP HTR RTN	30 LET -13A
PT-NS +5.3D	11 +28V MAIN/OP HTR RTN	6 LET +2.6D
EPT-NS +5.3D	12 Spare	31 LET +2.6D
PT-NS SEP STAR	13 +28V SURV HTR RTN	7 LET +3.4D
EPT-NS SEP STAR	14 +28V SURV HTR RTN	32 LET +3.4D
PT-E ANA RTN	15 PWR HRNS SHLD	8 LET +5.1D
EPT-E ANA RTN		33 LET +5.1D
PT-E +5.6A		9 CENTRAL ANA RTN
EPT-E +5.6A		34 CENTRAL ANA RTN
are		10 CENTRAL +13A
are		35 CENTRAL +13A
EPT-E DIG RTN		11 CENTRAL +6A
EPT-E DIG RTN		36 CENTRAL +6A
EPT-E +2.6D		12 CENTRAL -6A
EPT-E +2.6D		37 CENTRAL -6A
EPT-E +5.3D		13 CENTRAL -13A
EPT-E +5.3D		38 CENTRAL -13A
EPT-E SEP STAR		14 CENTRAL DIG RTN
EPT-E SEP STAR		39 CENTRAL DIG RTN
T PWR RTN		15 CENTRAL +2.6D
T PWR RTN		40 CENTRAL +2.6D
T +13A		16 CENTRAL +3.4D
T +13A		41 CENTRAL +3.4D
T +6A		17 CENTRAL +5.1D

49 SIT +6A		42 CENTRAL +5.1D
18 SIT +5A RTN		18 BIAS RTN
50 SIT +5A RTN		43 BIAS RTN
19 SIT -6A		19 LVPS TEMP SENSOR
51 SIT -6A		44 +28V OP HTR
20 SIT -13A		20 +28V OP HTR
52 SIT -13A		45 +28V OP HTR RTN
21 SIT -5.2D		21 +28V OP HTR RTN
53 SIT -5.2D		46 +28V SURV HTR
22 SIT +2.6D		22 +28V SURV HTR
54 SIT +2.6D		47 +28V SURV HTR RTN
23 SIT +3.4D		23 +28V SURV HTR RTN
55 SIT +3.4D		48 Spare
24 SIT +5.1D		24 Spare
56 SIT +5.1D		49 Spare
25 HET PWR RTN		25 Spare
57 HET PWR RTN		50 Spare
26 HET +13A		51 Spare
58 HET +13A		
27 HET +6A		
59 HET +6A		
28 HET -6A		
60 HET -6A		
29 HET -13A		
61 HET -13A		
30 HET +2.6D		
62 HET +2.6D		
31 HET +3.4D		
63 HET +3.4D		
32 HET +5.1D		
64 HET +5.1D		
65 Spare		

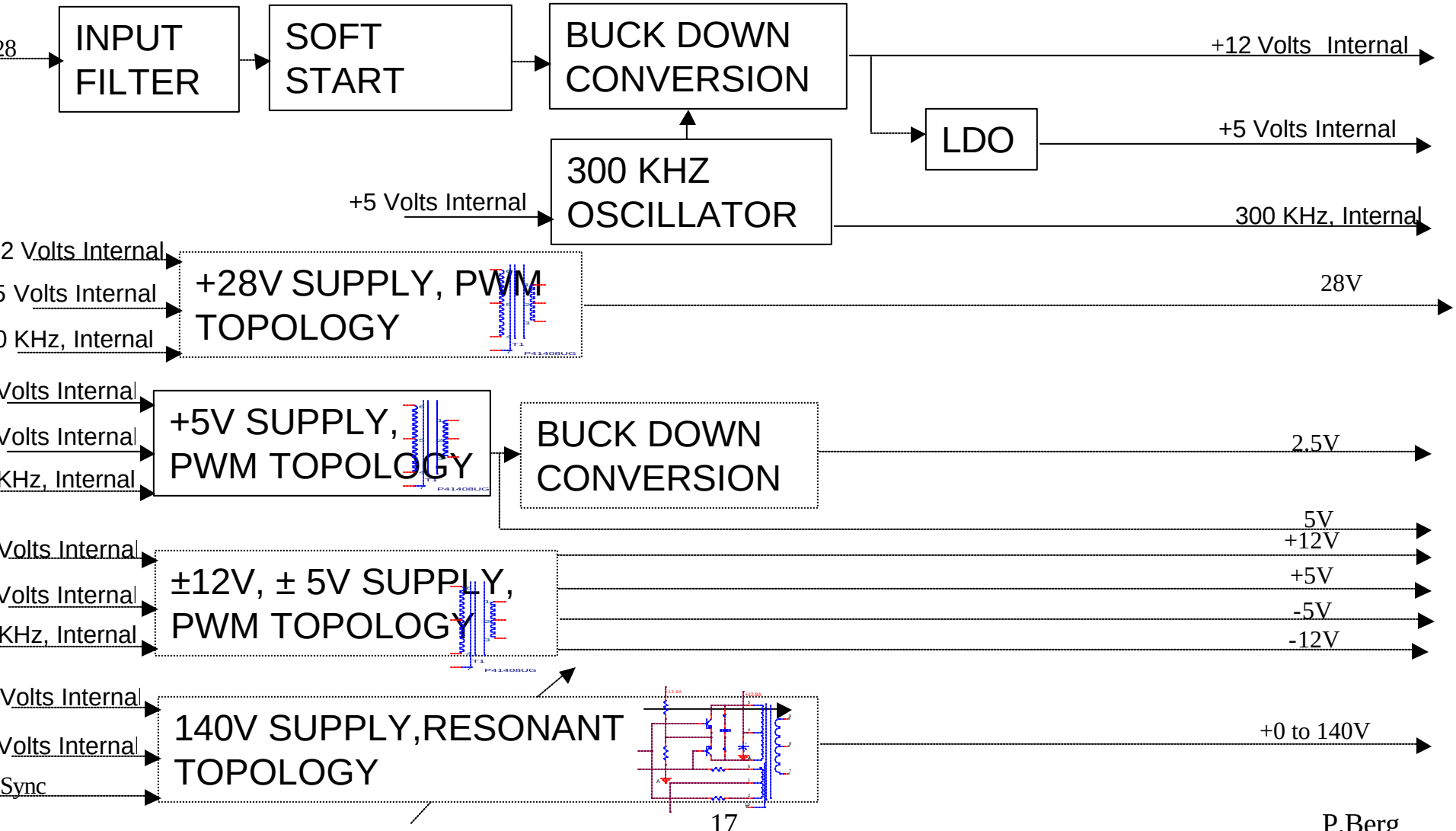
IDPU LVPS BLOCK DIAGRAM



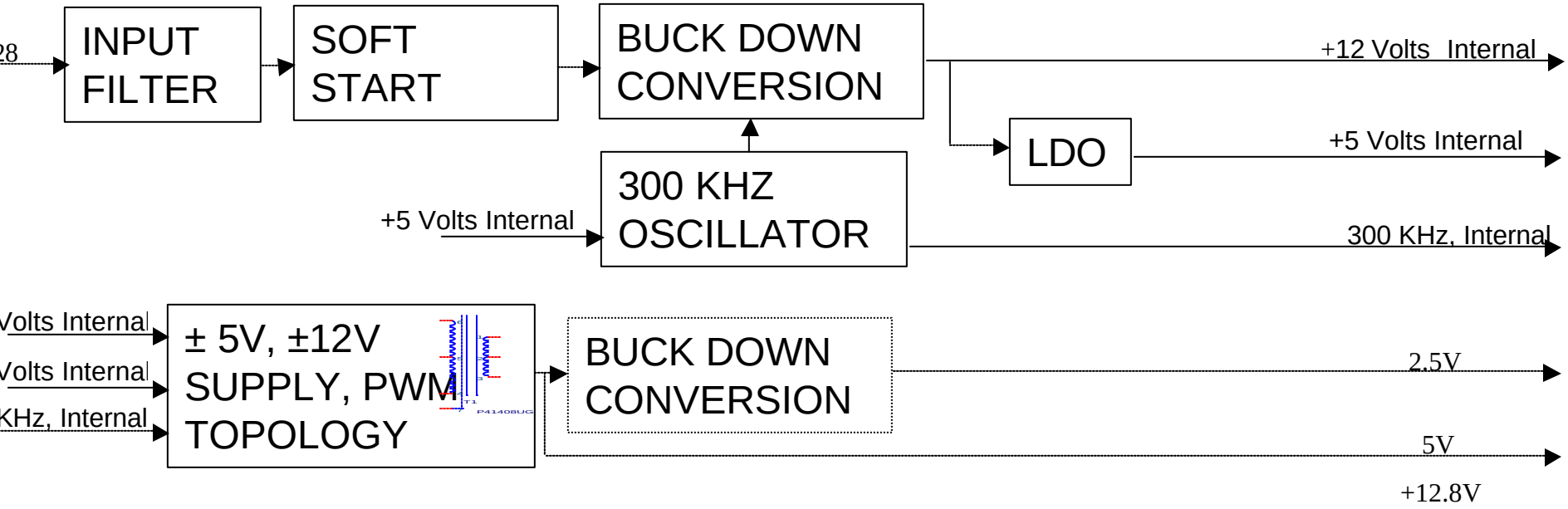
SEP LVPS BLOCK DIAGRAM



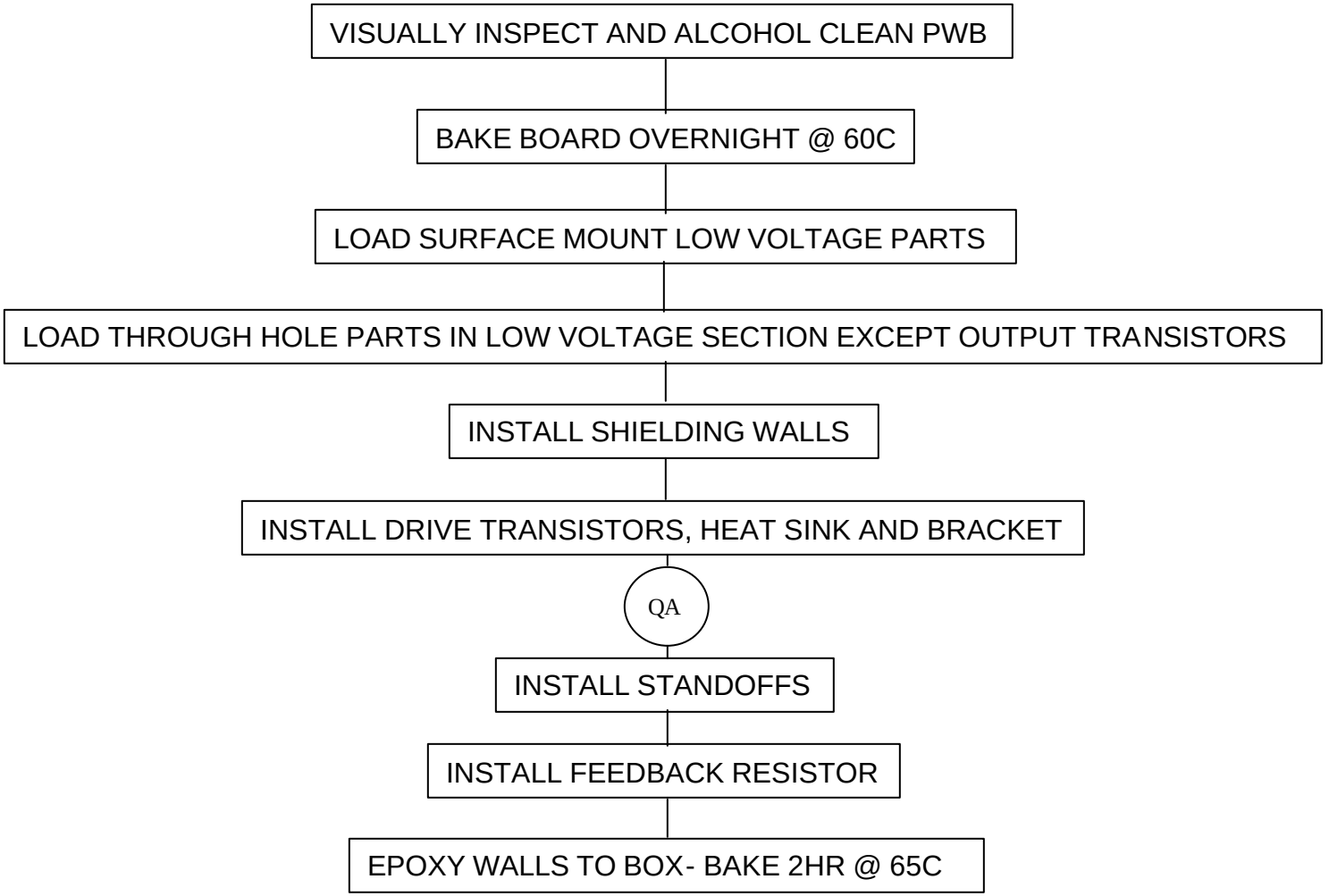
SWEA LVPS BLOCK DIAGRAM



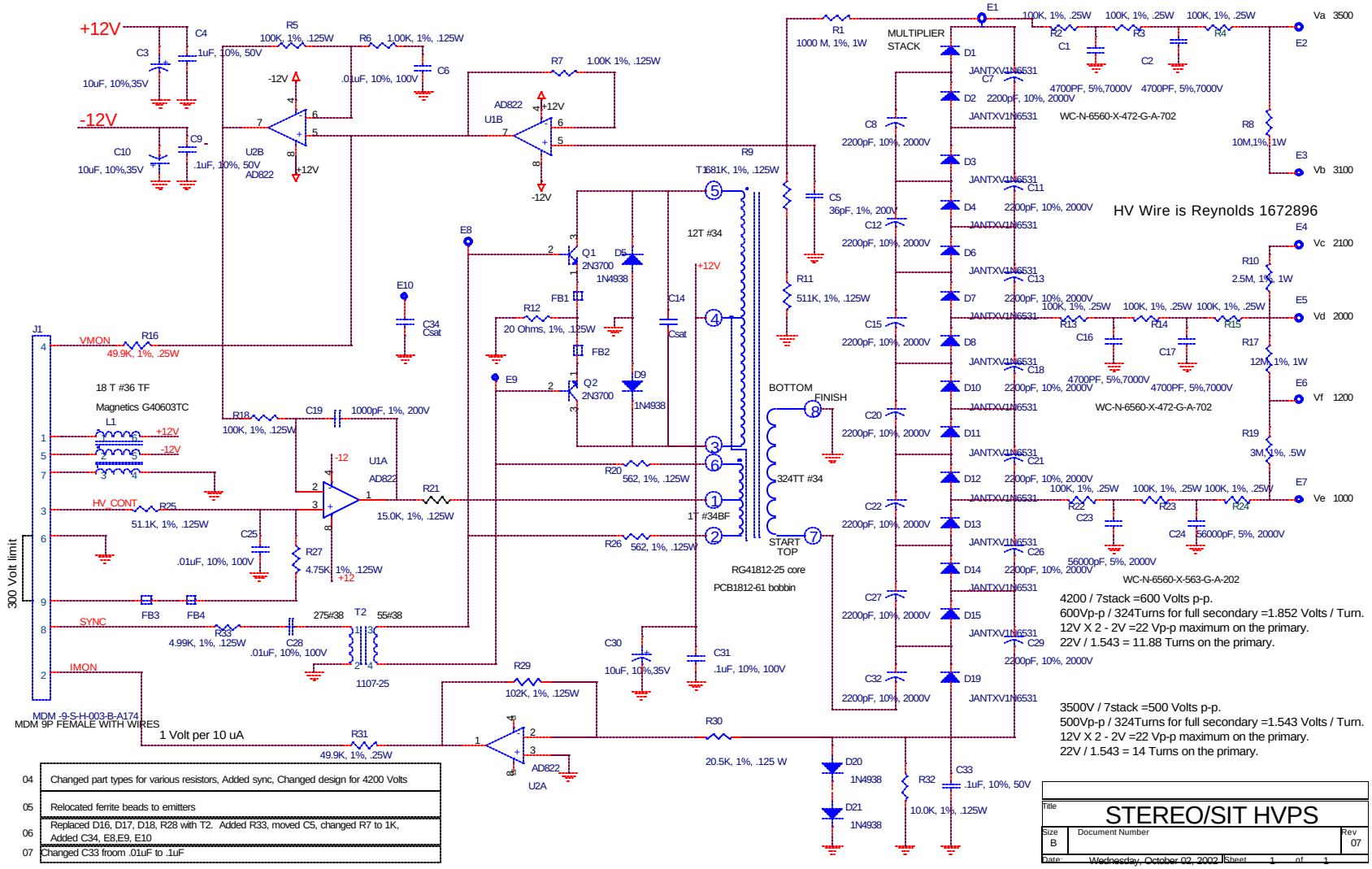
PLASTIC LVPS BLOCK DIAGRAM



HIGH VOLTAGE MANUFACTURING FLOW

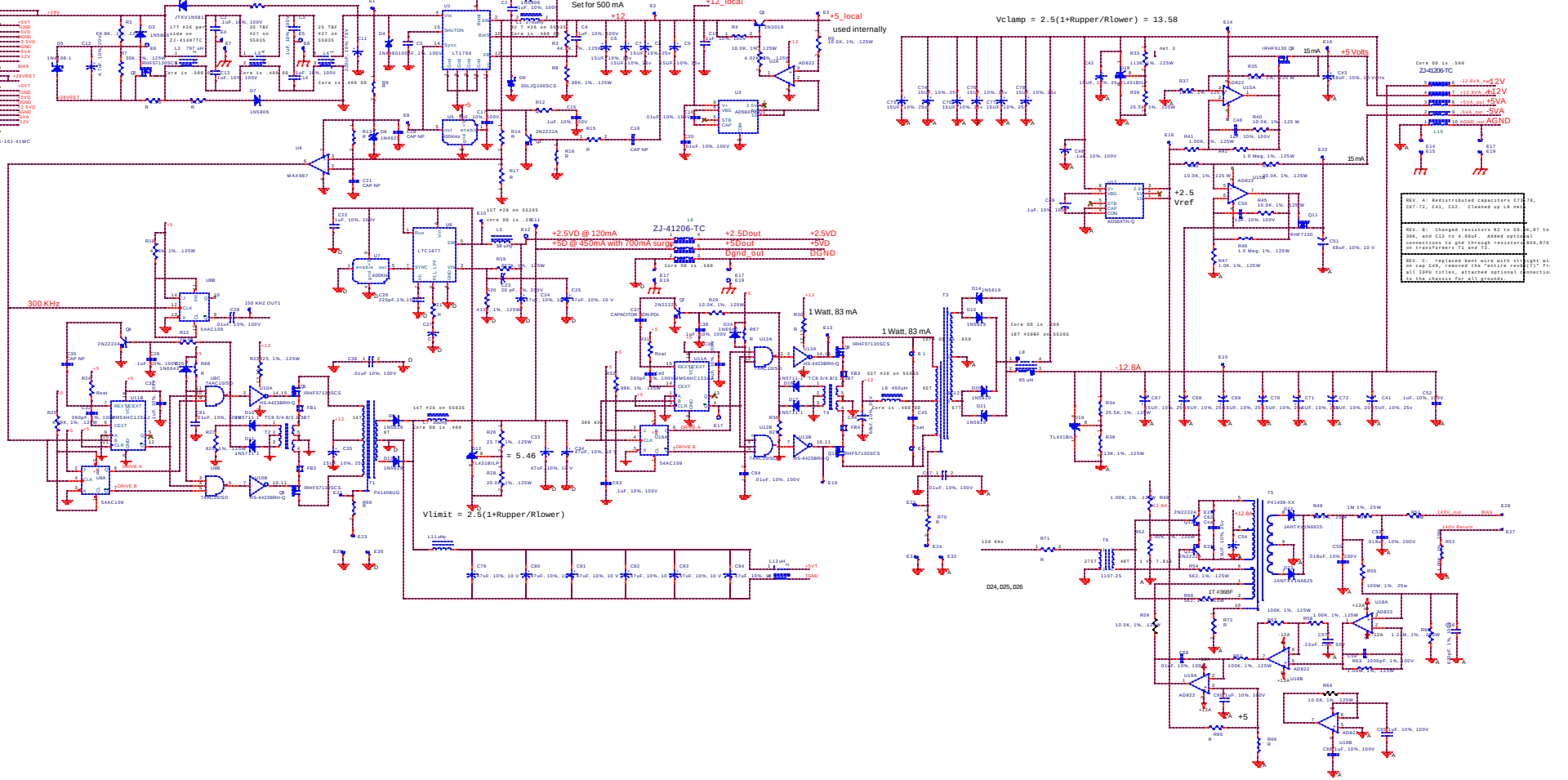


SCHEMATICS


+12V
-12V
C4
1uF, 10%, 50V
C3
10uF, 10%,35V
C10
10uF, 10%,35V
C9
.1uF, 10%, 50V
R5
100K, 1%, .125W
R6
1.00K, 1%, .125W
C6
.01uF, 10%, 100V
U2B
AD822
R7
1.00K 1%, .125W
U1B
AD822
R9
T1681K, 1%, .125W
R1
1000 M, 1%, 1W
MULTIPLIER STACK
E1
100K, 1%, .25W
100K, 1%, .25W
100K, 1%, .25W
R2
R3
R4
C1
C2
Va 3500
E2
JANTXV1N6531
2200pF, 10%, 2000V
4700PF, 5%,7000V
WC-N-6560-X-472-G-A-702
R8
10M,1%,1W
E3
Vb 3100
C5
36pF, 1%, 200V
R11
511K, 1%, .125W
HV Wire is Reynolds 1672896
E4
Vc 2100
R10
2.5M, 1%, 1W
E5
Vd 2000
R13
R14
R15
C16
C17
R17
12M, 1%, 1W
E6
Vf 1200
R19
3M, 1%, .5W
E7
Ve 1000
R22
R23
R24
C23
C24
56000pF, 5%, 2000V
WC-N-6560-X-563-G-A-202
E8
E9
E10
Q1
2N3700
D5
1N4938
Q2
2N3700
D9
1N4938
FB1
FB2
R12
20 Ohms, 1%, .125W
C14
Csat
C34
Csat
12T #34
+12V
BOTTOM FINISH
324TT #34
1T #34BF
START TOP
RG41812-25 core
PCB1812-61 bobbin
R20
562, 1%, .125W
R26
562, 1%, .125W
J1
VMON
R16
49.9K, 1%, .25W
18 T #36 TF
Magnetics G40603TC
L1
R18
100K, 1%, .125W
C19
1000pF, 1%, 200V
U1A
AD822
R21
15.0K, 1%, .125W
HV_CONT
R25
51.1K, 1%, .125W
C25
.01uF, 10%, 100V
R27
4.75K, 1%, .125W
+12
300 Volt limit
FB3
FB4
SYNC
R33
4.99K, 1%, .125W
C28
.01uF, 10%, 100V
T2
275#38
55#38
1107-25
IMON
MDM -9-S-H-003-B-A174
MDM 9P FEMALE WITH WIRES
1 Volt per 10 uA
R31
49.9K, 1%, .25W
U2A
AD822
R29
102K, 1%, .125W
C30
10uF, 10%,35V
C31
.1uF, 10%, 100V
R30
20.5K, 1%, .125 W
D20
1N4938
D21
1N4938
R32
10.0K, 1%, .125W
C33
.1uF, 10%, 50V
C1
C2
C7
C8
C11
C12
C13
C15
C18
C20
C21
C22
C26
C27
C29
C32
D1
D2
D3
D4
D6
D7
D8
D10
D11
D12
D13
D14
D15
D19
4200 / 7stack =600 Volts p-p.
600Vp-p / 324Turns for full secondary =1.852 Volts / Turn.
12V X 2 - 2V =22 Vp-p maximum on the primary.
22V / 1.543 = 11.88 Turns on the primary.
3500V / 7stack =500 Volts p-p.
500Vp-p / 324Turns for full secondary =1.543 Volts / Turn.
12V X 2 - 2V =22 Vp-p maximum on the primary.
22V / 1.543 = 14 Turns on the primary.
04 Changed part types for various resistors, Added sync, Changed design for 4200 Volts
05 Relocated ferrite beads to emitters
06 Replaced D16, D17, D18, R28 with T2. Added R33, moved C5, changed R7 to 1K, Added C34, E8,E9, E10
07 Changed C33 from .01uF to .1uF
Title
STEREO/SIT HVPS
Size B
Document Number
Rev 07
Date: Wednesday, October 02, 2002
Sheet 1 of 1

STEREO IMPACT

Critical Design Review
2002 November 20,21,22

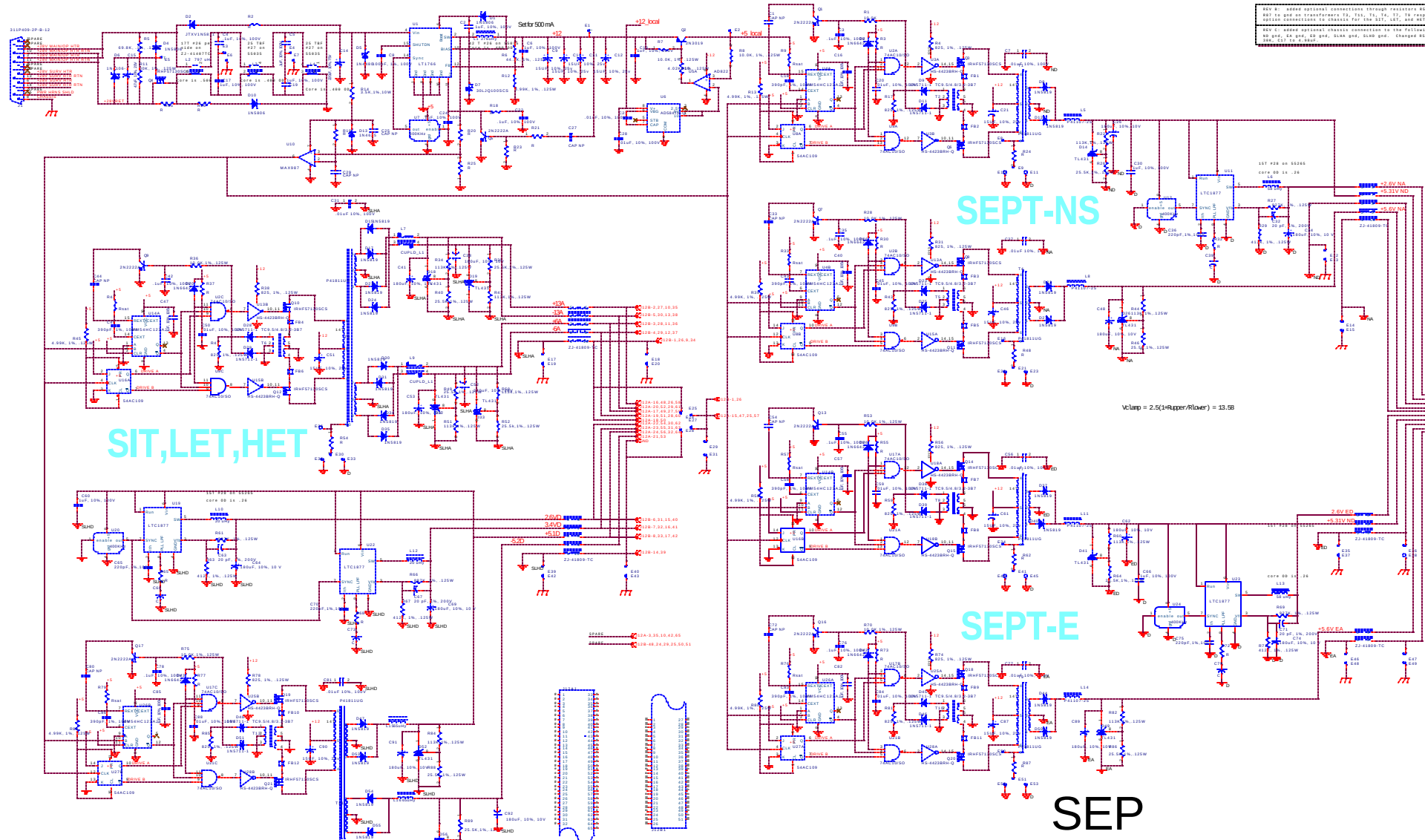


IDPU

P.Berg

STEREO IMPACT

Critical Design Review
2002 November 20,21,22



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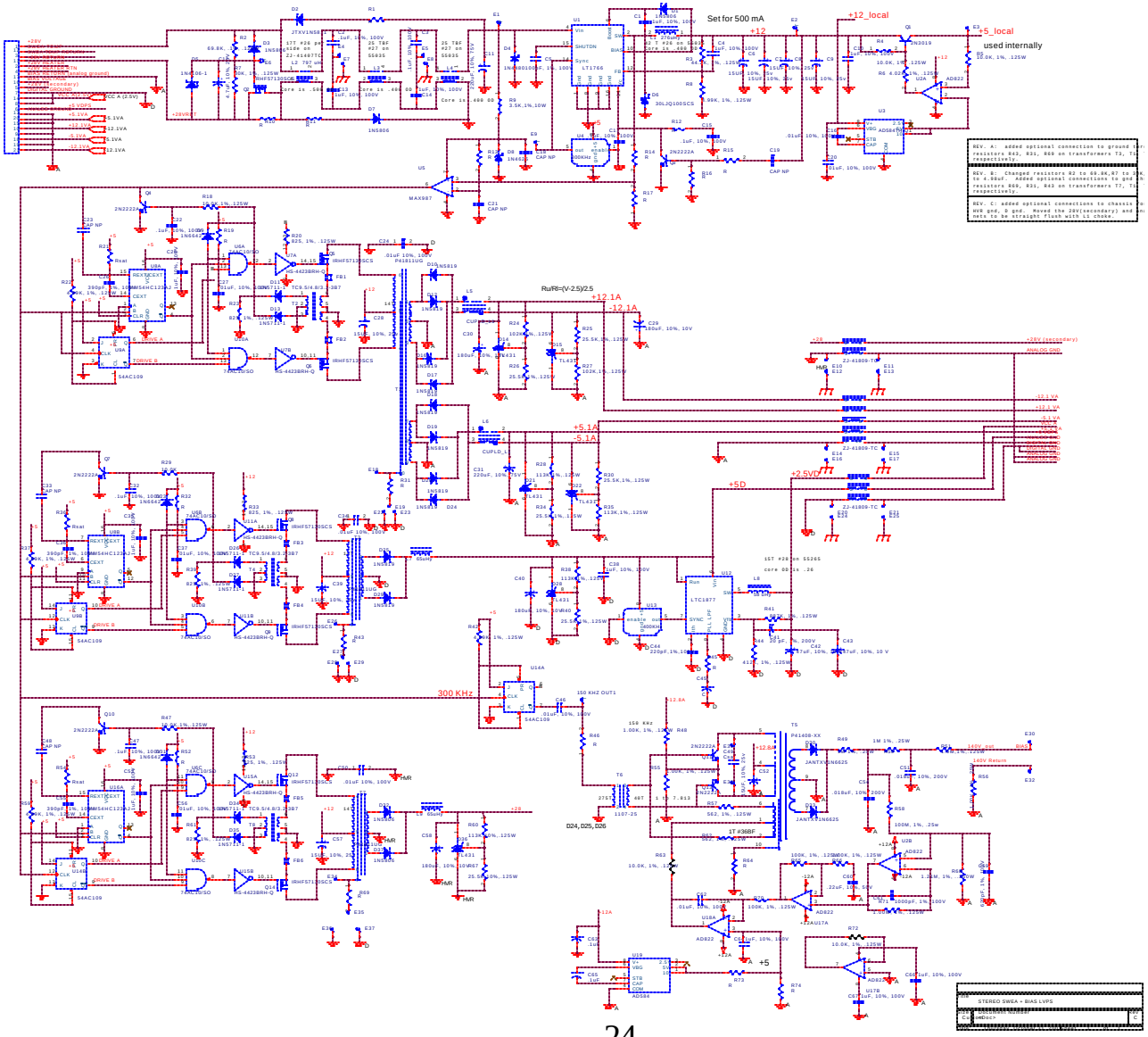
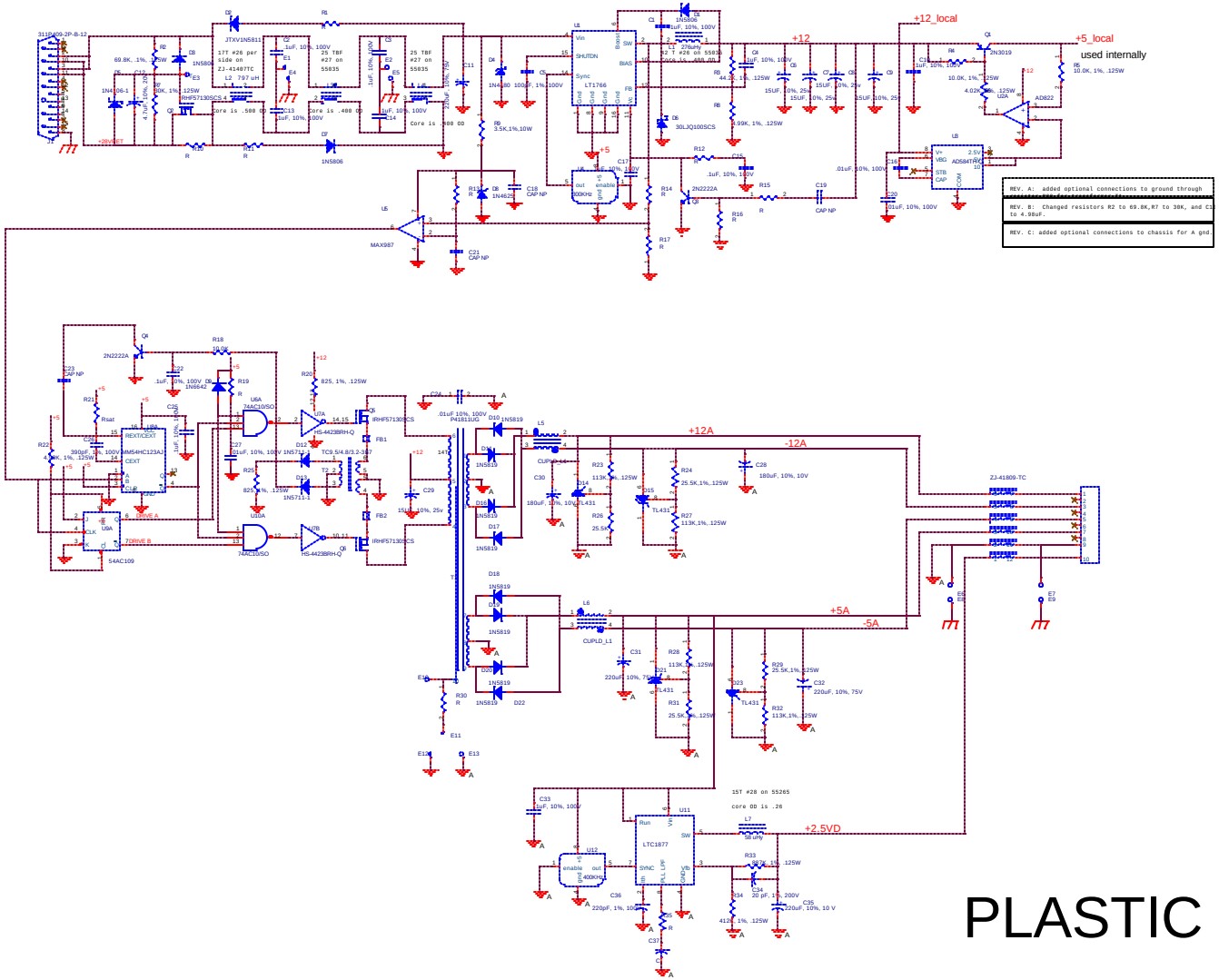
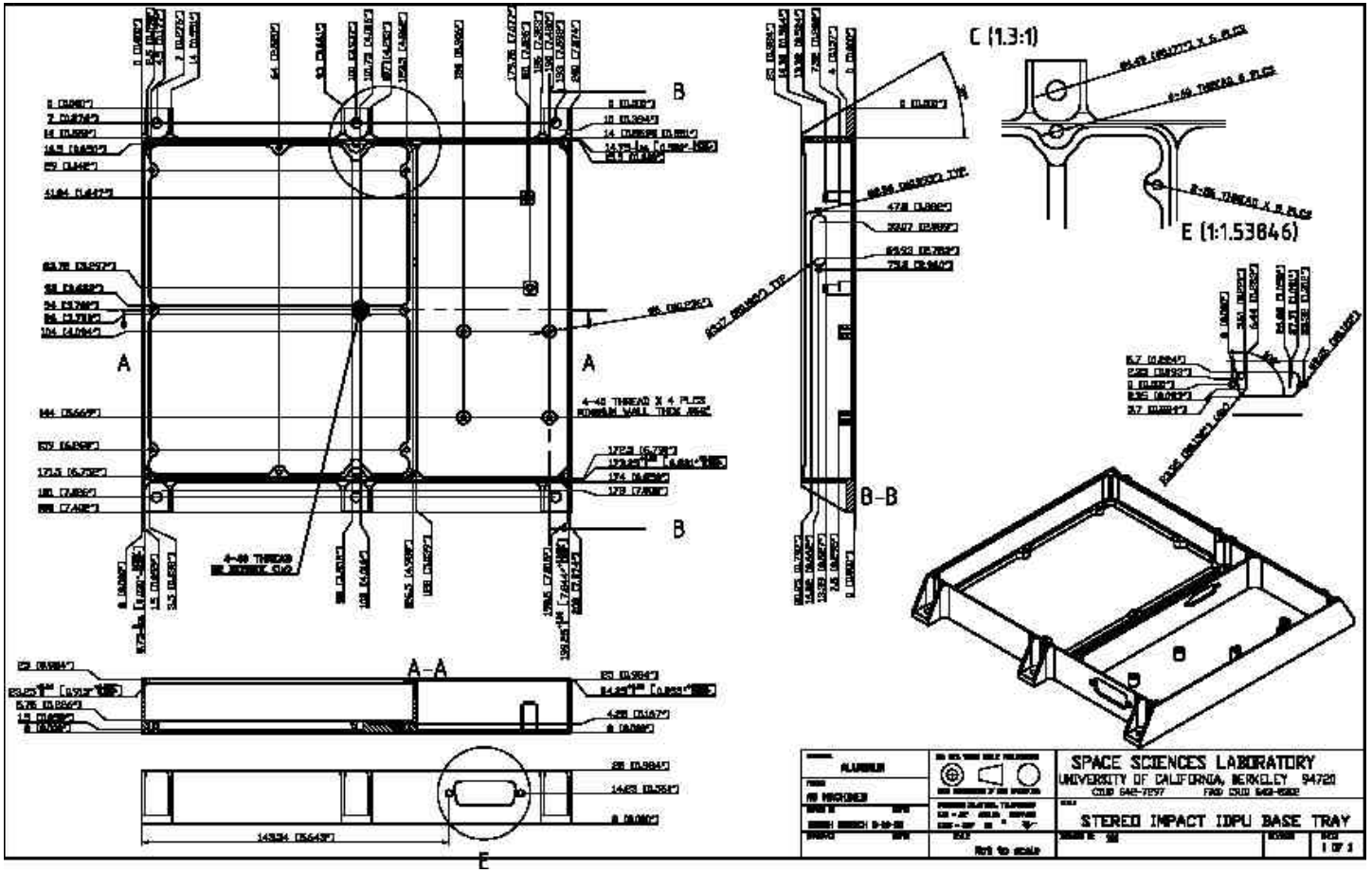

Set for 500 mA
+12_local
+5_local
used internally
+12
+5
+12.1A
-12.1A
+5.1A
-5.1A
+2.5VD
+5D
300 KHz
150 KHZ OUT1
D24, D25, D26
STEREO SWEA + BIAS LVPS



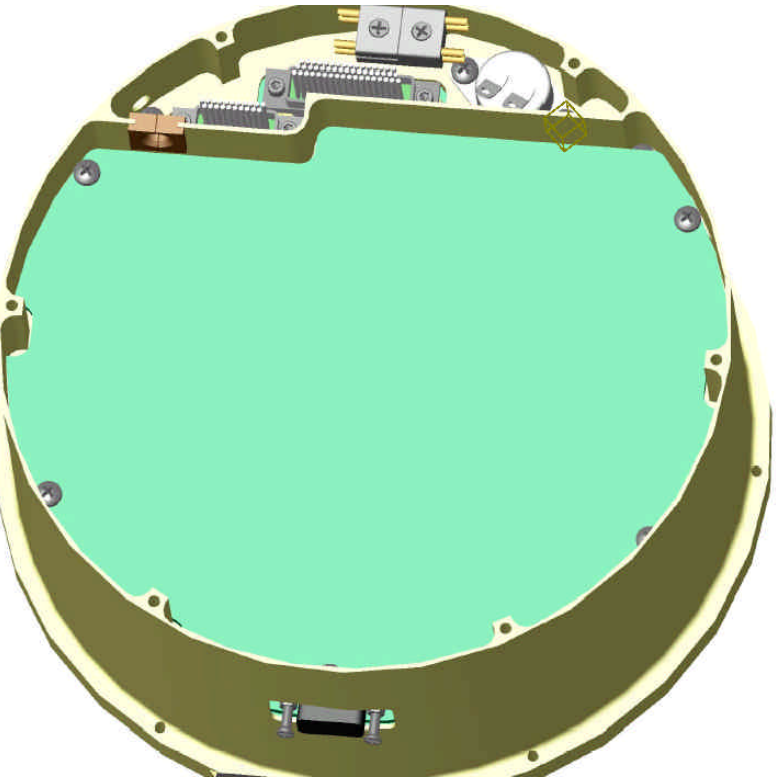
STEREO PLASTIC LVPS NEW VER.

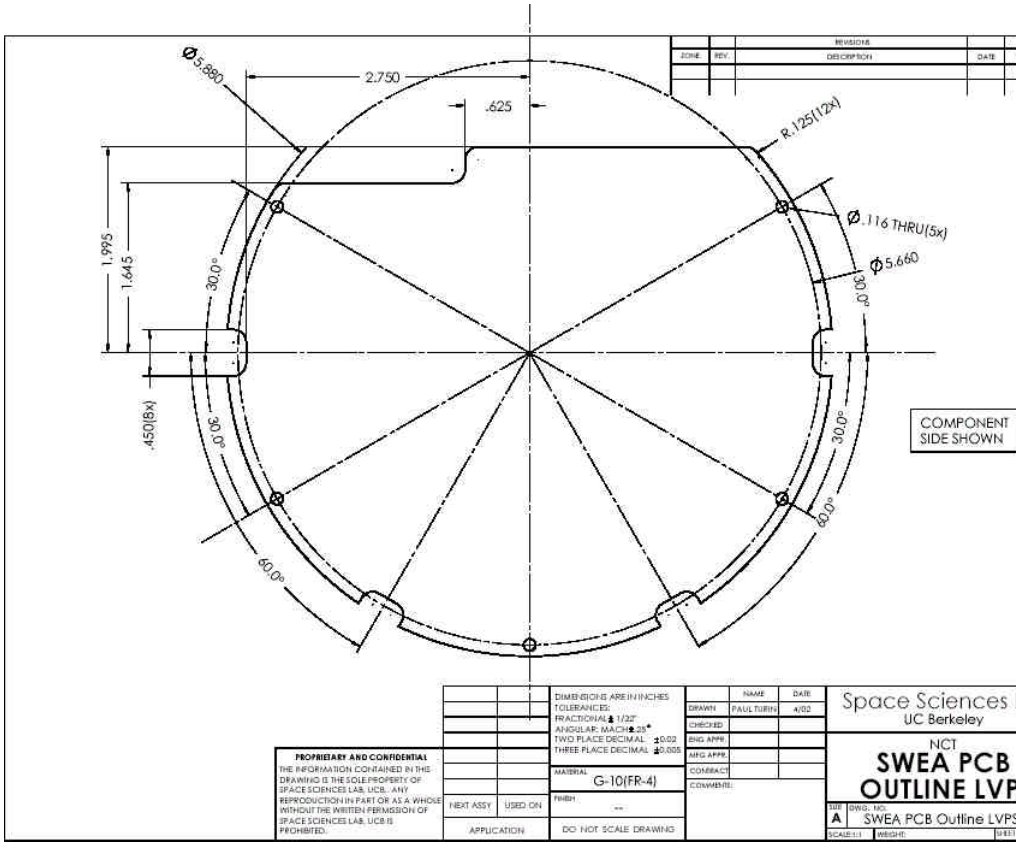
P.Berg

IDPU LVPS


C (1.3:1)
E (1:1.53846)
B-B
A-A
SPACE SCIENCES LABORATORY
UNIVERSITY OF CALIFORNIA, BERKELEY 94720
STEREO IMPACT IDPU BASE TRAY

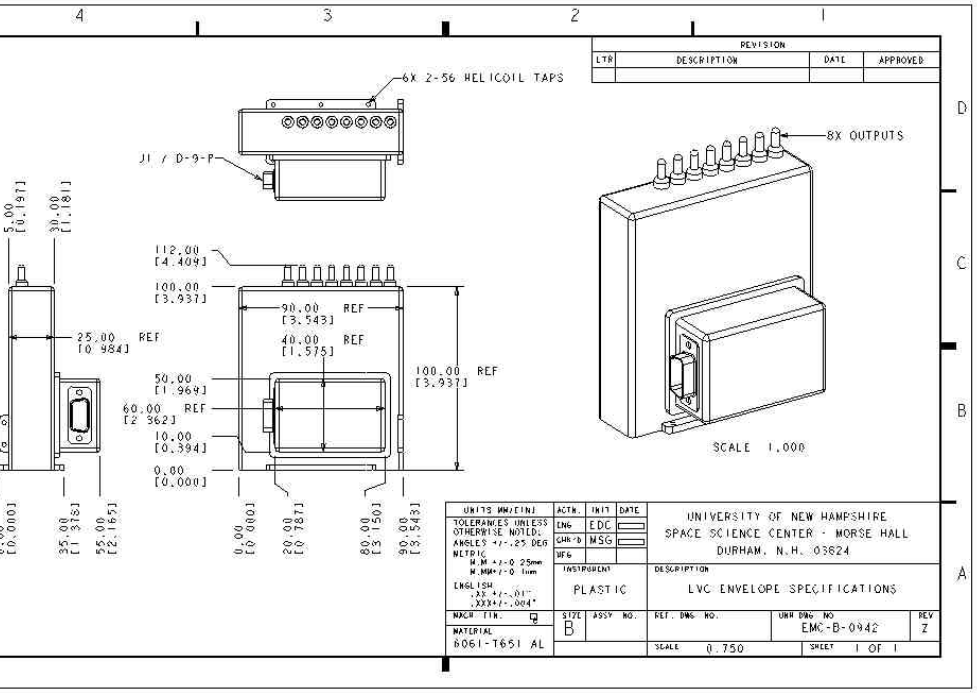
SWEA

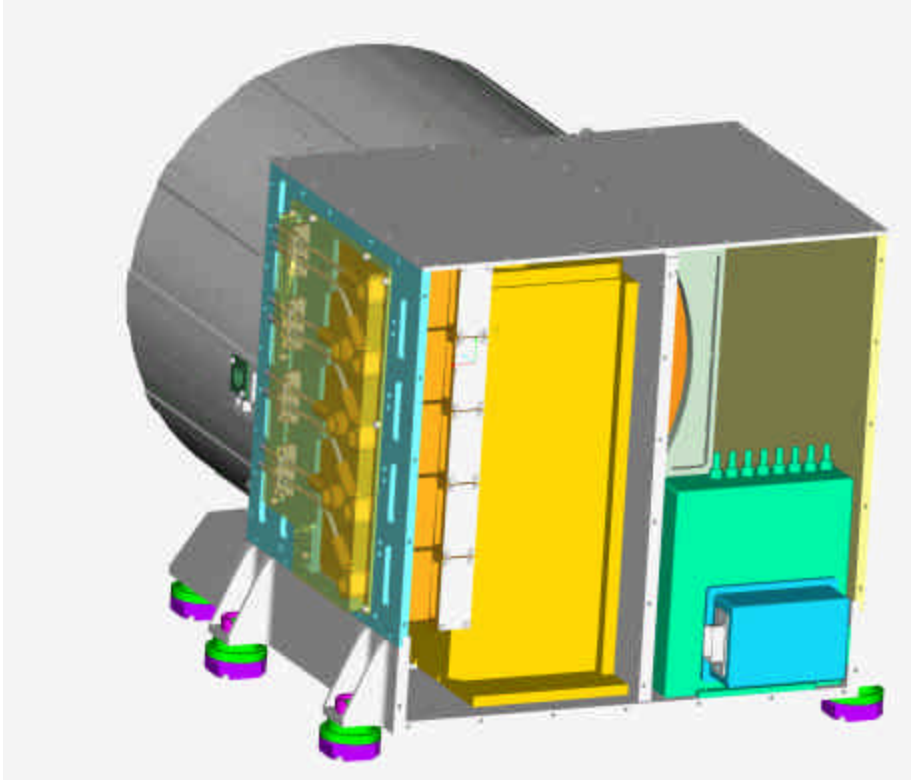



Ø5.890
2.750
.625
R.125(12x)
Ø.116 THRU(5x)
Ø5.660
1.995
1.645
30.0°
.450(8x)
60.0°
COMPONENT SIDE SHOWN
PROPRIETARY AND CONFIDENTIAL
THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF SPACE SCIENCES LAB, UCB. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF SPACE SCIENCES LAB, UCB IS PROHIBITED.
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ± 1/32"
ANGULAR: MACH ± .25°
TWO PLACE DECIMAL ±0.02
THREE PLACE DECIMAL ±0.005
MATERIAL
G-10(FR-4)
FINISH

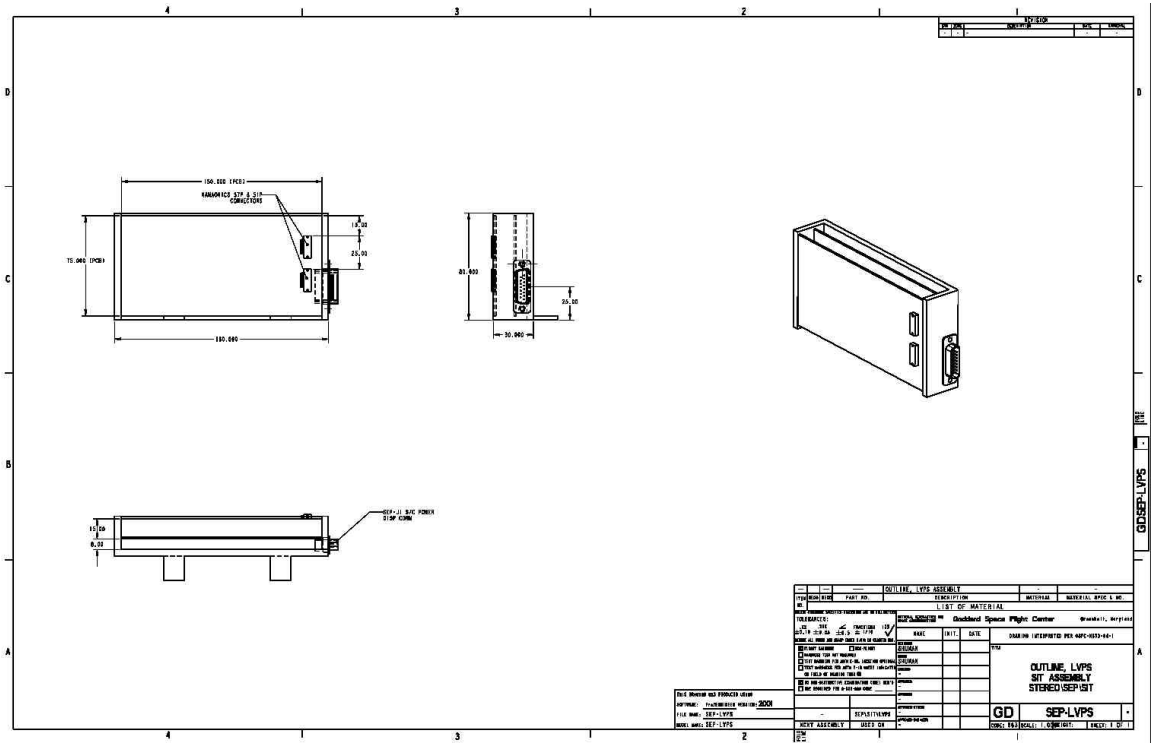
DO NOT SCALE DRAWING
NEXT ASSY
USED ON
APPLICATION
DRAWN
PAUL TURPIN
4/02
CHECKED
ENG APPR.
MFG APPR.
COMMENTS:
Space Sciences
UC Berkeley
NCT
SWEA PCB
OUTLINE LVP
SIZE
A
SWEA PCB Outline LVPS

PLASTIC


6X 2-56 HELICOIL TAPS
J1 / D-9-P
8X OUTPUTS
SCALE 1.000
REVISION
LTR
DESCRIPTION
DATE
APPROVED
UNIVERSITY OF NEW HAMPSHIRE
SPACE SCIENCE CENTER - MORSE HALL
DURHAM, N.H. 03824
PLASTIC
LVC ENVELOPE SPECIFICATIONS
EMC-B-0942
6061-T651 AL



SEP LVPS


OUTLINE, LVPS ASSEMBLY
LIST OF MATERIAL
Goddard Space Flight Center
OUTLINE, LVPS
S/T ASSEMBLY
STEREO\SEP\ST
GD
SEP-LVPS
GDSEP-LVPS

STATUS

SIT HV ETU BUILT AND DELIVERED

IDPU LVPS BOX FABRICATED, ETU IN TEST

SCHEMATICS MOSTLY COMPLETE

PEER REVIEW RFAs

IMPACT UCB LVPS/HVPS Review CLOSURE STATUS (8/9/02)

Action No.	Action Item TITLE	ORIGINATOR	RESPONSE STATUS	DATE CLOSED
1	HVPS Temperature test	Brian King	TBDone	
2	SIT HVPS Grounding	Shane Hynes	TBDone	
3	Potting material	Harry Culver	Submitted	
4	Capacitive load testing	Harry Culver	Submitted	
5	LVPS Soft Start	Shane Hynes	Submitted	
6	LVPS Input Voltage Testing	Harry Culver	Submitted	
7	Oscillation Protection	Harry Culver	Done	
8	Loss of synchronization circuitry	Harry Culver	Designed	
9	Survival of 40V	Harry Culver	Designed	
10	IDPU LVPS Clarity	Harry Culver	Done	
11	Add grounding jumpers	Harry Culver	Designed	
12	Terminate shields	Harry Culver	Designed	
13	Add capacitor	Harry Culver	Done	
14	PLASTIC ripple requirements	Shane Hynes	Received	
15	Grounding requirement for PLASTIC LVPS	Ken Crocker	Submitted	

WHATS LEFT

SIT HV ETU – RESOLVE ETU TEST ISSUES

IDPU FINISH ETU TEST

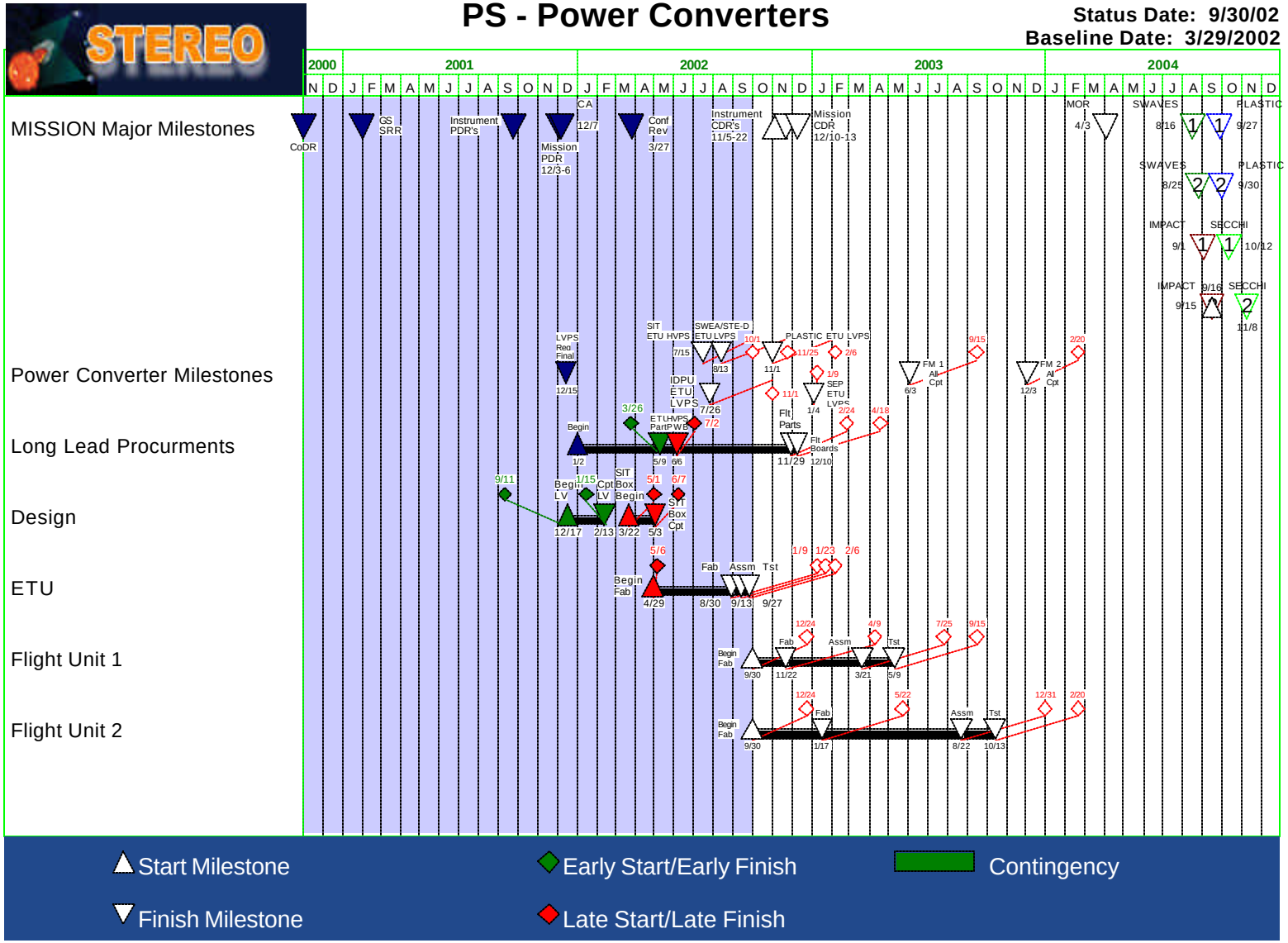
SIT, SEPT, PLASTIC –> LAYOUT, BUILD AND TEST ETUS

VERIFICATION

PERFORM CE TESTS ON FINISHED ETUS

ETU DELIVERY SCHEDULE

- IDPU DEC 30, 2002
- SEP JAN 30, 2003
- SWEA, FEB 28, 2003
- PLASTIC MAR 15, 2003


PS - Power Converters
Status Date: 9/30/02
Baseline Date: 3/29/2002
2000
2001
2002
2003
2004
N D J F M A M J J A S O N D J F M A M J J A S O N D J F M A M J J A S O N D J F M A M J J A S O N D
MISSION Major Milestones
Power Converter Milestones
Long Lead Procurments
Design
ETU
Flight Unit 1
Flight Unit 2
CoDR
GS SRR
Instrument PDR's
Mission PDR 12/3-6
CA 12/7
Conf Rev 3/27
Instrument CDR's 11/5-22
Mission CDR 12/10-13
MOR 4/3
SWAVES 8/16
PLASTIC 9/27
SWAVES 8/25
PLASTIC 9/30
IMPACT 9/1
SECCHI 10/12
IMPACT 9/15
SECCHI 11/8
LVPS Req Final 12/15
SIT ETU HVPS 7/15
SWEA/STE-D ETU LVPS 8/13
10/1
PLASTIC ETU LVPS 11/1
11/25
2/6
IDPU ETU LVPS 7/26
11/1
1/9
SEP ETU LVPS 1/4
FM 1 All Cpt 6/3
9/15
FM 2 All Cpt 12/3
2/20
3/26
ETU HVPS PartP WB 7/2
Flt Parts 11/29
2/24
4/18
Flt Boards 12/10
Begin 1/2
9/11
Begin LV 12/17
1/15
Cpt LV 2/13
SIT Box Begin 3/22
5/1
6/7
SIT Box Cpt 5/3
5/9
6/6
5/6
Begin Fab 4/29
Fab
Assm
Tst
8/30
9/13
9/27
1/9
1/23
2/6
12/24
9/30
11/22
4/9
3/21
7/25
5/9
9/15
5/22
1/17
8/22
12/31
10/13
Start Milestone
Finish Milestone
Early Start/Early Finish
Late Start/Late Finish
Contingency

KNOWN ISSUES

•SCHEDULE

REVISE PRIORITIES, ADD MANPOWER

•SIT HVPS

RESOLVE SPECIFICATIONS

RESOLVE CONSUMPTION VS SYNC

•PARTS ISSUES

LONG LEAD TIMES ON HV MOX RESISTORS

LTC1877 PWM METALIZATION