SupraThermal Electron Detector (STE)

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STE Overview

- STE is an instrument to cover the electron energy range 2-20keV (between SWEA and SEPT) with enhanced sensitivity
  - Reasonably sized electrostatic analyzers have insufficient sensitivity
  - Standard silicon detector telescopes cannot reach this low an energy
- STE uses small, low capacitance, passively cooled silicon detectors with ultra low noise electronics
  - Similar detectors have been successfully used for X-rays down to 1keV
  - Measurements of prototype detectors indicates electrons down to 3.5keV can be measured
- A large FOV is required to cover the solar wind electrons and back-streaming electrons
  - Two oppositely directed 80 degree by 80 degree FOV oriented along the Parker Spiral covers the halo electron distribution the majority of the time.
  - Detector sensitivity to visible light requires the FOV to be clear of any object that can scatter sunlight

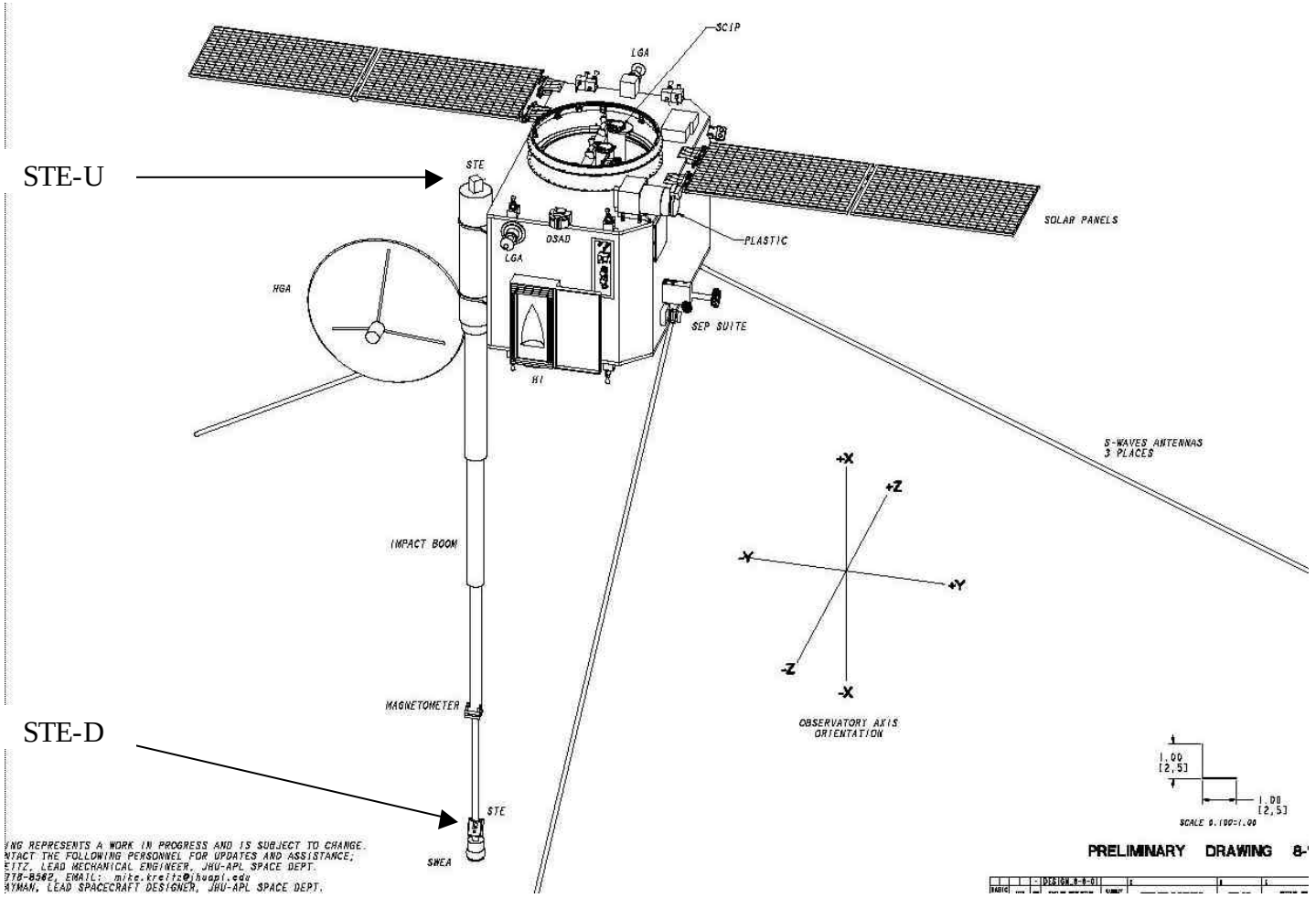
STE Performance Requirements

Description	Requirement	Goal	Source
FOV	60 x 60 degree	Two opposite 80 x 80 degree	Derived from MRD 4.7(F,G) & solar wind characteristics
Resolution	60 x 20 degrees	80 x 20 degrees	Derived from MRD 4.7(F,G) & solar wind characteristics
Energy	5 – 100 keV	2 - 100 keV	MRD 4.7 (F,G)
Energy Resolution (Telemetry)	100%	35%	Derived from MRD 4.7(F,G) & solar wind characteristics
Energy Resolution (Electronic)	2keV	300eV FWHM	Derived from lower energy and resolution requirements above.
Geometric Factor	0.1 cm^2 ster	0.4 cm^2 ster	Derived from MRD 4.7(F,G) & solar wind characteristics
Background	<30c/s /detector	<1c/s/detector	Derived from MRD 4.7(F,G) & solar wind characteristics
Max Count Rate (per detector)	10,000 counts/sec	100,000 counts/sec	Derived from MRD 4.7(F,G) & solar wind characteristics
Time Resolution	1 minute	16 seconds 2 seconds (burst)	MRD 4.7 (F,G)

STE Design

- There are 2 STE Units per spacecraft
  - STE-U (Upstream), mounted on the sunward (fixed) end of the boom
  - STE-D (Downstream), mounted near SWEA at the end of the boom
  - Divided to provide clear fields of view
- The STE Detector Units contain only the detectors, input devices and passive components
  - Minimizes thermal dissipation to simplify passive cooling
  - Cooling the detectors lowers noise and enhances performance
- The rest of the preamp is in the SWEA/STE housing (STE-D) or a separate housing supporting the detector unit (STE-U)
- The shaper electronics is located in SWEA or the IDPU enclosure
- STE must have reclosable doors
  - Contamination on the ground, during launch, and during thruster firings
  - Damage due to overheating if detector is exposed to sunlight
  - Simple TiNi actuators , one to open and one to close door

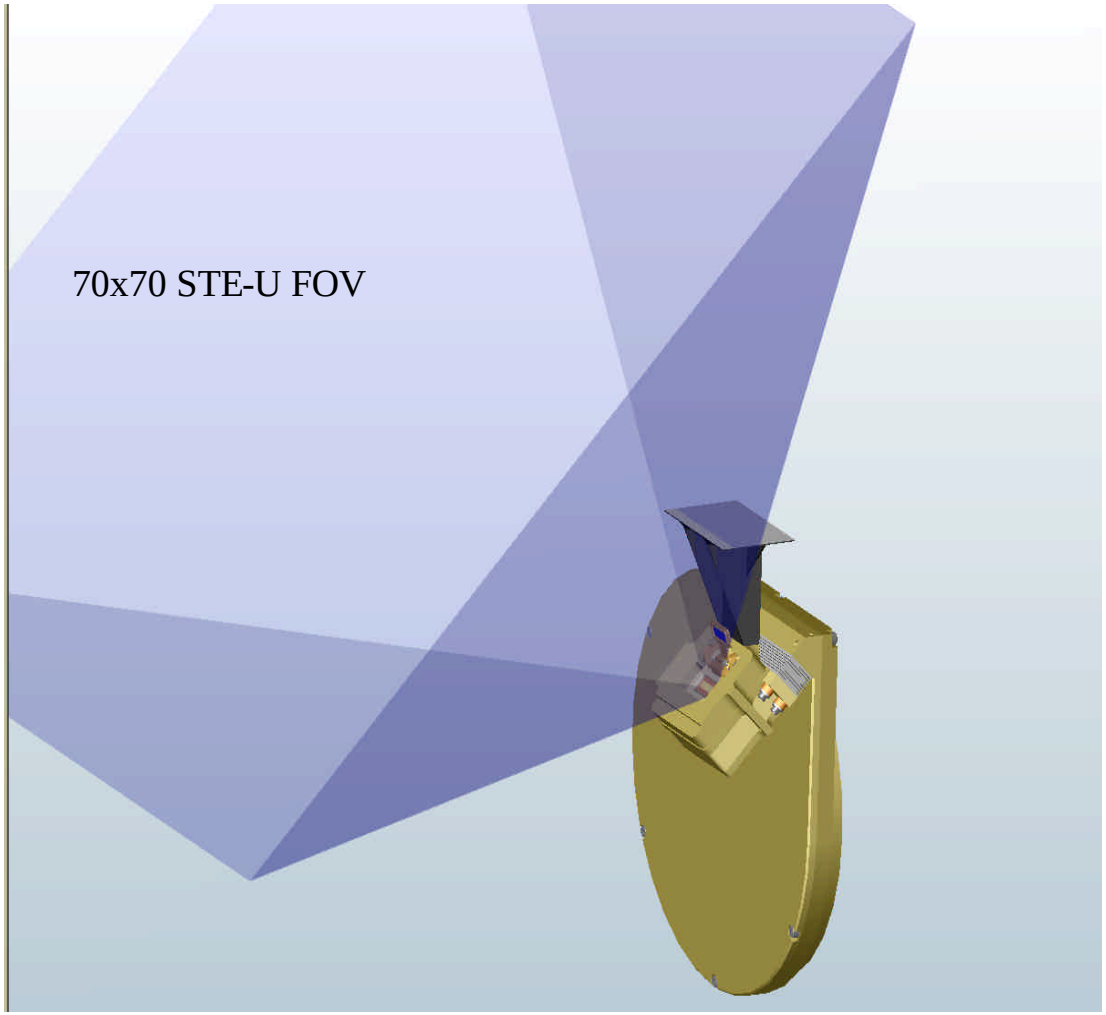
STE on SPACECRAFT



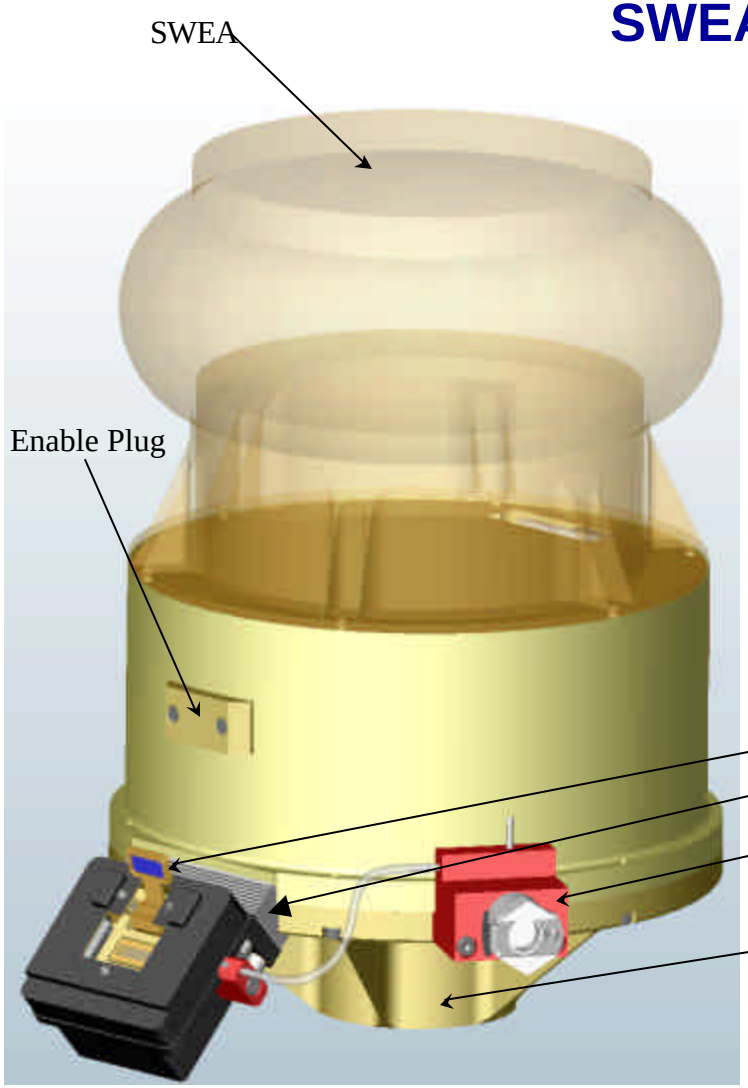
STE-U

STE-U w/FOV and Preamp

Mounts to side of IMPACT Boom



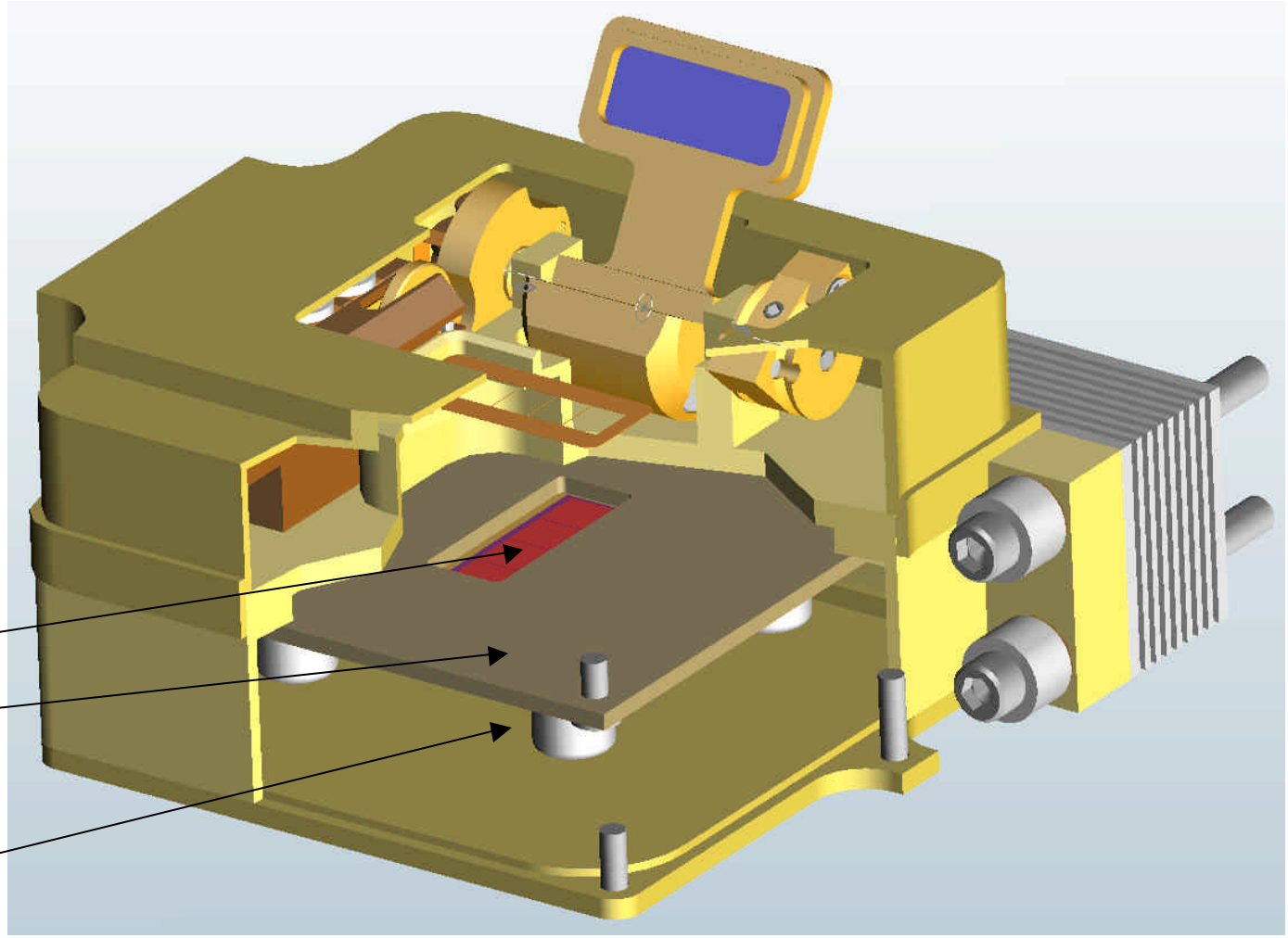
SWEA/STE-D Pedestal



- **Fabricated from 6061-T6xx Aluminum, incorporates both instruments and their electronics in a compact package and mounts them on the IMPACT boom.**
- **STE-D is thermally isolated from pedestal to allow it to cool to 187K.**
- **The SWEA is mounted to the extreme end, where its 4p Steradian FOV is unobstructed, and the STE-D is mounted to the side, under the SWEA FOV.**

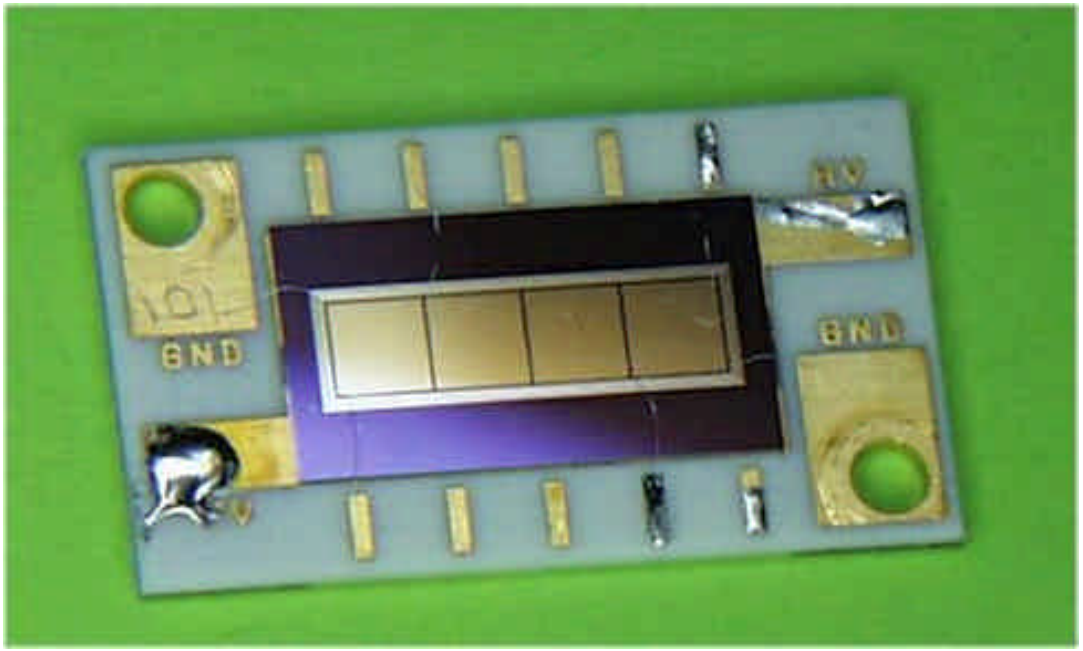
STE Detector and Housing

Cutaway showing Detector and PCB

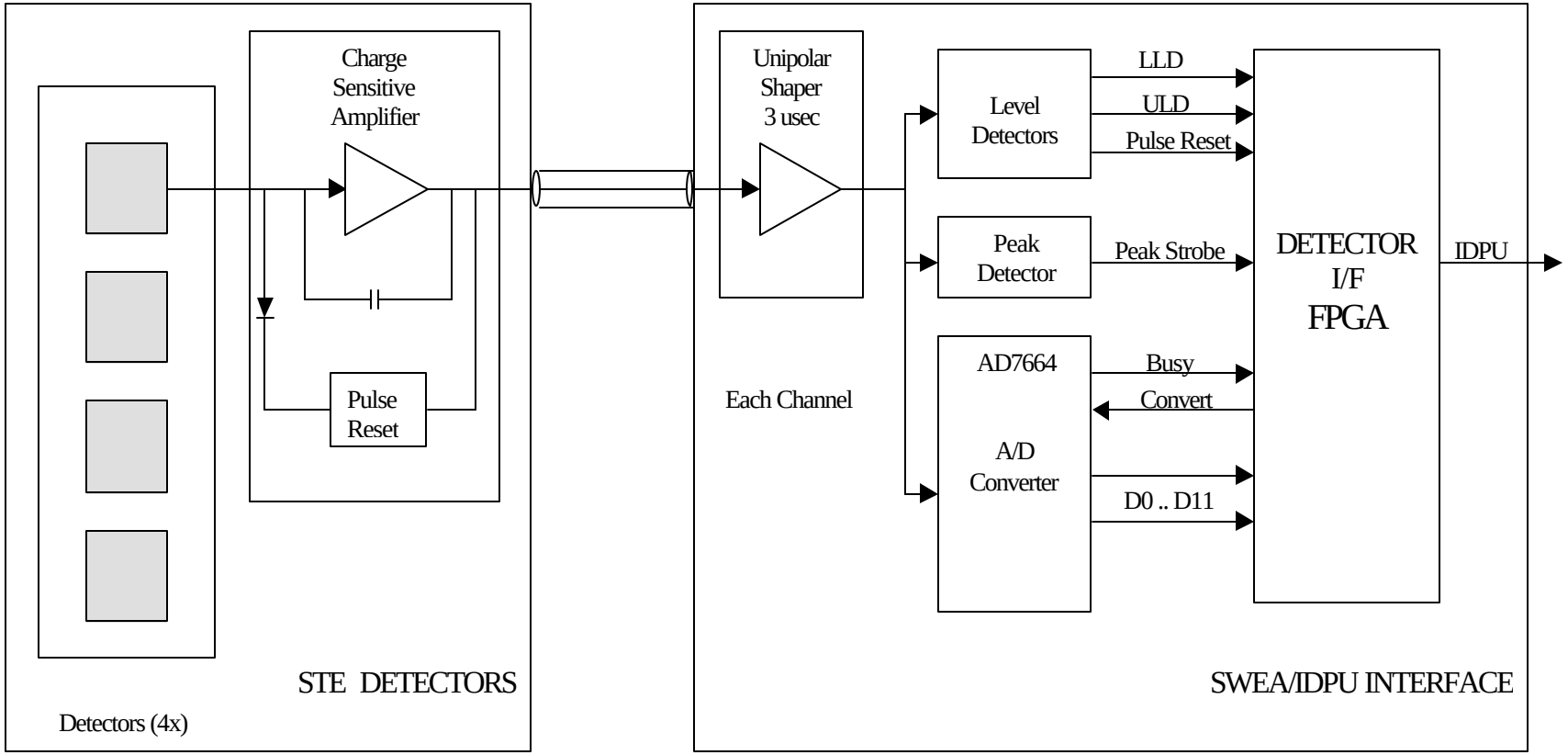


STE Detector

- **STE prototype detector**



STE Signal Chain (one of 4)



STE ELECTRONICS

- **Low Noise Charge Sensitive Amplifier (preamp)**
  - **Pulse reset topology for lowest noise**
  - **State of art 4 terminal JFETs used for input device**
  - **Detectors and input FETs passively cooled to lower noise**
- **Unipolar Shaper with 3 usec peaking time**
- **Level comparators and peak detector provide signals to FPGA**
- **FPGA generates signals that control AD7664 A/D converter**
- **Event data accumulated by FPGA**

STE Status

- ETU preamp constructed and tested
- ETU preamp (700-900eV FWHM) and prototype detector meet performance requirements
- Flight detectors supplied by LBL
- Flight detector boards in process of assembly

STE Problem Items

- **MX16 (input FET) Delivery Problem**
  - **Expect delivery 11/30**
  - **Approximately 8 weeks needed for qualification**
  - **Detector testing can proceed without qualified parts**

STE Development Plan

- An ETU STE has been fabricated and is currently in test
  - Flight detectors have been fabricated by LBNL
  - Flight detector PWB boards have been fabricated awaiting mounting of components and detectors
  - An ETU Charge Sensitive Amplifier showing 800eV noise has been designed and fabricated
  - The ETU Pulse Height Analyzer (shaper, ADC) has been designed and fabricated and will be used to test the flight detectors
  - Integrated tests with electrons shall start shortly at UCB
- Once the tests determine the best detectors and input FETs, final detector assemblies will be prepared for flight
- Two flight units shall be fabricated following CDR

STE Detector Manufacturing

- Detector Fabrication at LBNL
- Preliminary Detector Board Assembly
  - Electronic components installed and assembly cleaned
  - Detector attached to board using conductive epoxy
  - Thermal compression 1 mil gold wire used to attach detector to board
  - Wire bond process control monitor
    - Bond wire pull testing
  - QA inspection after each step
- Test Detector Board subassemblies with test jig and ETU preamp
  - Electronic noise levels
  - Response of detector to electron beam
- Test Input FETs
  - Select for low noise using test jig made from extra ETU preamp PCB
- Final assembly
  - Maintain detector cleanliness with special jig

STE Verification Plan

Verification Matrix for STEREO/IMPACT/STE

Revision Date: 11/7/2002

Revision Number: 2

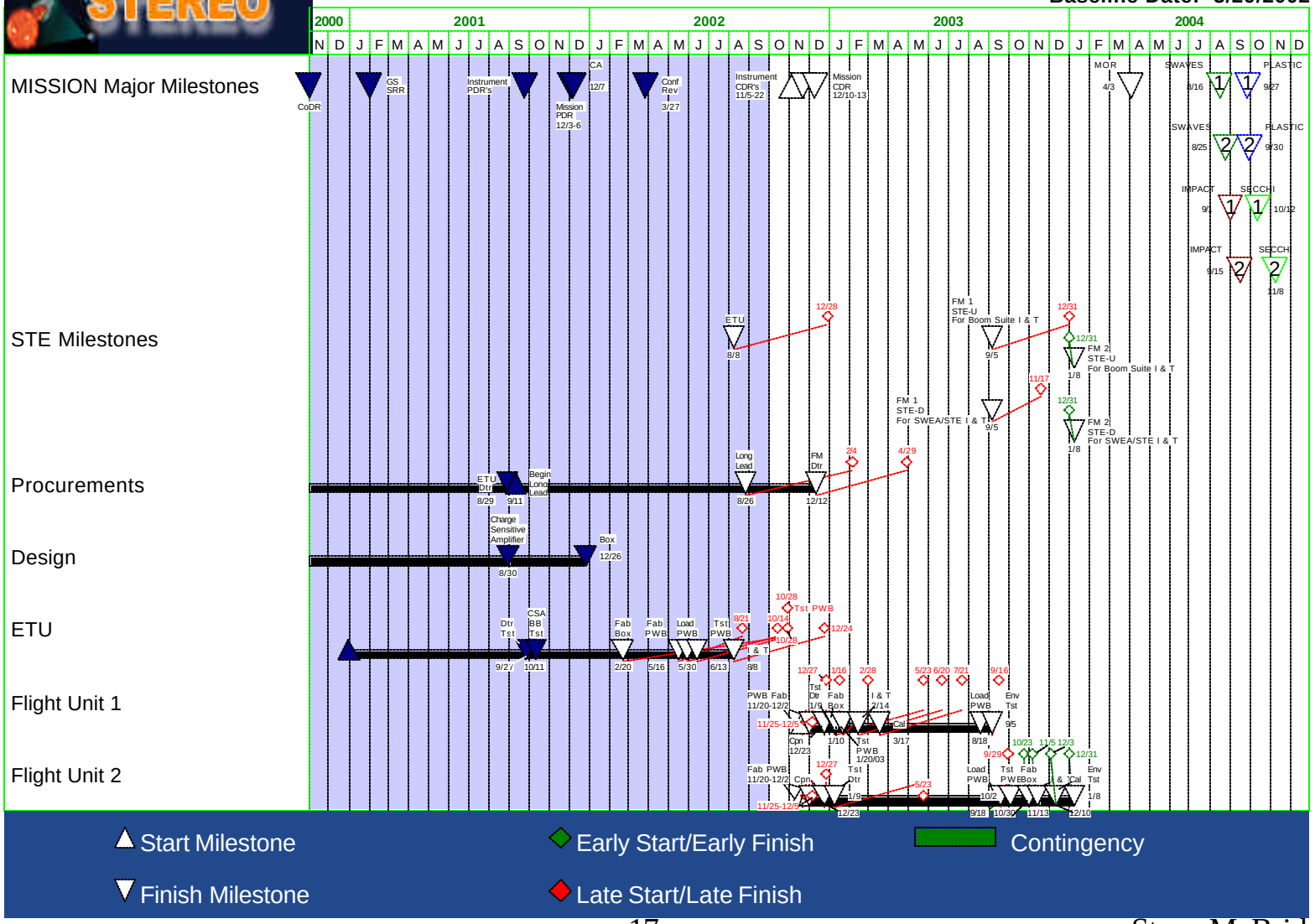
Hardware Description		Test																	
Level of Assembly	Item	Elect. test, rm. Temp	Bench Calibration	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Self Shock	Acoustics	Thermal Vacuum	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Beam Calibration	Bakeout	Contamination	Comments
C	Detector, EM	X																		
C	Detector, F	X																	X	
C	Preamp, BB	X	X																	
I	Instrument, ETU	X	X	X	X			X	A		X						X			
I	Instrument, PF (FM1)	X	X	X	X	H	H	X		X	X		X	X	H	X	X	X	X	
I	Instrument, F (FM2)	X	X	X	X	H	H	X		X	X			X	H	X	X	X	X	

Legend:

Level of Assembly	Unit Type		
		X =	Test required
		A =	Analysis
C = Component	BB	H =	Test at higher level of assembly
I = Instrument	EM	Engineering Model	
	PF	Protoflight	
	F =	Flight	

STE - Suprathermal Electron Telescope

Status Date: 9/30/02
Baseline Date: 3/29/2002



SWEA / STE Interface

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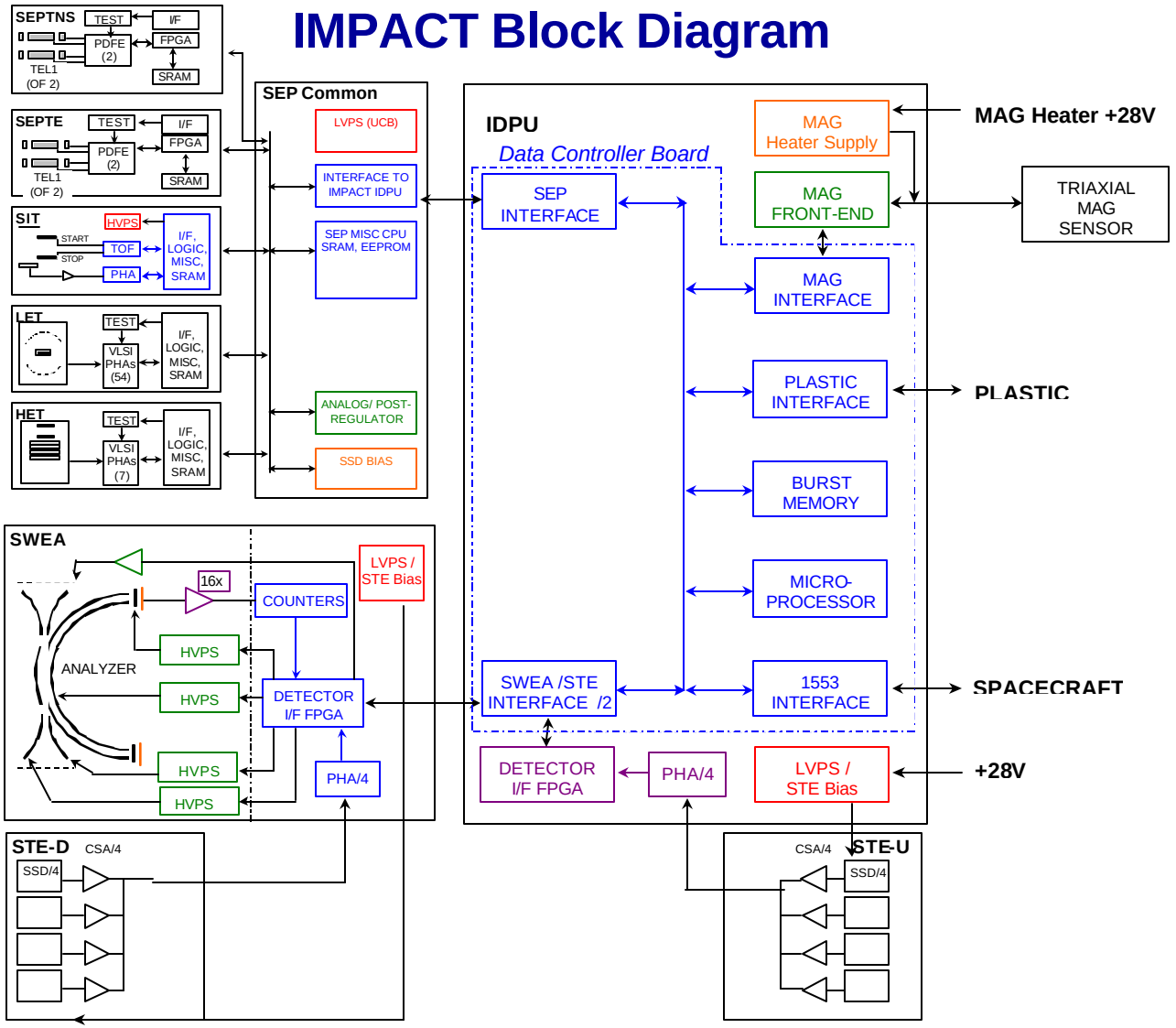
SWEA/STE Responsibilities

- **SWEA - CESR**
  - **Includes Electrostatic optics, MCP detector, HVPS, Preamps**
- **STE - UCB**
  - **Detectors and Preamp design from LBNL**
- **SWEA/STE Interface - UCB**
  - **Includes LVPS, STE Bias Supply, Controls, PHA, Accumulators, Interface to IDPU**
  - **Mounted in the base of SWEA**

IMPACT Block Diagram



STE Interface

- There are 2 STE Units per spacecraft
  - STE-U (Upstream), mounted on the sunward (fixed) end of the boom
  - STE-D (Downstream), mounted near SWEA at the end of the boom
- The STE Units contain only the detectors and preamps
- The rest of the STE-U electronics are mounted in the IDPU
- The rest of the STE-D electronics are mounted in the base of SWEA
- A common circuit design has been developed for both the SWEA and IDPU hosted electronics
  - The SWEA PWB has the SWEA Interface electronics
  - The SWEA interface electronics is not included in the IDPU-hosted PWB
- The interface electronics includes shaper, ADC, binning electronics, (collectively called the Pulse Height Analyzer, or PHA) and Serial Instrument Interface to the IDPU processor

SWEA/STE Interface Requirements, IDPU

- Interface between SWEA and STE instruments and the IDPU
- IDPU Interface:
  - Mode Commands to control instrument settings
    - No high-bandwidth requirements; instrument runs itself
  - Data Readback
    - SWEA Counters, STE Accumulator, Housekeeping
    - About 50kbps throughput required
    - Sequencer to automatically sample & read out data
  - Common timebase clock for synchronized, low-jitter, deterministic sampling
  - Common interface design with other instruments to IDPU
    - Common development
    - Common GSE
  - Minimize number of wires down IMPACT boom
  - Meet EMC requirements
- Implementation Described in IMPACT Serial Interface document

SWEA/STE Interface Requirements, SWEA

- **SWEA Interface:**
  - **Provide interface to the CESR-provided analyzer per the SWEA ICD**
  - **Voltage control for 5 analyzer voltages**
    - **MCP, VO, Analyzer, Deflector 1, Deflector 2**
    - **VO, Analyzer & Deflector Supplies have programmable waveforms**
      - **690 samples/second, 2 second period**
    - **Analyzer and Deflector supplies are referenced to VO in the supplies to simplify controls**
    - **Analyzer needs a 16-bit DAC to get sufficient accuracy (5%) over the dynamic range (3000x)**
    - **Deflector supply controls are multipliers based on Analyzer control to minimize dynamic range requirements (1% of Analyzer voltage)**
  - **Counters for Anode 16 pulses (logic pulses)**
  - **6 Voltage and one temperature housekeeping monitors**
  - **Test pulse generator (digital pulses), HV Enables (logic levels)**
  - **SWEA Cover Actuator power (switched 28V primary)**

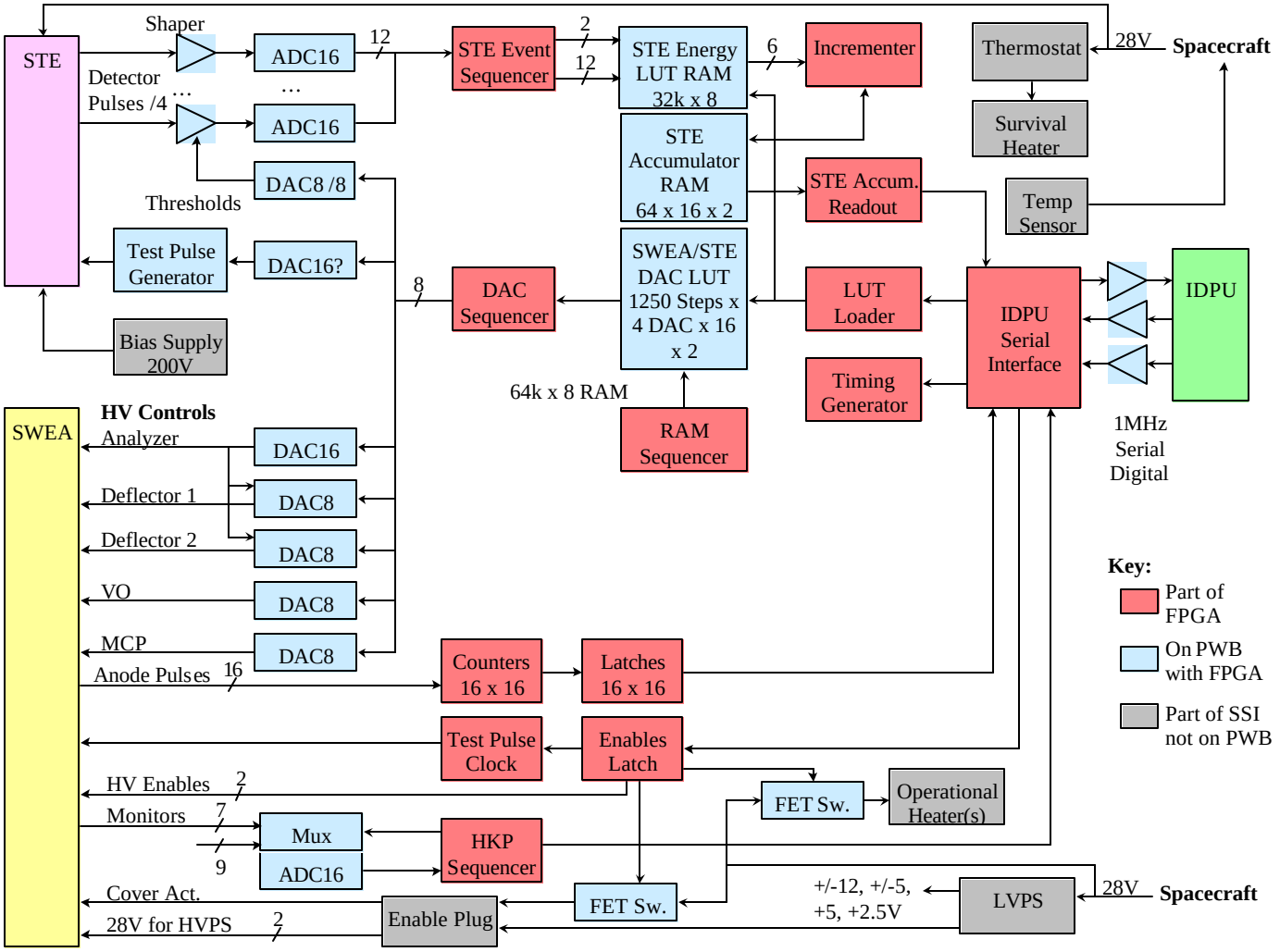
SWEA/STE Interface Requirements, STE

- **STE Interface:**
  - **4 analog chains**
    - **Charge Sensitive Amplifier inside SWEA/STE (separate for STE-U)**
    - **Shaper**
    - **Discriminator (programmable threshold)**
    - **ADC (200x dynamic range, 5% DNL -> 14-16 bit ADC)**
  - **Pulse height analyzer**
    - **Programmable Energy binning to 16 log-spaced energy channels**
    - **64-channel double-buffered accumulator (16E x 4 Det.)**
    - **>15KHz/detector throughput**
  - **Test pulse generator to test electronics**
    - **Ramped-amplitude pulse generator**
    - **Coupled into bias voltage**
    - **When pulser active, only allow events near pulse times**
  - **Temperature housekeeping monitor**
  - **Cover Actuator power (switched 28V primary)**

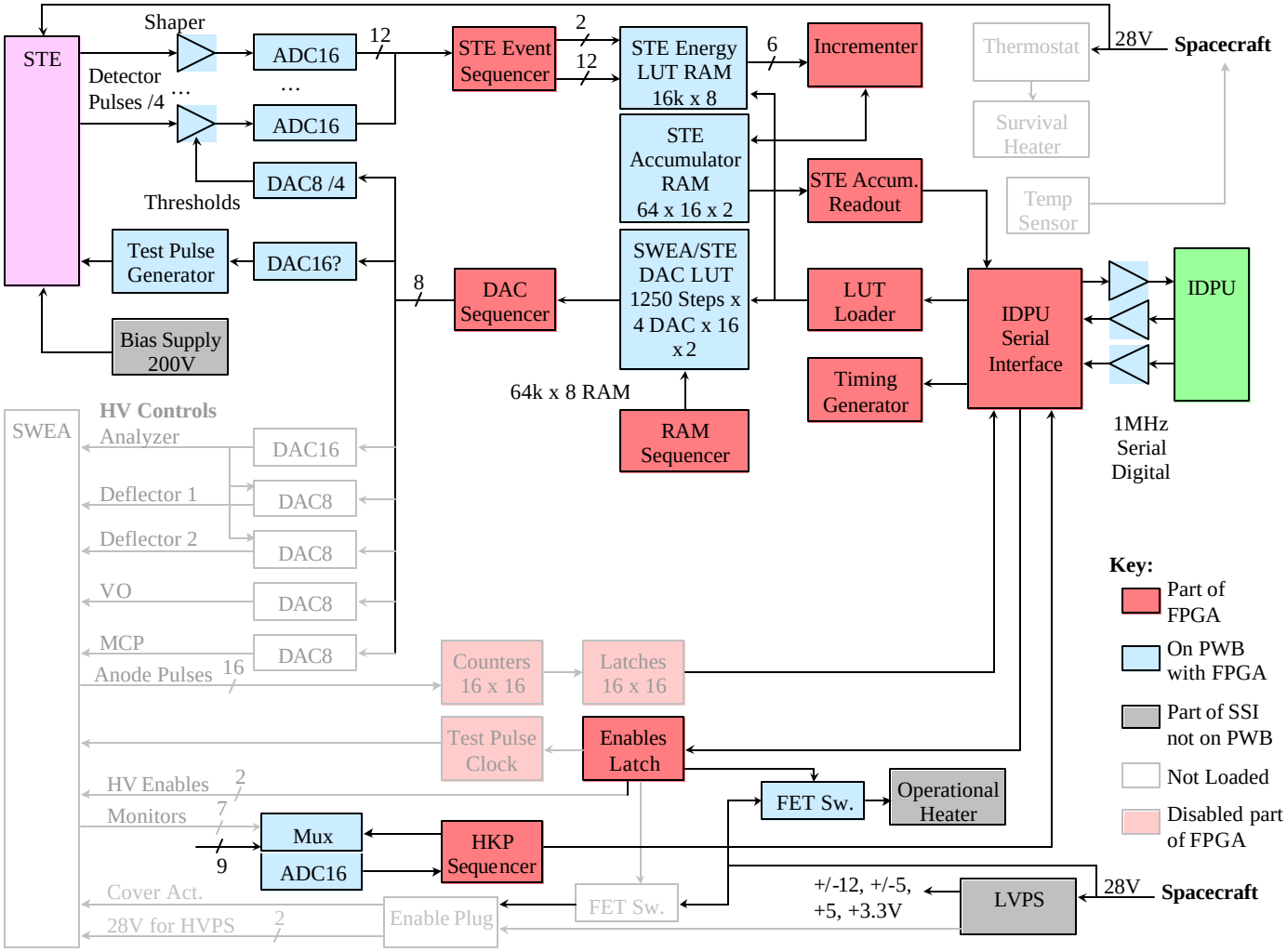
SWEA/STE Interface Requirements, Misc

- **Miscellaneous Requirements**
  - **Survival heaters (thermostatically controlled)**
    - **SWEA and STE in parallel on one spacecraft circuit**
    - **SWEA heater/thermostat part of SWEA/STE Interface**
  - **Operational Heaters**
    - **SWEA and STE heaters powered off the primary 28V**
    - **IDPU-Software Controlled FET switches**
  - **Spacecraft-monitored temperature sensor (in SWEA)**
    - **Only one to minimize wires down boom; two instrument-monitored sensors when SWEA/STE is on**
    - **Mounted in SWEA/STE Interface**
  - **Green-tag Enable Connector**
    - **Separate loops to enable:**
      - **MCP HV**
      - **Analyzer/Deflector HV**
      - **SWEA Cover**

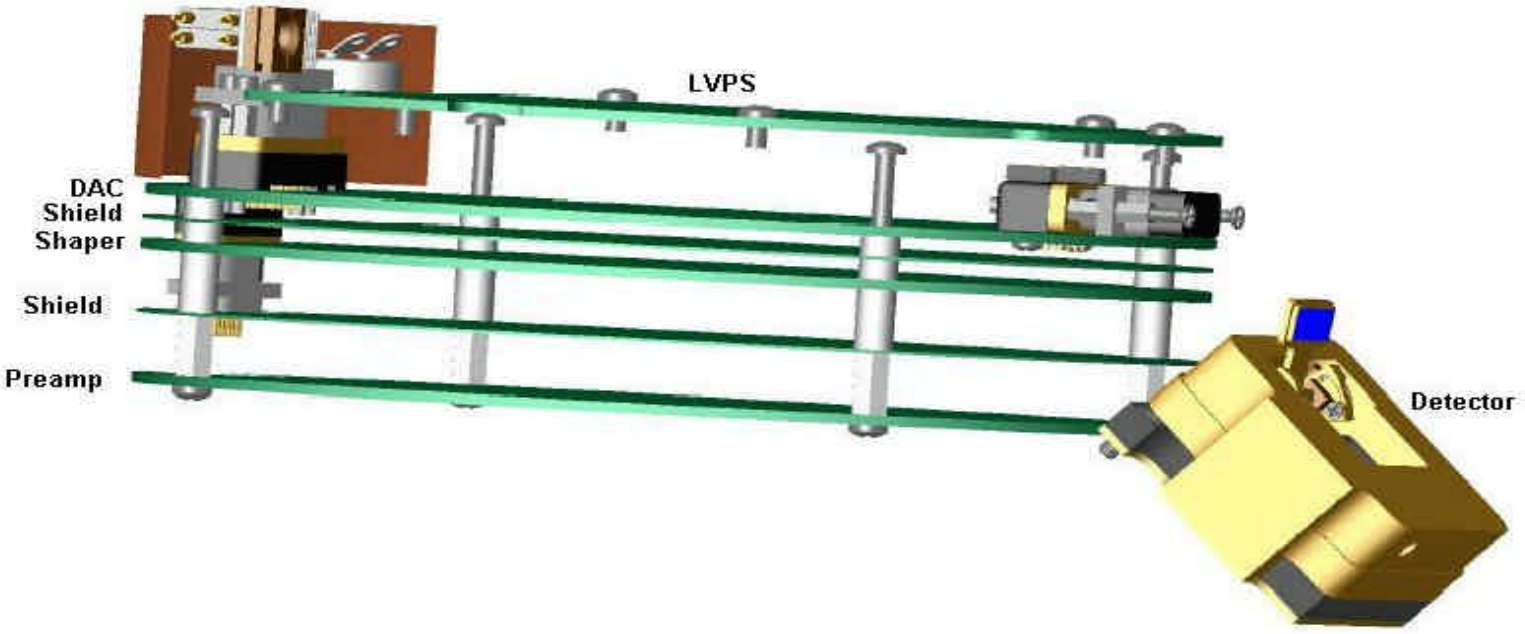
SWEA/STE-D Interface Block Diagram (In SWEA)



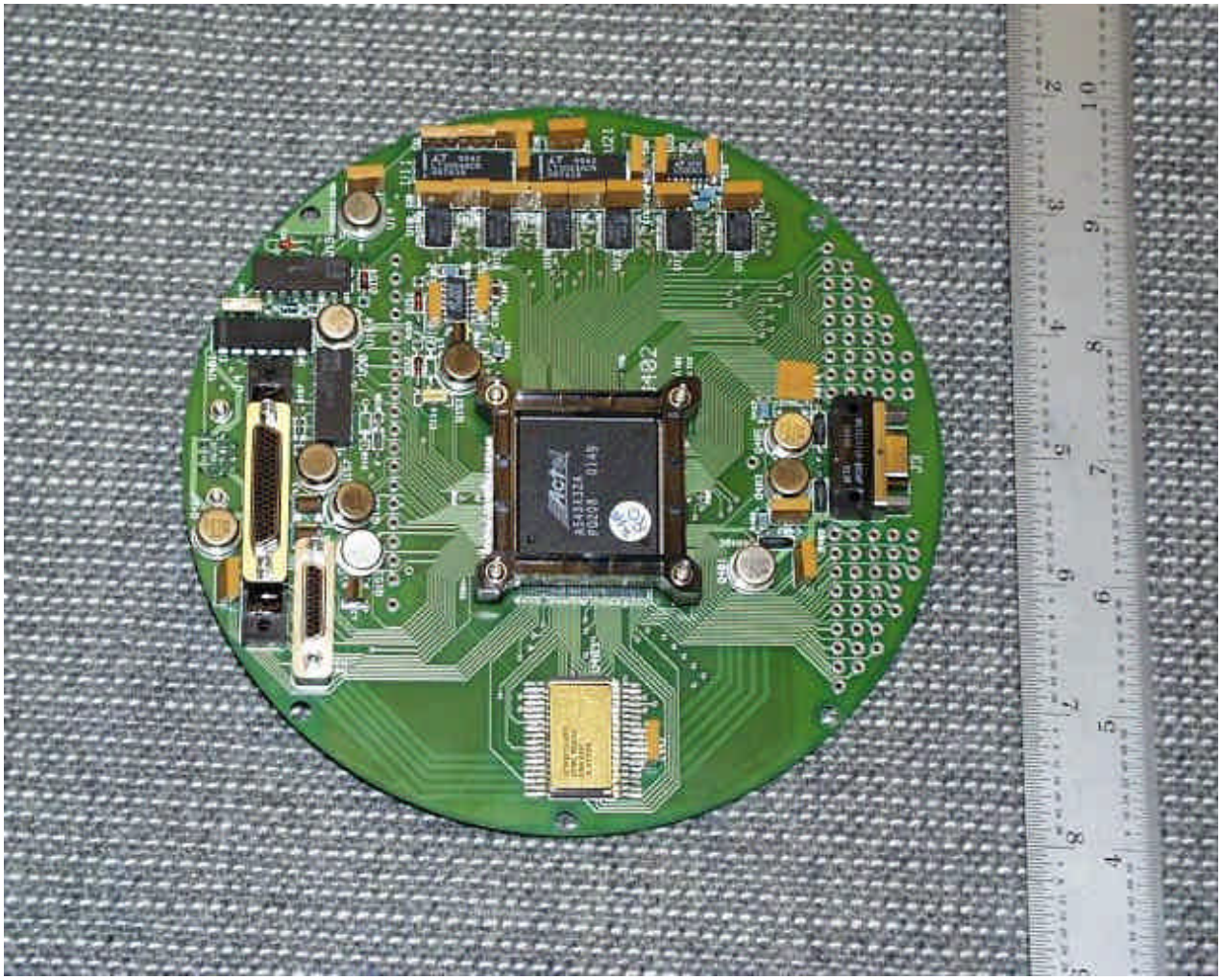
STE-U Interface Block Diagram (In IDPU)



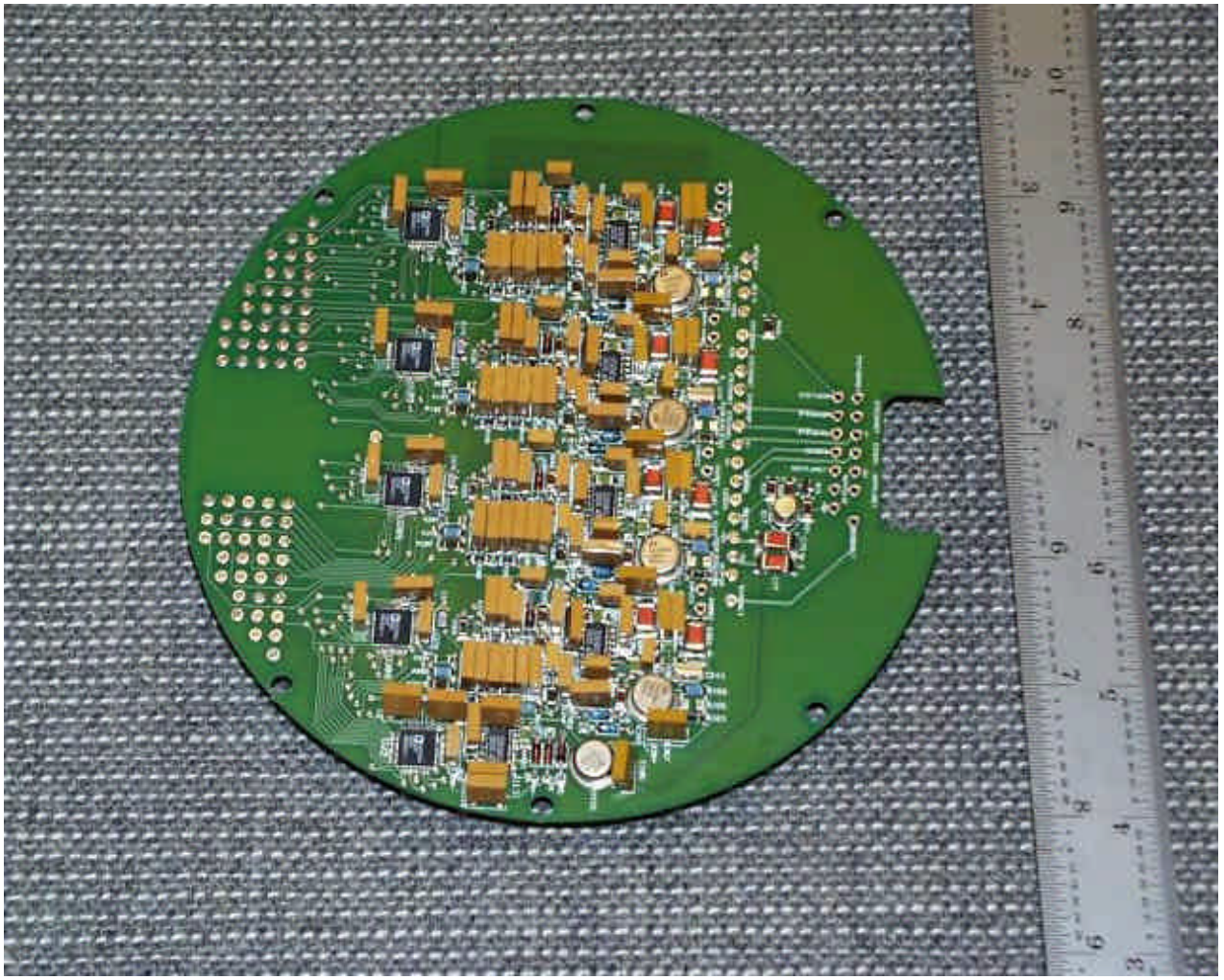
STE-D Board Assembly



DAC BOARD



Shaper Board



SWEA/STE Interface Logic

- SWEA/STE Interface Logic implemented in an FPGA, augmented with a memory for Look-up tables (LUT) and STE accumulator
- Actel RT54SX32S
  - Common FPGA selected for IMPACT team
  - Rad tollerant (100krads)
  - High Rel
- Actel designed by Elf Electronics
  - Logic has been tested on ETU board
- FPGA controls most digital interfaces
  - Interface to IDPU
  - Interface to SWEA data collection
  - Interface to SWEA sweep DACs
  - Controls door switches and heaters
  - Interface to STE shaper signals and A/D converters

SWEA/STE Interface Memory

- The memory is used for:
  - STE Energy Look-up Table
    - 12-bit ADC output plus 3-bit detector ID results in a 8-bit energy bin number
    - 32k x 8 bits
  - STE Accumulator
    - 64 Energies, 4 Detectors, 16 bit accumulators, double-buffered
    - 256 x 16 bits
    - Incrementer uses up to 4 memory cycles to increment an accumulator; Read, Increment, Write 8 LSB, repeat for 8 MSB on carry out of LSB
  - SWEA DAC Waveform Look-Up Table
    - Waveform update rate is ~690Hz
    - All DACs updated each step for simplicity
      - each DAC has its own area in RAM
      - Sequencer has set pattern of DAC addresses
    - 2 second period; sized at 1344 samples * 4 DACs * 16 bits * 2 buffers ~21.5 Kbyte (32 Kbyte reserved)

SWEA/STE Interface Memory (Continued)

- **Total Size requirement ~ 66.6Kbytes**
  - **Uses common SRAM with IDPU - 512Kx8**
  - **Command to select which of four 128K sections used**
- **Access Rate:**
  - **STE Accumulation: 15,000 events/sec/det * 4 Det * 5 cycles/event = 300,000 cycles/second (includes LUT & Accumulate)**
  - **STE readout: 1MHz serial bitrate to IDPU (burst) = 63,000 cycles/second max (Note: reset accumulator following readout of full accumulator, so no bandwidth impact)**
  - **LUT Write: 1MHz serial bitrate from IDPU (burst) = 125,000 cycles/second max**
  - **SWEA LUT readout; Up to 5 DAC bytes need to be updated in one sample interval (625Hz) = 3,125 cycles/second MAX (Note: DACs are double-buffered)**
  - **Total bandwidth required: 491KHz**
  - **Using 1 RAM cycle per 1MHz clock, can allocate 8 fixed time slots at 125KHz: 5 for STE Accumulation, 1 for STE readout, 1 for LUT write, and one for SWEA LUT readout (allows up to 30,000 STE events/sec/det)**

SWEA/STE Interface Misc

- Power Switches
  - SWEA heater (PWM) and SWEA door actuator
  - STE door open and door close actuators
  - sense switches for STE door position
- Power Supply Control
  - SEU detection
  - Power supply switches controlled by FPGA
  - FPGA removes all other voltages from affected circuits
- Analog Housekeeping
  - Multiplexed analog inputs
  - FPGA controls A/D and input selection
- MCP Voltage
- SWEA Test Pulser
- STE Test Pulser

SWEA/STE Interface Misc (Continued)

- STE Thresholds
  - set minimum event size for each channel
- STE channel enables
  - can disable noisy channel
- STE rates accumulation
  - LLDs, ULDs, Pulse Resets
- Subsystem Enables
  - Counters
  - Housekeeping
  - STE
  - Rates
  - SWEA (sweep and counter readout)

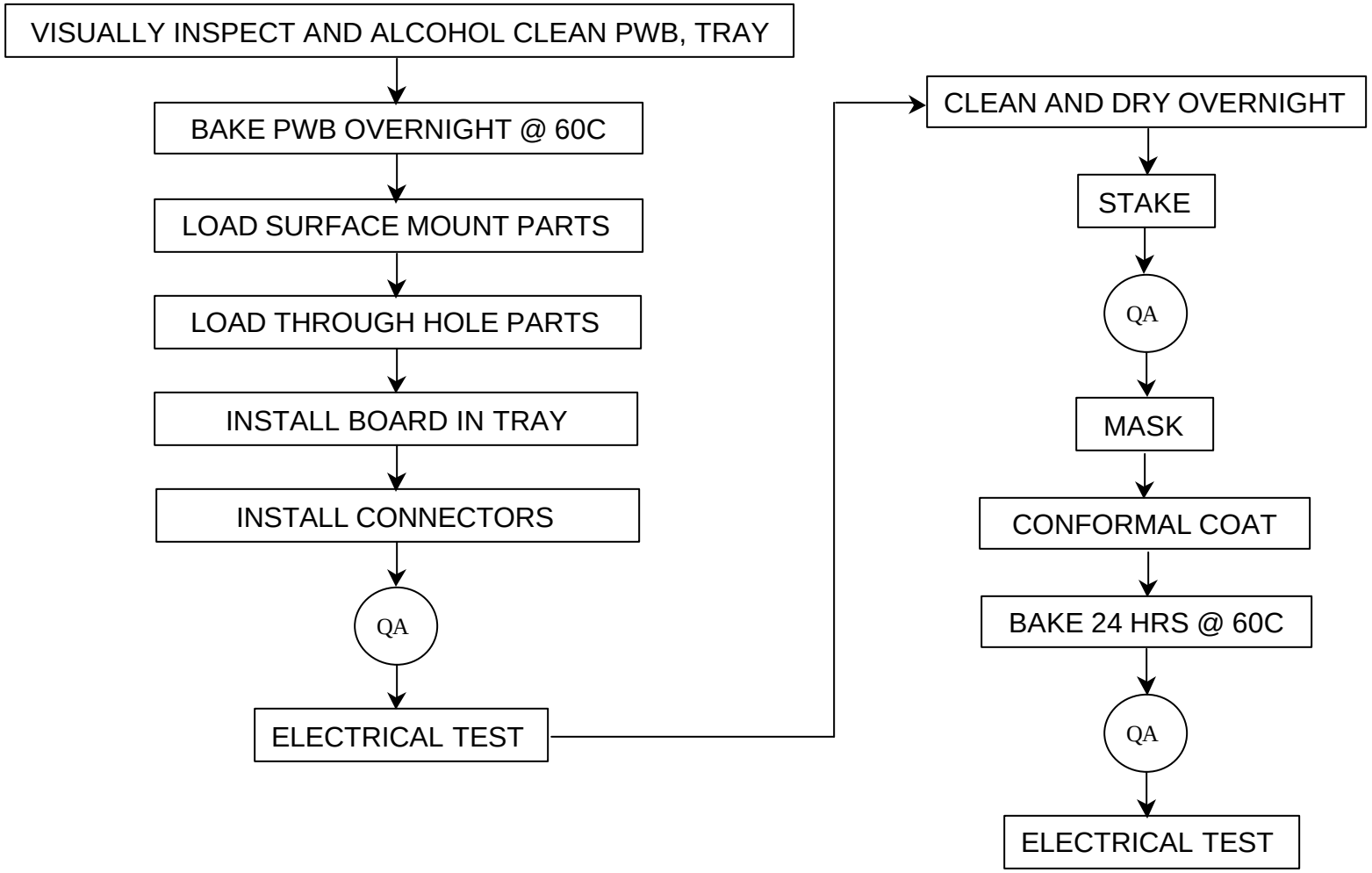
STE-U Interface

- Same electrical design as SWEA/STE interface
- Parts used solely for SWEA eliminated on layout
- IDPU can selectively enable only STE subsystems
- PCB in IDPU housing with different form factor

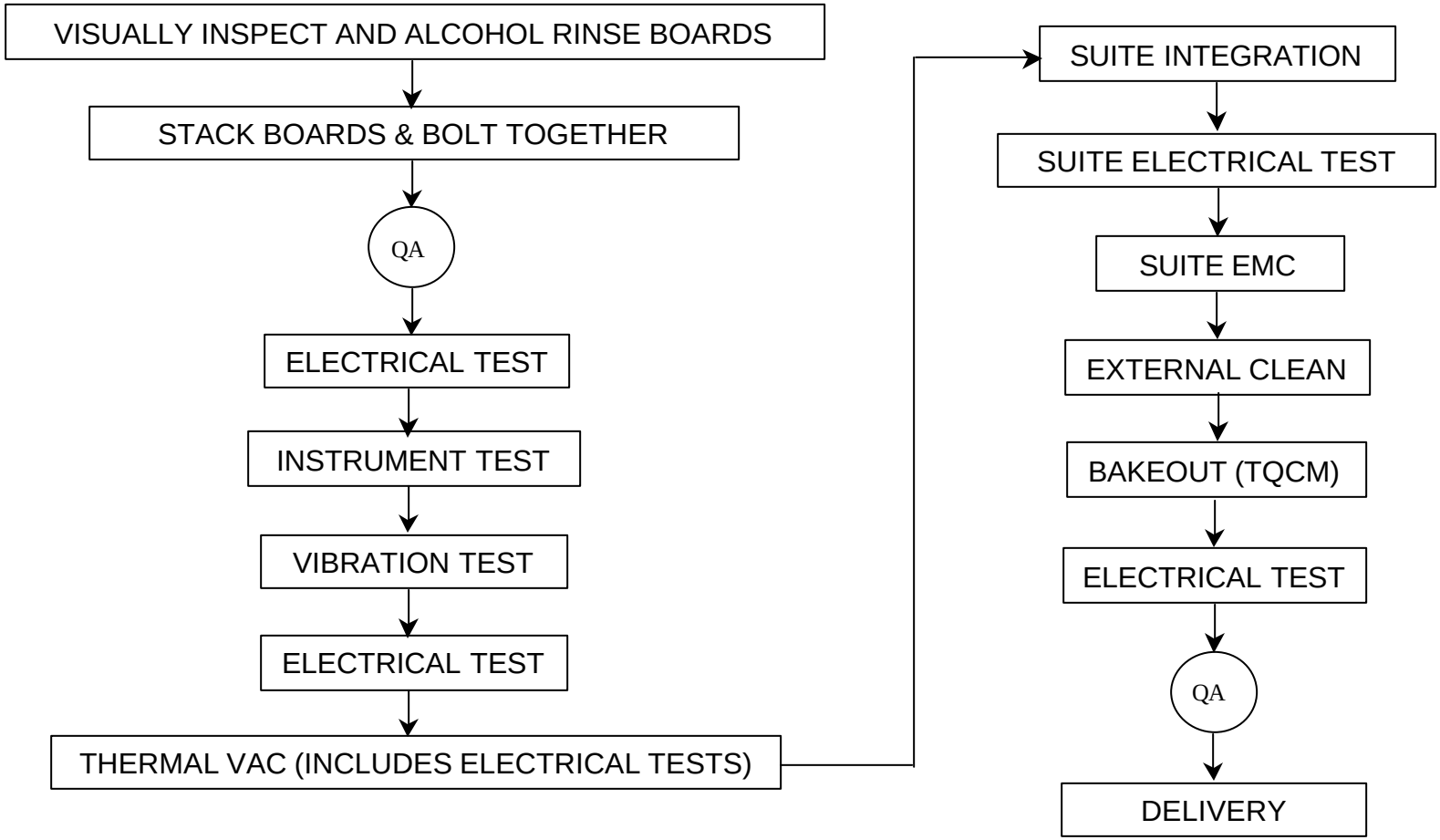
SWEA/STE Interface Status

- ETU SWEA/STE-D constructed and all subsystems tested
- Testing with ETU SWEA in progress
- STE-U PWB in layout

DAC,Shaper and Preamp PWB Manufacturing Flow



DAC,Shaper and Preamp Integration and Test Flow



SWEA/STE Interface Development and Verification Plans

- An ETU of the SWEA/STE-D Interface has been built
  - FPGA developed by ELF
  - Interface tests with STE, SWEA, and IDPU
  - Support SWEA & STE Functional & performance tests at UCB
- STE-U Interface is in layout
  - Same design as STE-D minus some function
  - Different form factor to fit into IDPU housing
- Four Flight Units shall be developed and tested at UCB
  - Two for IDPU, without SWEA Interface
  - Two with SWEA Interface
- The interface circuits shall be be functionally tested with the STE ETU and Flight Units per the STE verification plan
- The interface circuits shall be environmentally tested with the IDPU and SWEA units respectively per their verification plans

SWEA/STE Problem Items

- **AD7664 Qualification**
  - **Question about Radiation especially SEU vulnerability**
  - **LT1604 possible backup**
    - **higher latchup threshold (used on HESSI)**
    - **increased power consumption**
    - **slower**
    - **requires more control signals**
    - **ACTEL logic modification needed**

- **UT9Q512 Qualification**
  - **Possible SEU latchup problem**
  - **Goddard to perform radiation test**
  - **Several other ram possibilities, PCB layout change needed**

SWEA/STE Problem Items (continued)

- **LTC1599 DAC Failed Radiation Test**
  - **Main Sweep DAC has high accuracy requirements**
  - **Search for alternative parts (16 bit DAC)**
    - **Goddard will perform preliminary radiation test on candidates before additional qualification**
    - **Requires FPGA modification to adopt different DAC interface**
    - **ETU no longer representative of final design**
  - **Investigate cascaded DAC design**
    - **two 12 bit DACs or gain switch**
    - **accuracy requirements are for relative accuracy**
    - **approach could meet requirements**

SSI - SWEA/STE Interface

Status Date: 9/30/02
Baseline Date: 3/29/2002