SEPT Operation Control And Data Processing Requirements

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VERSION 3.0

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1 Objectives

The purpose of this document is to describe the foreseen operation control of the SEPT instrument by the SEP central processor. The document is based on the Engineering Model of the instrument. Some minor differences exist between the engineering model and the flight model, they will indicated accordingly in section 17.
Rem: to improve clarity, the present document should be printed in color.

2 Revision History

- Version 0.1 to 0.4: Sept-2002 – Preliminary drafts.
- Version 0.5: Sept 2002- First release
- Version 1.0: Oct. 2002: includes comments of R. Mueller-Mellin +
    - Spelling corrected
    - Addition of Acronyms
    - Reaction to interrupts: separate section has been made to introduce the status word.
    - Calibration mode detailed.
    - Nominal mode detailed
    - Detail on timing specifications
    - No separation between nominal mode and beacon mode at the command level.
    - Look up table specifications updated.
    - The use of the command cClearIrq has been reviewed in the pre/post operation sequence.
    - Correction of the calibration configuration sequence (9.4)
    - Data processing requirement for nominal, calibration and test generator merged.
    - Binning indexes for the beacon mode.
- Version 1.1: Oct 2002
    - Status word extended to contain operational mode designator
    - last row changed to >2200.
- Version 2.0: November 2002
    - The document is now based on the EM FPGA (third prototype release)
    - Details added
    - All modes and sequences refined to reflect the agreement on the absence of instantaneous interrupt handling by the SEP-DPU
- Version 2.1: February 2003 (not released)
    - Paragraph 6.1: asynchronous serial link waveform example added.
- Version 3.0: May 2003
    - Interruption table modified
    - Single counter description updated
    - Nominal mode updated
    - Calibration mode description included
    - Test generator mode description included
    - Commissioning mode description included
    - Initialization sequence updated
    - cEnPDFE bit pattern corrected in telescope power on sequence, A alone power on sequence, B alone power on sequence.
    - Test generator configuration sequence included
    - Bias voltage setting sequence A alone suppressed
    - Bias voltage setting sequence B alone suppressed
    - Status word updated
    - Time stamp and priority section modified
    - PDFE configuration error handling section modified
    - SEP health monitor section updated
    - Instrument power on flow chart modified
    - Calibration mode flow chart updated
    - Test generator flow chart updated
    - Data rate for nominal rate updated
    - Preliminary temperature sensor calibration curves (Engineering model) included,
    - Mode and sequence identifier table modified.

3 Applicable Documents

AD1 SEPT - FPGA Data Sheet – SEPT-001-04, version 1.2

AD2 RS-232 EIA/TIA Standard

AD3 Particle Detector Front End, Preliminary datasheet, IMEC, Nov. 28, 2000

AD4 CCSDS 301.0-B-2: Recommendation: Time Code Formats, Blue Book, Issue 2

4 Acronyms and Abbreviations

CS Center Segment (or main channel)
FPGA Field Programmable Gate Array
GR Guard Ring (or coincidence channel)
IR Interrupt Register
LUT Look Up Table
PDFE Particle Detector Front End
RAM Random Access Memory
SEP Solar Energetic Particles
SEPT Solar Electron Proton Telescope
SSD Solid State Detector
TBD To be defined
TBC To be confirmed
TBA To be added

5 Overview

5.1 Introduction

SEPT consists of two identical electronic units (SEPT-NS and SEPT-E) per STEREO spacecraft dedicated to the measurements of electrons (from 20 keV to 400keV) and ions (20 keV to 7 MeV). Each electronics unit analyses the signals of four solid-state detectors (SSD) and four corresponding guard rings. The four detectors are integrated in two opposite oriented telescopes, either in north-south (NS) or ecliptic (E) orientation. Each detector is connected to a PDFE (Particle Detector Front End) ASIC. Additional 9 housekeeping signals (+ 1 redundant) per unit are sampled and transferred to SEP-DPU as well as general status. A specific test generator permits control of the electronics in flight. The low-level operation of SEPT electronics is controlled by a specific FPGA. The high level operation of SEPT is controlled by the SEP central processor by means of commands sent on the serial interface. The same serial interface is used to transfer all scientific, calibration and housekeeping data from SEPT to SEP-DPU.

All the modes of operation of SEPT are based on a one-minute cycle.

The block diagram in Figure 1 shows more details for one of the two SEPT telescope units (SEPT-NS and SEPT-E).

5.2 Block Diagram

One SEPT unit is divided into two telescopes (A and B), each telescope can be independently switched ON/OFF. In case of latchup in one telescope, only the corresponding telescope is automatically switched-off by the FPGA.
In addition to handling the detection of the charge particles impinging on the detectors, the PDFEs are also used to digitize the housekeeping:

- PDFE0: 4 leakage currents (related to the detectors of telescope A)
- PDFE 1: temperature TA (AD590: see section 16)
- PDFE 2: 4 leakage currents (related to the detectors of telescope B)
- PDFE 3: temperature TB (AD590: see section 16)

Only one of the two temperature sensor values shall be transmitted in the HK flow (by default TA). TB is only used when:

- An anomaly has been detected on the values of TA
- Telescope A is switched-off because of a latchup

Two RAMs (each being divided into 2 buffers) are used to store the recorded events (one per telescope).. However it has to be noted that these RAMs cannot store the events corresponding to two consecutive 1-minute measurement cycles. If unread, the data corresponding to the measurement cycle n are overwritten by the data corresponding to the cycle n+1, this feature means that a proper timing has to be defined between SEPT and SEP DPU to transfer the data. Indeed, during the transfer of the data, no event accumulation can take place, resulting in a “dead time” in the scientific acquisition”. This dead time shall be minimized.
A counter placed in the FPGA is used to record all the events which occurred on a specific channel during a measurement.

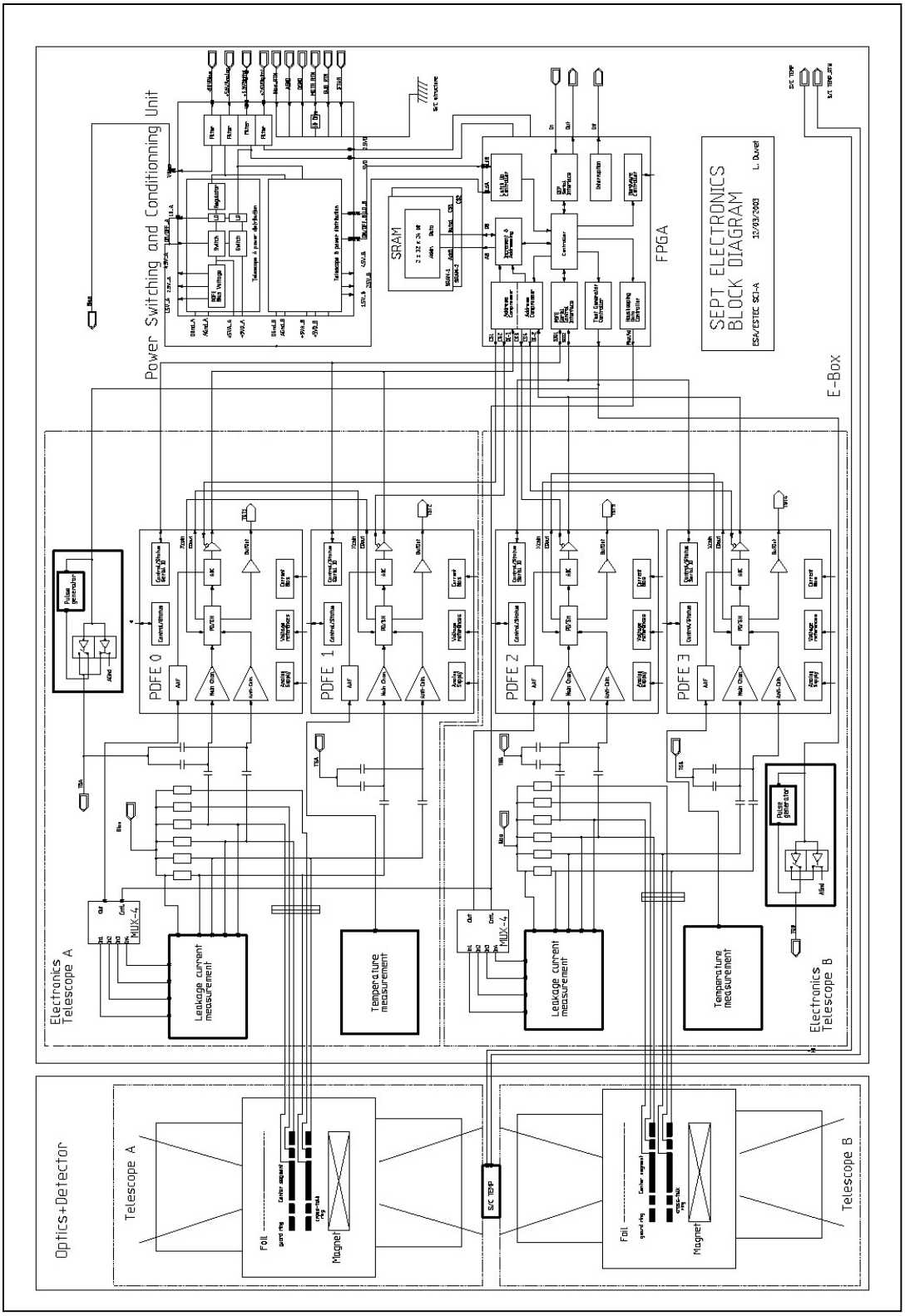

Figure 1 SEPT Block diagram

5.3 Housekeeping

The following table lists the housekeeping channels in each SEPT unit[1].

Housekeeping Variable	Description
HK_T	Temperature of the electronics
HK_CS0	Leakage current of center segment linked to PDFE0
HK_CS1	Leakage current of center segment linked to PDFE1
HK_CS2	Leakage current of center segment linked to PDFE2
HK_CS3	Leakage current of center segment linked to PDFE3
HK_GR0	Leakage current of guard ring linked to PDFE0
HK_GR1	Leakage current of guard ring linked to PDFE1
HK_GR2	Leakage current of guard ring linked to PDFE2
HK_GR3	Leakage current of guard ring linked to PDFE3

Table 1: Housekeeping channels that will be measured.

HK_T shall be used by the SEP central processor to control the operational heater (see remark on temperature in the introduction)
Note: the main channel of a PDFE is connected to the central segment (CS) of one detector; the coincidence channel is connected to the corresponding guard ring (GR).

[1] A SEPT unit will always refer to SEPT-NS or SEPT-E

6 Communication specifications

6.1 Asynchronous serial link

The communication between the SEPT instrument and the SEP central processor is made through an asynchronous serial link (compliant with AD2) with the parameters shown in Table 2, and Table 3.

Setting	Value
Baud rate	57600
Start bit	1
Data bits	8
Stop bits	2

Table 2: Serial Communications settings

The UART is built inside the SEPT FPGA. The bit rate for the transceiver is based on a 4.5 MHz internal clock (derived from the 18 MHz external clock).
The output rate is 57 692.3 baud (within 1.6% of 57600). This is derived by dividing 4.5 MHz with 78. On receipt, the FPGA can tolerate up to 10 % but this figure should be limited to 2 % to prevent potential errors.

Asynchronous RS232 type format	start	D0	D1	D2	D3	D4	D5	D6	D7	Stop	Stop
	first	LSB							MSB		last
General data format i={0,n}		8*i+7	8*i+6	8*i+5	8*i+4	8*i+3	8*i+2	8*i+1	8*i		
		last							first		

Table 3 Asynchronous bit serial data format

The table 3 defines the translation between the Asynchronous bit serial data format and the general data format used elsewhere in this document and in AD1. The Least significant bit is transmitted first.
Ex: cClearIrq has the code 01110000 in the general data format (B0 to B7). The RS232 bits are sent in the D0 to D7 order as shown on Figure 2, besides in the case of cClear Irq, i=0 since 1 byte only is sent, then D0=B7, D1=B6….D7=B0. Consequently, the pattern 00001110 would be observed on the line with an oscilloscope (without the start and stop bits). The interface is independent of the transmitted data contents. No handshaking is required.

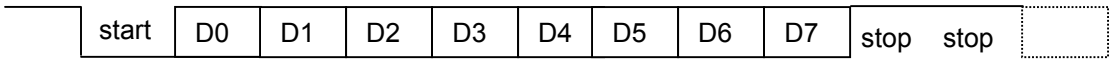

Figure 2 Serial link waveform format (at the connector level)

Positive logic is used. To avoid any ambiguity, the following figure show one particular example of waveforms measured at the SEPT connector.

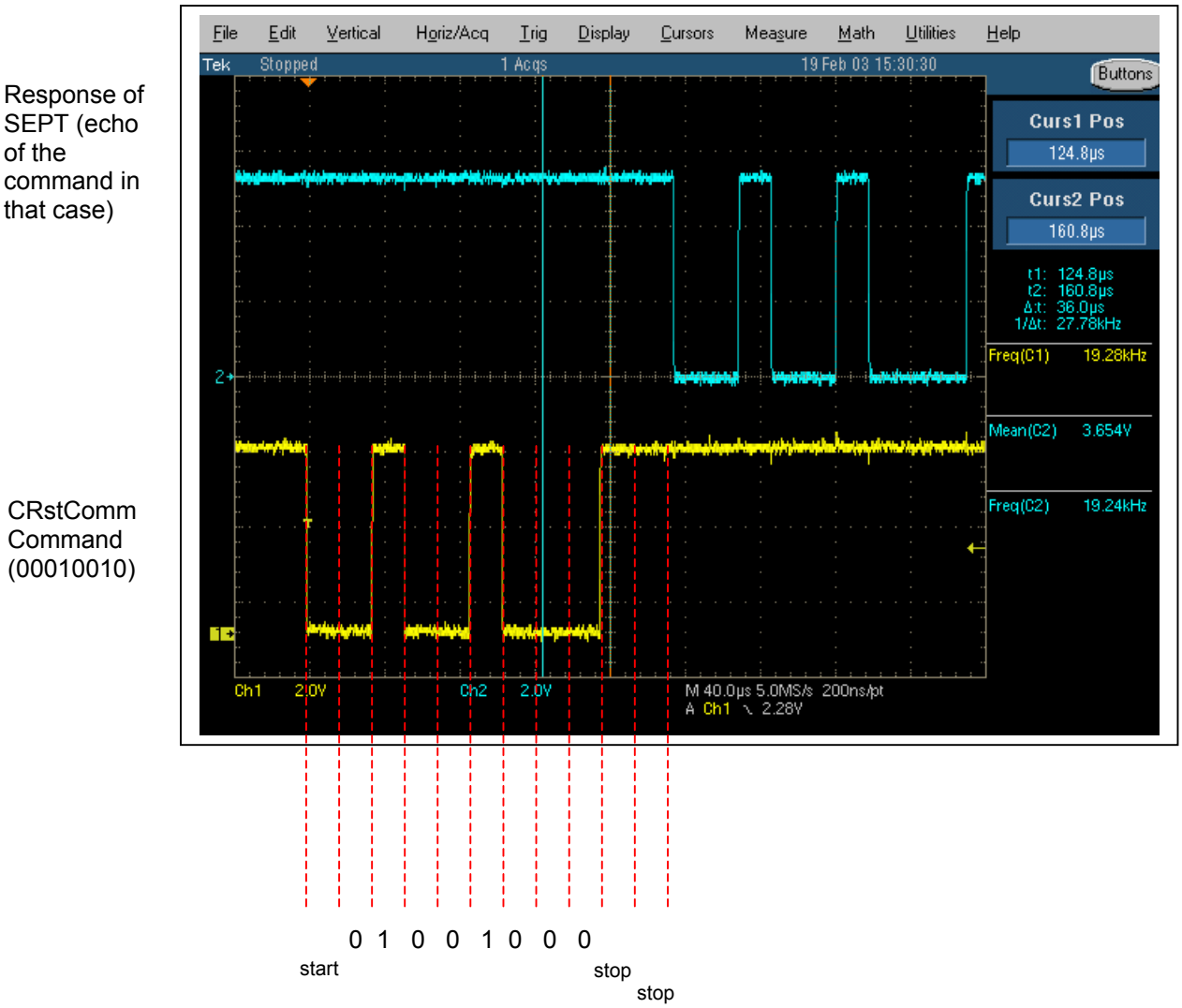

Figure 3 Example of waveform for the asynchronous link at the SEPT connector level.

6.2 Interrupt line

A direct digital line exists between the SEPT instrument and the SEP processor (SEPT-E-LATCHUP and SEPT-NS-LATCHUP). This line is used for interrupt notification (see section 11) but will not be used for the interface with SEP DPU.

6.3 Command structure: parameters and arguments

All commands consist of an 8-bit pattern. Up to 3 bits in this pattern can be used as **parameters**, for addressing purposes (PDFE or telescope) and configuration. When a command consists only of a single byte, it is said to have no arguments. Some commands, such as cConfPDFE, have **arguments**. These arguments consist of one or several bytes sent after the 8-bit pattern command. It is assumed that there is at most 1.8 ms between the receipt of a command byte and subsequent argument on the input interface, otherwise a time-out response (rTimeOut, see appendix A) will be generated and the transmission will be aborted.

A command response always contains the command itself. This feature enables to check that the SEPT FPGA has properly received the command. Consequently, before the next command is

sent in a command sequence, the SEP processor shall always check that the previous command has been properly echoed. In the case of a non-properly echoed command the action to be taken is described in section 6.5. The structure of the response to a command depends on the command itself, detailed specifications for each command can be found in appendix 19.5. Unless specifically required, only the length of the response should be checked and not the content.

6.4 BREAK response

In addition to transmitting and receiving bytes, the serial interface can also generate a break code on the occurrence of an interrupt (see section 11). This is done by transmitting a zero start bit, one byte with the data filled all zero, two stop bits being zero and an additional zero bit to violate the nominal protocol.
The break signal is sent nearly simultaneously with the assertion of the external interrupt signal, only delayed by any ongoing byte transmission.
The SEP DPU should ignore the BREAK signal.

6.5 Communication errors

The following table lists the response issued by the SEPT FPGA whenever a problem occurs at the communication level.

rUnknown	Send back 00000011 whenever an unknown command is sent
rTimeOut	Send back 00001111 whenever a time out has occurred while waiting for an argument.

Table 4 Communication troubleshooting response

Whenever a rUnknown and rTimeOut or a non-properly echoed command is encountered by the SEP DPU, the cRstComm should be sent to reset the communication and the last command should be sent again. This operation can be repeated 1 more time. If after these 2 attempts, the problem is still present, the emergency switch-off sequence should be applied followed by the initialization sequence so that the current operation can be reestablished **automatically**. A maximum of two reboot for communication error should be tolerated everyday. The error should be reported only if the communication error has not been solved.

7 Interrupt register

The status of the instrument can be described by a certain number of bits contained in the interrupt register of the SEPT FPGA:

Bit 0	Event propagation enabled on PDFE 0 and 1 (set to 1 when PDFE operational)
Bit 1	Event propagation enabled on PDFE 2 and 3 (set to 1 when PDFE operational)
Bit 2	Time Alarm interrupt, latched
Bit 3	Saturation interrupt on PDFE 0 and 1, latched
Bit 4	Saturation interrupt on PDFE 2 and 3, latched
Bit 5	Not used
Bit 6	PDFE 0 or 1 error or latchup during measurement
Bit 7	PDFE 2 or 3 error or latchup during measurement
Bit 8	PDFE 0 configuration error, latched

Bit 9	PDFE 1 configuration error, latched
Bit 10	PDFE 2 configuration error, latched
Bit 11	PDFE 3 configuration error, latched
Bit 12	PDFE 0 or 1 analogue latchup, latched
Bit 13	PDFE 0 or 1 digital latchup, latched
Bit 14	PDFE 2 or 3 analogue latchup, latched
Bit 15	PDFE 2 or 3 digital latchup, latched

Table 5 Status register

Bits 2 to 15 are set to 1 whenever the corresponding event has happened. Bit 0 and bit 1 are set to 1 when the corresponding pair of PDFE is operational.
The whole register is accessible through the `cClearIrq` command. This command also clears all the latched interruption bits in the interrupt register.

Note: The cStatPDFE command gives access to the current PDFE status bits (from bit 8 to bit 15) unlatched, however this command will not be used.

8 Operational modes

8.1 Settings Look Up Table

A lookup table should be stored in the mass memory of the SEP processor. It shall contain all settings needed to properly operate the SEPT instrument and the binning parameters for the beacon mode (see 14.2). The LUT can be divided into two parts:

- LUT_SETTINGS
- LUT_BEACON

The following settings are needed (see AD3 for more details):

Name	Description	Size (bits)
ACC_TIME	Accumulation time	24
G_PDFE0-SEPT-E	Conversion gain adjustment PDFE0-SEPT-E	5
G_PDFE1-SEPT-E	Conversion gain adjustment PDFE1-SEPT-E	5
G_PDFE2-SEPT-E	Conversion gain adjustment PDFE2-SEPT-E	5
G_PDFE3-SEPT-E	Conversion gain adjustment PDFE3-SEPT-E	5
G_PDFE0-SEPT-NS	Conversion gain adjustment PDFE0-SEPT-NS	5
G_PDFE1-SEPT-NS	Conversion gain adjustment PDFE1-SEPT-NS	5
G_PDFE2-SEPT-NS	Conversion gain adjustment PDFE2-SEPT-NS	5
G_PDFE3-SEPT-NS	Conversion gain adjustment PDFE3-SEPT-NS	5
ML_PDFE0-SEPT-E	Main event detection level PDFE0-SEPT-E	8
ML_PDFE1-SEPT-E	Main event detection level PDFE1-SEPT-E	8
ML_PDFE2-SEPT-E	Main event detection level PDFE2-SEPT-E	8
ML_PDFE3-SEPT-E	Main event detection level PDFE3-SEPT-E	8
ML_ PDFE0-SEPT-NS	Main event detection level PDFE0-SEPT-NS	8
ML_ PDFE1-SEPT-NS	Main event detection level PDFE1-SEPT-NS	8
ML_ PDFE2-SEPT-NS	Main event detection level PDFE2-SEPT-NS	8
ML_PDFE3-SEPT-NS	Main event detection level PDFE3-SEPT-NS	8
CL_PDFE0-SEPT-E	Coincidence event detection level PDFE0-SEPT-E	8
CL_ PDFE1-SEPT-E	Coincidence event detection level PDFE1-SEPT-E	8
CL_ PDFE2-SEPT-E	Coincidence event detection level PDFE2-SEPT-E	8
CL_ PDFE3-SEPT-E	Coincidence event detection level PDFE3-SEPT-E	8
CL_ PDFE0-SEPT-NS	Coincidence event detection level PDFE0-SEPT-NS	8
CL_ PDFE1-SEPT-NS	Coincidence event detection level PDFE1-SEPT-NS	8
CL_ PDFE2-SEPT-NS	Coincidence event detection level PDFE2-SEPT-NS	8
CL_ PDFE3-SEPT-NS	Coincidence event detection level PDFE3-SEPT-NS	8

Table 6 LUT_SETTINGS

The values stored in the LUT_SETTINGS will be used by the cConfPDFE and cSetTimer commands.

The LUT_BEACON shall contain the binning parameters for the beacon mode. The binning parameters are related to Table 27 and should be stored as 5 bit values with the following naming.

Name	Default value
Electron_bin1	1
Electron_bin2	5
Electron_bin3	8
Electron_bin4	13
Electron_bin5	17
Ion_bin1	1
Ion_bin2	8
Ion_bin3	20
Ion_bin4	30
Ion_bin5	31

Table 7 LUT_BEACON

The lookup table shall be able to be modified by tele-commands from ground control.
The size of the LUT_SETTINGS is 192 bits; the size of the LUT_BEACON is 50 bits. The whole LUT is consequently 242 bits long.
There is one LUT_setting per SEPT unit (E or NS), and a single LUT_BEAQCON for all SEPT units.

8.2 Accumulation time

The SEP DPU shall know the actual accumulation time. The format used is compliant to the Time Field (T-Field) of the CCSDS Unsegmented Code, defined in AD4. The T-Field consists of two octets of coarse time (seconds) and one octet of fine time (sub seconds). The single fine time octet provides a resolution of 3.90 milliseconds.

CCSDS Unsegmented Code – Time Field	Coarse time		Fine time
Bit weight	2^{15} - 2^{8}	2^{7} - 2^{0}	2^{-1} - 2^{-8}
Bit numbering	0-7	8 - 15	16 –23
Rs232 type correspondence	D7 – D0	D7 – D0	D7 – D0

Table 8 CCSDS Unsegmented Code - Time Field

Note: The counter in the timer is based on a synthesizer to generate an internal binary clock frequency. The obtained synthesized frequency with a 32 bit wide frequency synthesizer is $f_{synth\ obtained}=f_{ck}*244335/2^{32}$. The resulting static drift caused by the ratio between the ideal and obtained synthesized frequency is 225 microseconds per minute.

8.3 Filtered event counters

These counters are recording the filtered event for each detector, they are 24 bits wide, there are 4 of them located in two RAMs. The most significant byte (bits 0 to 7) of a counter is transmitted first over the asynchronous serial interface. In case of the 24 bit counters, the 31st counter is sent first, counter 0 is the most significant and counter 31 is the least significant.

8.4 Single Counter

The Single event counter records all the events associated to one channel during ACC_TIME. It is 24 bits[2] wide which enables to cover 60 seconds at maximum count rate (250 kevents/s). Bits B0 to B7 are the most significant.

[2] In the Engineering Model, the single counter is 23 bits wide only.

8.5 Nominal Mode

8.5.1 Description

This mode will be used most of the time during the mission. It consists of the accumulation of the 4 buffers (per SEPT subsystem) during ACC_TIME and the reading of the buffers, the PDFE working in full anti-coincidence mode. HK values will also be read at the end of each accumulation.

The accumulation duration is based on the internal timer of the FPGA. The binning of the energy is logarithmic and is done internally (32 bins) according to Table 37.
The nominal mode is an “endless” repetition of the 8 series of commands described in Table 9. The 8 series enable to cover the 8 channels (4 PDFE, main and coincidence channels) with the unique single counter (see paragraph 1.1.1).
It is assumed that the “Nominal Configuration sequence” described in section 9.3 has been initially performed.
The following table describes the series of commands and events in the case where no error occurs (else refer to section 11).

Nom1			
step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
1	cStartRun	01100100	
2	Accumulation of events during ACC_TIME. During this period, SEP send the cClearIrq command to get the interrupt register (to check for latchup and configuration error). The polling frequency is discussed in 8.5.2).		
3	`cClearIrq`	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110000	PDFE 0 32 counters
5	Cread32	10110001	PDFE 1 32 counters
6	Cread32	10110010	PDFE 2 32 counters
7	Cread32	10110011	PDFE 3 32 counters
8	cConfPDFE	10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE 0 in ADC mode
9	cGetHK	01000000	HK_CS0 (1 byte), HK_GR0 (1 byte), HK_CS1 (1 byte), HK_GR1 (1 byte)
10	cConfPDFE	10010000+First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE0 back into the charge amplification mode with active coincidence channel (full anticoincidence)
11	cConfPDFE	10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E	Configure PDFE 1 in ADC mode

		Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	
12	cGetHK	01000001	The temperature TA is read (4 times the same values), only one is taken for HK_T
13	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 back into the charge amplification mode with active coincidence channel (full anticoincidence)
14	cConfPDFE	10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configure PDFE 2 in ADC mode
15	cGetHK	01000010	HK_CS2 (1 byte), HK_GR2 (1 byte), HK_CS3 (1 byte), HK_GR3 (1 byte)
16	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configure PDFE2 back into the charge amplification mode with active coincidence channel (full anticoincidence)
17	cConfPDFE	10010011+ First byte: 110xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE 3 in ADC mode
18	cGetHK	01000011	The temperature TB is read (4 times the same values), only one is taken for HK_T
19	cConfPDFE	10010011+ First byte: 100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 back into the charge amplification mode with active coincidence channel (full anticoincidence)
20	cGetSingle	01001100	The response contains the counter value corresponding to the PDFE0 , main channel. At the same time is made the selection of PDFE0 coincidence channel for single counter next record.
21	cClearIrq	01110000	Interrupt register

Nom2
Same as Nom 1 except for step 20 which corresponds to the command 01001001: selection of single counter for PDFE1, main channel and read of single counter corresponding to PDFE0 coincidence channel.
Nom3
Same as Nom 1 except for step 20 which corresponds to the command01001101: selection single counter for PDFE1, coincidence channel and read of single counter corresponding to PDFE1, main channel
Nom 4
Same as Nom 1 except for step 20 which corresponds to the command01001010: selection of the single counter for PDFE2, main channel and read of single counter for PDFE1, coincidence channel
Nom 5
Same as Nom 1 except for step 20 which corresponds to the command01001110: selection of the single counter for the PDFE2, coincidence channel and read of single counter for the PDFE2 main channel
Nom 6
Same as Nom 1 except for step 20 which corresponds to the command 01001011: selection of the single counter for the PDFE3, main channel and read of single counter for PDFE2 coincidence channel
Nom 7
Same as Nom 1 except for step 20 which corresponds to the command 0100111: selection of the single counter for the PDFE3, coincidence channel and read of single counter for PDFE3 main channel.
Nom 8
Same as Nom 1 except for step 20 which corresponds to the command 0100000: selection of the single counter for PDFE0, main channel and read of single counter for PDFE3 coincidence channel

Table 9: Nominal mode command/response series

Step 8, 11, 14 and 17 configure the corresponding PDFE in ADC mode, steps 10, 13, 16 and 19 put them back in observation mode. This means that from one series to the next one, both telescopes are by default completely reconfigured.
TA and TB are acquired but only TA is transmitted in the HK flow and used for operational heater. The benefit of still acquiring both temperature is that the whole nominal sequence of commands stay the same even if one temperature sensor has failed. SEP should be able to choose one of the two values (TA by default) via a command from grounds.
Important: step 3 has to be carried out, i.e it has to be verified that the timer interrupt (bit 2) bit is set to 1.
Rem: The command corresponding to the single counter sends back the data corresponding to the targeted channel specified in the previous single counter command.

Note: the so called « beacon mode » corresponds to a special binning performed by the SEP processor and is based on the data produced in the nominal mode.

8.5.2 Timing

We detail here the timing for one series of steps. The main constraint is to start an accumulation (step 1) every 60 seconds (the start should be synchrone[3] with respect to the other SEPT units and if possible with respect to the other instruments of IMPACT (TBC Impact team). Since the time between two starts is fixed and the dead time should be as short as possible for scientific reasons, steps 3 to 20 should be performed as fast as possible. A rough estimate (considering

[3] A difference of a few milliseconds could be tolerated providing that it is fixed (in case the UART is common to two SEPT units)

the immediate response to a command) shows that the minimum time to carry out the different steps is around 100 ms, **300 ms** would be considered as a satisfying dead time, providing also margin enough to treat potential errors which may have occurred (especially PDFE configuration error, see section 11.4).
To limit the switching noise due to the interface, the polling frequency during the accumulation shall be limited to 0.2 Hz (THIS REMARKS APPLIES TO ALL THE OPERATION MODE). Since ACC_TIME is known by SEP DPU, step 3 could be performed right after ACC_TIME has been elapsed.

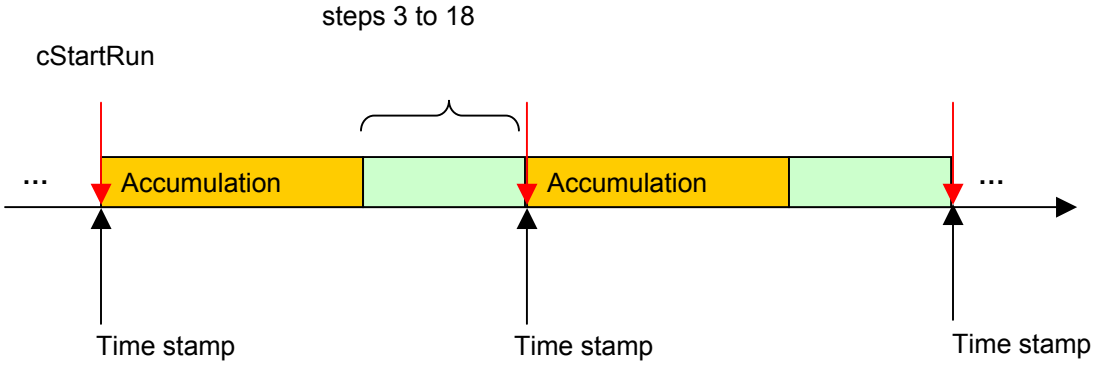

Figure 4 Timing diagram (not to scale)

8.6 Calibration Mode

This mode occurs once a month during one day. The difference with the previous mode resides only in the configuration of the instrument, which will be set to coincidence mode between two center segments of a telescope and in anticoincidence with the corresponding guard rings. Only the penetrating particles will be recorded.
Once the "calibration configuration" sequence has been carried out, Table 10 should be used as the definition of sequence of commands for the calibration mode.
The calibration mode is only valid when the telescopes are both powered on.

Calib 1			
step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
1	cStartRun	01100100	
2	Accumulation of events during ACC_TIME. During this period, SEP send the cClearIrq command to get the interrupt register (to check for latchup and configuration error). The polling frequency is discussed in 8.5.2).		
3	`cClearIrq`	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110000	PDFE 0 32 counters
5	Cread32	10110001	PDFE 1 32 counters
6	Cread32	10110010	PDFE 2 32 counters
7	Cread32	10110011	PDFE 3 32 counters
8	cConfPDFE	10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_	Configure PDFE0 in ADC mode

		PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	
9	cGetHK	01000000	HK_CS0 (1 byte), HK_GR0 (1 byte), HK_CS1 (1 byte), HK_GR1 (1 byte)
10	cConfPDFE	10010000+First byte:101xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE0 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
11	cConfPDFE	10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 in ADC mode
12	cGetHK	01000001	The temperature TA is read (4 times the same values), only one is taken for HK_T
13	cConfPDFE	10010001+First byte:101xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
14	cConfPDFE	10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configure PDFE2 in ADC mode
15	cGetHK	01000010	HK_CS2 (1 byte), HK_GR2 (1 byte), HK_CS3 (1 byte), HK_GR3 (1 byte)
16	cConfPDFE	10010001+First byte:101xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configure PDFE2 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
17	cConfPDFE	10010011+ First byte: 110xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 in ADC mode
18	cGetHK	01000011	The temperature TB is read (4

			times the same values), only one is taken for HK_T
19	cConfPDFE	10010011+ First byte: 101xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
20	cGetSingle	01001100	The response contains the counter value corresponding to the PDFE0 , main channel. At the same time is made the selection of PDFE0 coincidence channel for single counter next record.
21	cClearIrq	01110000	Interrupt register
Calib 2			
Same as Calib 1 except for step 20 which corresponds to the command 01001001: selection of single counter for PDFE1, main channel and read of single counter corresponding to PDFE0 coincidence channel.			
Calib 3			
Same as Calib 1 except for step 20 which corresponds to the command 01001101: selection single counter for PDFE1, coincidence channel and read of single counter corresponding to PDFE1, main channel			
Calib 4			
Same as Calib 1 except for step 20 which corresponds to the command 01001010: selection of the single counter for PDFE2, main channel and read of single counter for PDFE1, coincidence channel			
Calib 5			
Same as Calib 1 except for step 20 which corresponds to the command 01001110: selection of the single counter for the PDFE2, coincidence channel and read of single counter for the PDFE2 main channel			
Calib 6			
Same as Calib 1 except for step 20 which corresponds to the command 01001011: selection of the single counter for the PDFE3, main channel and read of single counter for PDFE2 coincidence channel			
Calib 7			
Same as Calib 1 except for step 20 which corresponds to the command 0100111: selection of the single counter for the PDFE3, coincidence channel and read of single counter for PDFE3 main channel.			
Calib 8			
Same as Calib 1 except for step 20 which corresponds to the command 0100000: selection of the single counter for PDFE0, main channel and read of single counter for PDFE3 coincidence channel			

Table 10 Calibration mode sequence

With respect to the nominal mode only the three first bits of the first byte for steps 10, 13, 16 and 19 are different: 100 in nominal mode, 101 in calibration mode.
The timing described in paragraph 8.5.2 also applies to the calibration mode.

8.7 Test Generator Mode

In this mode the test generator located in the electronics produces charge pulses (frequency 17.543 kHz) that can be routed to the different PDFE inputs (main or guard). Four different

charge amplitudes (equally spread over the full range) can be generated. Each telescope has its own test generator circuitry but both circuitries are operated in parallel. This mode can only be used whenever the two telescopes are operational.
The mode is divided in two parts:

- part Test1: the configuration of the PDFEs and FPGA is similar to the nominal mode (full anti-coincidence)
- part Test2: the configuration of the PDFEs and FPGA is similar to the calibration mode (coincidence with pair center segment and anticoincidence with guard ring and pair guard ring).

For each part the relevant stimuli patterns are tested and a specific channel is selected for the single counter.
The two following tables show the different configurations for both parts.

Series T1	Pattern	Evaluate 32-bin event counters	Evaluate single counter
Test1a	CS Even alone	CS0, CS2 (CS1, CS3)	CS0
Test1b	CS Odd alone	CS1, CS3 (CS0, CS2)	CS1
Test1c	CS Even and CS Odd	CS0, CS1, CS2, CS3	CS2
Test1d	CS Even and GR Even	CS0, CS2 (CS1, CS3)	GR0
Test1e	CS Odd and GR Odd	CS1, CS3 (CS0, CS2)	GR1
Test1f	CS Even and GR Odd	CS0, CS2 (CS1, CS3)	GR3
Test1g	CS Odd and GR Even	CS1, CS3 (CS0, CS2)	GR2

Table 11 Test generator mode: test 1

Series T2	Pattern	Evaluate 32-bin event counters	Evaluate single counter
Test2a	CS Even and CS Odd	CS0, CS1, CS2, CS3	CS3
Test2b	CS Even and CS Odd and GR Even	CS0, CS1, CS2, CS3	GR0
Test2c	CS Even and CS Odd and GR Odd	CS0, CS1, CS2, CS3	GR3

Table 12 Test generator mode: test 2

Each series Test### will be repeated for four different amplitudes. Consequently the duration of the full modes is: 7 * 4 (T1) + 3 *4 (T2)= 40 minutes
An abbreviated test generator mode shall run with only one amplitude (duration 10 minutes).During this mode, temperature and leakage currents will be available at the same rate as for the nominal mode, ie, on a minute basis. The stimulation pattern should be recorded in the status word defined in section 10.
The timing described in paragraph 8.5.2 also applies to the test generator mode.

The test generator mode will be used once every month or less often.
The following sequence of commands details the test1a series (which should be started after the test generator test 1 configuration sequence described in paragraph 9.5). The following series of test 1 can be deduced using the Table 11 and RD1 (bits to change are color highlighted).

Test1a			
step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
1	cStartRun	01100101	
2	Accumulation of events during ACC_TIME. During this period, SEP send the cClearIrq command to get the interrupt register (to check for latchup and configuration error). The polling frequency is discussed in 8.5.2).		
3	`cClearIrq`	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110000	PDFE 0 32 counters
5	Cread32	10110001	PDFE 1 32 counters
6	Cread32	10110010	PDFE 2 32 counters
7	Cread32	10110011	PDFE 3 32 counters
8	cConfPDFE	10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE0 in ADC mode
9	cGetHK	01000000	HK_CS0 (1 byte), HK_GR0 (1 byte), HK_CS1 (1 byte), HK_GR1 (1 byte)
10	cConfPDFE	10010000+First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE0 back in charge amplification mode with active coincidence channel (full anticoincidence)
11	cConfPDFE	10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 in ADC mode
12	cGetHK	01000001	The temperature TA is read (4 times the same values), only one is taken for HK_T
13	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 back in charge amplification mode with active coincidence channel (full anticoincidence)
14	cConfPDFE	10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-	Configure PDFE2 in ADC mode

		SEPT-E	
15	cGetHK	01000010	HK_CS2 (1 byte), HK_GR2 (1 byte), HK_CS3 (1 byte), HK_GR3 (1 byte)
16	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configure PDFE2 back in charge amplification mode with active coincidence channel (full anticoincidence)
17	cConfPDFE	10010011+ First byte: 110xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 in ADC mode
18	cGetHK	01000011	The temperature TB is read (4 times the same values), only one is taken for HK_T
19	cConfPDFE	10010011+ First byte: 100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 back in charge amplification mode with active coincidence channel (full anticoincidence)
20	cGetSingle	01001000	The response contains the counter value corresponding to the PDFE0 , main channel. At the same time is made the selection of PDFE0 main channel for single counter next record.
21	cConfCal	1110000+ 00011000	CS0 and CS2 are stimulated with amplitude 2.
22	cClearIrq	01110000	Interrupt register
Test1a steps are repeated 3 more times: - first time: step 21 is 1110000+ 00101000 (CS0 and CS2 are stimulated with amplitude 3) - second time: step 21 is 1110000+ 00111000 (CS0 and CS2 are stimulated with amplitude 4) - third time: step 20 is 01001001 (reading of the counter value corresponding to the PDFE0 main channel and selection of PDFE1 main channel for single counter next record. Step 21 is 1110000+00000010 (CS1 and CS3 are stimulated with amplitude 1)			

Figure 5 Test1a command sequence

After test1 has been completed the configuration sequence for test2 should been carried out (see paragraph 9.5).
The following sequence of commands details the test2a series . Test2b and test 2c can be deduced using the Table 12 and RD1 (bits to change are color highlighted).

Test2a			
step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
1	cStartRun	01100101	
2	Accumulation of events during ACC_TIME. During this period, SEP send the cClearIrq command to get the interrupt register (to check for latchup and configuration error). The polling frequency is discussed in 8.5.2).		
3	`cClearIrq`	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110000	PDFE 0 32 counters
5	Cread32	10110001	PDFE 1 32 counters
6	Cread32	10110010	PDFE 2 32 counters
7	Cread32	10110011	PDFE 3 32 counters
8	cConfPDFE	10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE0 in ADC mode
9	cGetHK	01000000	HK_CS0 (1 byte), HK_GR0 (1 byte), HK_CS1 (1 byte), HK_GR1 (1 byte)
10	cConfPDFE	10010000+First byte:101xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configure PDFE0 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
11	cConfPDFE	10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 in ADC mode
12	cGetHK	01000001	The temperature TA is read (4 times the same values), only one is taken for HK_T
13	cConfPDFE	10010001+First byte:101xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configure PDFE1 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
14	cConfPDFE	10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-	Configure PDFE2 in ADC mode

		SEPT-E	
15	cGetHK	01000010	HK_CS2 (1 byte), HK_GR2 (1 byte), HK_CS3 (1 byte), HK_GR3 (1 byte)
16	cConfPDFE	10010001+First byte:101xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configure PDFE2 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
17	cConfPDFE	10010011+ First byte: 110xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 in ADC mode
18	cGetHK	01000011	The temperature TB is read (4 times the same values), only one is taken for HK_T
19	cConfPDFE	10010011+ First byte: 101xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configure PDFE3 back in charge amplification mode with active coincidence channel (coincidence with pair detector anti coincidence with guard and pair guard)
20	cGetSingle	01001010	The response contains the counter value corresponding to the PDFE3 , main channel. At the same time is made the selection of PDFE3 main channel for single counter next record.
21	cConfCal	1110000+ 00011010	CS0 and CS2 are stimulated with amplitude 2.
22	cClearIrq	01110000	Interrupt register
Test1a steps are repeated 3 more times: - first time: step 21 is 1110000+ 00011010 (CS0, CS1, CS2 and CS3 are stimulated with amplitude 3) - second time: step 21 is 1110000+ 00111010 (CS0, CS1, CS2 and CS3 are stimulated with amplitude 4) - third time: step 20 is 01001100 (reading of the counter value corresponding to the PDFE3 main channel and selection of PDFE0 coincidence channel for single counter next record. Step 21 is 1110000+00001110 (CS0, CS1, CS2, CS3, GR0 and GR2 are stimulated with amplitude 1)			

Figure 6 Test2a command sequence

8.8 A alone mode

This mode is used when telescope B is non operating (after a latchup or in case of a definitive failure). The following table shows the different series of commands to be used (whatever the previous operational mode was). The 4 series are repeated endless until a command from ground has been sent to operate telescope B again if planned

Aalone 1			
step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
1	cStartRun	01100100	
2	Accumulation of events		
3	cClearIrq	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110000	PDFE 0 32 counters
5	Cread32	10110001	PDFE 1 32 counters
6	cConfPDFE	10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	
7	cGetHK	01000000	HK_CS0 (1 byte), HK_GR0 (1 byte), HK_CS1 (1 byte), HK_GR1 (1 byte)
8	cConfPDFE	10010000+First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	
9	cConfPDFE	10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	
10	cGetHK	01000001	The temperature TA is read (4 times the same values), only one is taken for HK_T
11	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	
12	cGetSingle	01001000	Return single event counter of the PDF0, main channel.
13	cGetSingle	01001100	Selection of PDFE0 coincidence channel for single counter. A counter value is returned but not used
14	cClearIrq	01110000	Interrupt register
Aalone 2			

Same as series 1 except for step 12 and 13. step 12 corresponds to the command 01001100: Return single event counter of the PDF1, coincidence channel, step 13 corresponds to the command 01001001: selection of single counter for PDFE1, main channel
Aalone 3
Same as series 1 except for steps 12 and 13: the step 12 corresponds to the command 01001001: Return single event counter of the PDF1, main channel. The step 13 corresponds to command 01001101: selection single counter for PDFE1, coincidence channel
Aalone4
Same as series 1 except for steps 12 and 13: the step 12 corresponds to the command 01001101: Return single event counter of the PDF1, coincidence channel, the step 13 corresponds to the command 01001000: selection of the single counter for PDFE0, main channel

Table 13 A alone mode series of commands

When this mode is used, all the data relative to telescope B should be filled with 0.

8.9 B alone mode

This mode is used when telescope A is non operating (after a latchup or in case of a definitive failure). The following table shows the different series of commands to be used (whatever the previous operational mode was). The 4 series are repeated endless until a command from ground has been sent to operate telescope B again if planned.

Balone 1			
Step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
1	cStartRun	01100100	
2	Accumulation of events		
3	cClearIrq	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110010	PDFE 2 32 counters
5	Cread32	10110011	PDFE 3 32 counters
6	cConfPDFE	10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	
7	cGetHK	01000010	HK_CS2 (1 byte), HK_GR2 (1 byte), HK_CS3 (1 byte), HK_GR3 (1 byte)
8	cConfPDFE	10010010+First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E	

		Third byte: CL_ PDFE2-SEPT-E	
9	cConfPDFE	10010011+ First byte: 110xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	
10	cGetHK	01000011	The temperature TB is read (4 times the same values), only one is taken for HK_T
11	cConfPDFE	10010011+ First byte: 100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	
12	cGetSingle	01001010	Return single event counter of the PDF2, main channel.
13	cGetSingle	01001110	Selection of PDFE2 coincidence channel for single counter. A counter value is returned but not used
14	cClearIrq	01110000	Interrupt register
Aalone 2			
Same as series 1 except for steps 12 and 13: the step 12 corresponds to the command is 01001110: Return single event counter of the PDF2, coincidence channel. The step 13 corresponds to the command 01001011: selection of the single counter for the PDFE3, main channel.			
Aalone 3			
Same as series 1 except for steps 12 and 13: the step 12 corresponds to the command 01001011: Return single event counter of the PDF3, main channel. The step 18 corresponds to the command: 0100111: selection of the single counter for the PDFE3, coincidence channel.			
Aalone 4			
Same as series 1 except for steps 12 and 13: the step 12 corresponds to the command is 0100111: Return single event counter of the PDF3, coincidence channel. The step 13 corresponds to the command 0100010: selection of the single counter for PDFE0, main channel.			

When this mode is used, all the data relative to telescope A should be filled with 0.

8.10 Commissioning mode

The purpose of this mode is to extensively test the electronics and the detectors after the first switch ON. It should be performed after the opening of the SEPT aperture doors, without and with bias voltage applied on the detector.

The mode is divided in two parts:

- Com1: Without bias voltage:
  - Com1a: command check
  - Com1b: Check FPGA consumption

- Com1c: Check RAM Write and Read
- Com1d: Check mode consumption:
  - Com1da: PDFEs in quiet mode: each telescope individually and both telescopes.
  - Com1db: PDFEs in ADC mode.
  - Com1dc: PDFEs in observation mode[4].
  - Com1dd: Telescopes power-off sequence
- Com1e: Post latchup sequences verification
  - Com1ea: Initialization sequence
  - Com1eb: A alone power on sequence
  - Com1ec: Telescope A reset sequence
  - Com1ed: A alone mode configuration sequence
  - Com1ee: A alone mode (once)
  - Com1ef: Telescope power-off sequence
  - Com1eg: B alone power on sequence
  - Com1eh: Telescope B reset sequence
  - Com1ei: B alone mode configuration sequence
  - Com1ej: B alone mode (once)
  - Com1ek: Telescope power-off sequence

- Com2: With bias voltage applied:
  - Com2a: Initialization sequence
  - Com2b: Telescope power on sequence
  - Com2c: Telescope A reset sequence
  - Com2d: Telescope B reset sequence
  - Com2e: Nominal mode configuration sequence
  - Com2f: Nominal mode for 16 minutes (essentially to monitor leakage currents and single counters values to help for a detector diagnosis)
  - Com2g: Calibration mode configuration sequence
  - Com2h: Calibration mode for 16 minutes (additional information on detector health)
  - Com2i: Test generator mode configuration sequence.
  - Com2j: Test generator mode for 40 minutes to validate the previous tests by checking the different filtering capabilities.

During Com1, the temperature value will be accessible in com1db, com1ee and com1ej. However since this mode will correspond to the first switch-on of this instrument, special care should be taken before the use of these values for thermal control.
During Com2, the house keeping will be accessible on a 1 minute basis, with a timing of the acquisition as defined in section 8.5.2.

If a latchup occurs during the commisionning mode, then the emergency power-off sequence is applied.

The following table details operations Com1a to Com1d.

Com1a		
Command	Expected response	To Do
cRstFPGA 00010001	00010001	Compare response to command

[4] Due to the absence of bias voltage, a non negligible noise will be present at the input of each PDFE's preamplifiers, leading to an increase power consumption.
[5] Com 1ea and Com1eb tests are needed since in case of problem in the nominal, calibration or test generator mode, the instrument should automatically switched to A alone mode or B alone mode.

cRstComm 00010010	00010010	Compare response to command
cGetId 00010100	10011000 for SEPT-E S/C A 10011001 for SEPT-NS S/C A 10011010 for SEPT-E S/C B 10011011 for SEPT-NS S/C B 10011100 for Spare SEPT-E 10011101 for Spare SEPT-NS	Check identification
cClearIrq 01110000	See section 11	
cConfFiltr 00110000	00110000	Compare response to command
cConfFiltr 00110100	00110100	Compare response to command
cConfFiltr 00111000	00111000	Compare response to command
cConfFiltr 00111100	00111100	Compare response to command
cConfFiltr 00110001	00110001	Compare response to command
cConfFiltr 00110101	00110101	Compare response to command
cConfFiltr 00111001	00111001	Compare response to command
cConfFiltr 00111101	00111101	Compare response to command
cConfFiltr 00110010	00110010	Compare response to command
cConfFiltr 00110110	00110110	Compare response to command
cConfFiltr 00111010	00111010	Compare response to command
cConfFiltr 00111110	00111110	Compare response to command
cConfFiltr 00110011	00110011	Compare response to command
cConfFiltr 00110111	0110111	Compare response to command
cConfFiltr 00111011	00111011	Compare response to command
cConfFiltr 00111111	00111111	Compare response to command
cClearIrq 01110000	See section 11	
cSetTimer 11010000 + ACC_TIME	11010000	Compare response to command
cReadTimer 11010100	00000000+00000000+00000000+11010100	Check response
cReadDate 11011000	00000000+00000000+00000000+11011000	Check response
cConfCal 11100000 + 00111111	11100000	Check response
cClearIrq 01110000	See section 11	
cConfLatch 11111111+11111111	11111111	Check response
cClearIrq 01110000	See section 11	

Com1b		
No command sent for 10 seconds, only monitor of LVPS consumption, 1 value per second.		
Com1c		
Command	Expected response	To Do
cRstFPGA 00010001	00010001	Compare response to command
cConfCntr 10100011 + 00000000	10100011	Compare response to command
cInitCntr 10101000	10101000	Compare response to command
cInitCntr 10101001	10101001	Compare response to command
cInitCntr 10101010	10101010	Compare response to command
cInitCntr 10101011	10101011	Compare response to command
cRead32 10110000	Returns the 32 counters of 24 bits set to 0 for PDFE0 + 10110000	Check last byte of the response. The counter value shall be considered as scientific data.
cRead32 10110001	Returns the 32 counters of 24 bits set to 0 for PDFE1 + 10110001	Check last byte of the response. The counter value shall be considered as scientific data.
cRead32 10110010	Returns the 32 counters of 24 bits set to 0 for PDFE2 + 10110010	Check last byte of the response. The counter value shall be considered as scientific data.
cRead32 10110011	Returns the 32 counters of 24 bits set to 0 for PDFE3 + 10110011	Check last byte of the response. The counter value shall be considered as scientific data.
cInitCntr 10101100	10101100	Compare response to command
cInitCntr 10101101	10101101	Compare response to command
cInitCntr 10101110	10101110	Compare response to command
cInitCntr 10101111	10101111	Compare response to command
cRead32 10110000	Returns the 32 counters of 24 bits set to a specific pattern for PDFE0 + 10110000	Check last byte of the response. The counter value shall be considered as scientific data.
cRead32 10110001	Returns the 32 counters of 24 bits set to a specific pattern for PDFE1 + 10110001	Check last byte of the response. The counter value shall be considered as scientific data.
cRead32 10110010	Returns the 32 counters of 24 bits	Check last byte of the

	set to a specific pattern for PDFE2 + 10110010	response. The counter value shall be considered as scientific data.
cRead32 10110011	Returns the 32 counters of 24 bits set to a specific pattern for PDFE3 + 10110011	Check last byte of the response. The counter value shall be considered as scientific data.
Com1da		
Command	Expected response	To Do
cRstFPGA 00010001	00010001	Compare response to command
cConfLatch 11111111+11111111	11111111	Check response. Measure consumption on LVPS
cClearIrq 01110000	See section 11	
cPwrPDFE for PDFE0 and PDFE1 10000010	10000010	Check response. Measure consumption on LVPS
cEnPDFE for PDFE0 and PDFE1 (reset) 10001000	10001000	Check response. Measure consumption on LVPS
cEnPDFE for PDFE0 and PDFE1 (operational) 10001010	10001010	Check response. Measure consumption on LVPS
cDrvPDFE for PDFE0 and PDFE1 10000110	10000110	Check response. Measure consumption on LVPS
cCtrlPDFE for PDFE0 and PDFE1 (analog) 10001110	10001110	Check response. Measure consumption on LVPS
cCtrlPDFE for PDFE0 and PDFE1 (digital) 10001100	10001100	Check response. Measure consumption on LVPS
cConfPDFE 10010000+First byte:111xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	4 bytes + 10010000	Check the last byte
cConfPDFE 10010000+First byte:111xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	00100000 + 111xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E + 10010000	Check response. Measure consumption on LVPS.
cConfPDFE 10010001+First byte:111xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	4 bytes + 10010001	Check the last byte
cConfPDFE 10010001+First byte:111xxxxx (xxxxx= G_	00100000 + 111xxxxx (xxxxx= G_ PDFE1-SEPT-E	Check response. Measure consumption

PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E + 10010001	on LVPS.
cDrvPDFE for PDFE0 and PDFE1 10000100	10000100	Check response. Measure consumption on LVPS
cPwrPDFE for PDFE0 and PDFE1 1000000	10000000	Check response. Measure consumption on LVPS
cClearIrq 01110000	See section 11	
cPwrPDFE for PDFE2 and PDFE3 10000001	10000001	Check response. Measure consumption on LVPS
cEnPDFE for PDFE2 and PDFE3 (reset) 10001000	10001000	Check response. Measure consumption on LVPS
cEnPDFE for PDFE2 and PDFE3 (operational) 10001001	10001001	Check response. Measure consumption on LVPS
cDrvPDFE for PDFE2 and PDFE3 10000101	10000101	Check response. Measure consumption on LVPS
cCtrlPDFE for PDFE2 and PDFE3 (analog) 10001101	10001101	Check response. Measure consumption on LVPS
cCtrlPDFE for PDFE2 and PDFE3 (digital) 10001100	10001100	Check response. Measure consumption on LVPS
cConfPDFE 10010010+First byte:111xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	4 bytes + 10010010	Check the last byte
cConfPDFE 10010010+First byte:111xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	00100000 + 111xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E + 10010010	Check response. Measure consumption on LVPS.
cConfPDFE 10010011+First byte:111xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	4 bytes + 10010011	Check the last byte
cConfPDFE 10010011+First byte:111xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	00100000 + 111xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E + 10010011	Check response. Measure consumption on LVPS.
cDrvPDFE for PDFE2 and PDFE3 10000100	10000100	Check response. Measure consumption

		on LVPS
cPwrPDFE for PDFE2 and PDFE3 10000010	10000000	Check response. Measure consumption on LVPS
cClearIrq 01110000	See section 11	
cPwrPDFE for all PDFEs 10000011	10000011	Check response. Measure consumption on LVPS
cEnPDFE for all PDFEs (reset) 10001000	10001000	Check response. Measure consumption on LVPS
cEnPDFE for all PDFEs (operational) 10001011	10001011	Check response. Measure consumption on LVPS
cDrvPDFE all PDFEs 10000111	10000111	Check response. Measure consumption on LVPS
cCtrlPDFE for all PDFEs (analog) 10001111	10001111	Check response. Measure consumption on LVPS
cCtrlPDFE for all PDFEs (digital) 10001111	10001111	Check response. Measure consumption on LVPS
cConfPDFE 10010000+First byte:111xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	4 bytes + 10010000	Check the last byte
cConfPDFE 10010001+First byte:111xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	4 bytes + 10010001	Check the last byte
cConfPDFE 10010010+First byte:111xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	4 bytes + 10010010	Check the last byte
cConfPDFE 10010011+First byte:111xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	4 bytes + 10010011	Check the last byte. Measure consumption on LVPS
cClearIrq 01110000	See section 11	
Com1db		
Command	Expected response	To Do
cConfPDFE 10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E	4 bytes + 10010000	Check the last byte. Measure consumption on LVPS

Third byte: CL_ PDFE0-SEPT-E		
cConfPDFE 10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	4 bytes + 10010001	Check the last byte. Measure consumption on LVPS
cConfPDFE 10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	4 bytes + 10010010	Check the last byte. Measure consumption on LVPS
cConfPDFE 10010011+First byte:110xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	4 bytes + 10010011	Check the last byte. Measure consumption on LVPS
cGetHK 01000000	4 bytes + 01000000	Since no bias voltage is not applied, the 4 data bytes are unknown values.
cGetHK 01000001	4 bytes + 01000001	The temperature TA is read (4 times the same values), only one is taken for HK_T. Check the last byte
cGetHK 010000010	4 bytes + 01000010	Since no bias voltage is not applied, the 4 data bytes are unknown values
cGetHK 01000011	4 bytes + 01000011	The temperature TB is read (4 times the same values), only one is taken for HK_T. Check the last byte
cClearIrq 01110000	See section 11	
Com1dc		
Command	Expected response	To Do
cConfPDFE 10010000+First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Byte 1: 00000000 Byte 2: 110xxxxx (xxxxx= G_ PDFE0-SEPT-E Byte 3: ML_ PDFE0-SEPT-E Byte 4: CL_ PDFE0-SEPT-E Byte 5: 10010000	Check ALL response bytes. The 5 last bits of byte 1 are parity and voting error of the PDFE.
cConfPDFE 10010001+First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Byte 1: 00000000 Byte 2: 110xxxxx (xxxxx= G_ PDFE1-SEPT-E Byte 2: ML_ PDFE1-SEPT-E Byte 4: CL_ PDFE1-SEPT-E Byte 5: 10010001	Check ALL response bytes. The 5 last bits of byte 1 are parity and voting error of the PDFE.
cConfPDFE 10010010+First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E	Byte 1: 00000000 Byte 2: 110xxxxx (xxxxx= G_ PDFE2-SEPT-E	Check ALL response bytes. The 5 last bits of byte 1 are parity and

Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Byte 2: ML_ PDFE2-SEPT-E Byte 4: CL_ PDFE2-SEPT-E Byte 5: 10010010	voting error of the PDFE.
cConfPDFE 10010011+First byte:100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Byte 1: 00000000 Byte 2: 110xxxxx (xxxxx= G_ PDFE3-SEPT-E Byte 2: ML_ PDFE3-SEPT-E Byte 4: CL_ PDFE3-SEPT-E Byte 5: 10010011	Check the last byte. Measure consumption on LVPS
cClearIrq 01110000	See section 11	
Com1dd		
Telescope power-off sequence. Measure LVPS consumption after completion.		

Table 14 Com1a to Com1d command sequence

During com1e, the LVPS consumption should be measured and logged after the completion of each sequence.

Whenever the response is different from the expected response the corresponding command and response should be logged, as well as when and where it occurred and transmitted via telemetry (TBC).

9 Pre/Post operation Sequences

These sequences are used to configure or power cycle the PDFEs as well as to set up the different operational modes.

9.1 Initialization sequence

After switch-on of the power lines of the SEPT instrument the initialization sequence should be used.

Step	Command	Bit pattern	Arguments	Description
1	cRstComm	00010010		Reset serial communication
2	cRstFPGA	00010001		Reset FPGA
3	cConfLatch	11111111	11111111	Set the timer for the latchup detection (signals on the pin are considered as a real latchup only if asserted longer than 910 us)
4	cClearIrq	01110000		Interrupt register

Table 15: Initialization sequence

9.2 Telescopes power-on sequence

This sequence is used whenever the instrument has been initialized and the two telescopes are to be powered ON.

Step	Command	Bit pattern	Description
1	cPwrPDFE	10000011	Power on PDFEs (telescope A and B are switched ON)

2	cDrvPDFE	10000111	Drive outputs to PDFEs
3	cEnPDFE	10001011	PDFE in acquisition mode
4	cCtrlPDFE	10001100	PDFE in digital mode
4	cClearIrq	01110000	Interrupt register

Table 16: Command sequence to power-up PDFE

9.3 Nominal Configuration Sequence

The following sequence applies to a SEPT-E unit (the sequence for SEPT-NS is easily deducted).

Step	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configuration of PDFE 0
2	cConfFiltr	00110010		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	cConfPDFE	10010001	First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110110		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	cConfPDFE	10010010	First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configuration of PDFE 2
8	cConfFiltr	00111010		Set the filter mode for PDF2 in FPGA
9	cInitCntr	10101010		Initialize counter for PDFE 2
10	cConfPDFE	10010011	First byte:100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
11	cConfFiltr	00111110		Set the filter mode for PDF3 in FPGA
12	cInitCntr	10101011		Initialize counter for PDFE 3
13	cSetTimer	11010000	ACC_TIME	
14	cSingleCounter	01001000		Selection of the single counter for PDFE0, main channel
15	cClearIrq	01110000		Interrupt register

Table 17: Nominal configuration sequence

9.4 Calibration Configuration Sequence

The following sequence applies to a SEPT-E unit (the sequence for SEPT-NS is easily deducted). The difference with the nominal configuration sequence is in the coincidence/anticoincidence configuration (cConfFiltr command).

Step	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:101xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configuration of PDFE 0
2	cConfFiltr	00110011		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	cConfPDFE	10010001	First byte:101xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110111		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	cConfPDFE	10010010	First byte:101xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configuration of PDFE 2
8	cConfFiltr	00111011		Set the filter mode for PDF2 in FPGA
9	cInitCntr	10101010		Initialize counter for PDFE 2
10	CConfPDFE	10010011	First byte:101xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
11	cConfFiltr	00111111		Set the filter mode for PDF3 in FPGA
12	cInitCntr	10101011		Initialize counter for PDFE 3
13	cSetTimer	11010000	ACC_TIME	
14	cSingleCounter	01001000		Selection of the single counter for PDFE0, main channel
15	cClearIrq	01110000		Interrupt register

Table 18: Configuration sequence

9.5 Test Generator Configuration Sequence

The following two tables show the configuration sequence for Test1 and Test2 of the test generator mode. Each sequence is respectively almost identical to the nominal configuration sequence and the calibration sequence with the exception of step 15 which corresponds to the stimulus definition.

Step	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configuration of PDFE 0
2	cConfFiltr	00110010		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	cConfPDFE	10010001	First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110110		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	cConfPDFE	10010010	First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configuration of PDFE 2
8	cConfFiltr	00111010		Set the filter mode for PDF2 in FPGA
9	cInitCntr	10101010		Initialize counter for PDFE 2
10	cConfPDFE	10010011	First byte:100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
11	cConfFiltr	00111110		Set the filter mode for PDF3 in FPGA
12	cInitCntr	10101011		Initialize counter for PDFE 3
13	cSetTimer	11010000	ACC_TIME	
14	cSingleCounter	01001000		Selection of the single counter for PDFE0, main channel
15	cConfCal	11100000	00001000	Configure the calibration pattern to CS0 and CS2, with the amplitude 1.
16	cClearIrq	01110000		Interrupt register

Table 19: Test1 generator mode configuration sequence

Step	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:101xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E	Configuration of PDFE 0

			Third byte: CL_ PDFE0-SEPT-E	
2	cConfFiltr	00110011		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	cConfPDFE	10010001	First byte:101xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110111		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	cConfPDFE	10010010	First byte:101xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configuration of PDFE 2
8	cConfFiltr	00111011		Set the filter mode for PDF2 in FPGA
9	cInitCntr	10101010		Initialize counter for PDFE 2
10	CConfPDFE	10010011	First byte:101xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
11	cConfFiltr	00111111		Set the filter mode for PDF3 in FPGA
12	cInitCntr	10101011		Initialize counter for PDFE 3
13	cSetTimer	11010000	ACC_TIME	
14	cGetSingle	01001010		Selection of the single counter for PDFE3, main channel
15	cConfCal	11100000	00001010	Configure the calibration pattern to CS0, CS1, CS2 and CS3 with the amplitude 1.
15	cClearIrq	01110000		Interrupt register

Table 20: Test 2 configuration sequence

9.6 A alone Power ON sequence

This sequence shall be used only if telescope A and B have been switched-off and A is then supposed to work alone.

Step	Command	Bit pattern	Description
1	cPwrPDFE	10000010	Power on telescope A
2	cDrvPDFE	10000110	Drive outputs to PDFEs of telescope A
3	cEnPDFE	10001010	PDFE of telescope A in

			acquisition mode
4	cCtrlPDFE	10001100	PDFE in digital mode
5	cClearIrq	01110000	Interrupt register

Table 21 A alone power ON sequence

9.7 B alone Power ON sequence

This sequence shall be used only if telescope A and B have been switched-off and B is then supposed to work alone.

Step	Command	Bit pattern	Description
1	cPwrPDFE	10000001	Power on telescope A
2	cDrvPDFE	10000101	Drive outputs to PDFEs of telescope A
3	cEnPDFE	10001001	PDFE of telescope A in acquisition mode
4	cCtrlPDFE	10001100	PDFE in digital mode
5	cClearIrq	01110000	Interrupt register

Table 22 B alone power ON sequence

9.8 A alone configuration sequence

This sequence should be used after the A alone Power ON sequence. It applies to a SEPT-E unit (the sequence for SEPT-NS is easily deducted).

Step	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configuration of PDFE 0
2	cConfFiltr	00110010		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	cConfPDFE	10010001	First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110110		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	cSetTimer	11010000	ACC_TIME	
8	cGetSingle	01001000		Selection of the single counter for PDFE0, main channel
9	cClearIrq	01110000		Interrupt register

Table 23 A alone configuration sequence

9.9 B alone configuration sequence

This sequence should be used after the B alone Power ON sequence. It applies to a SEPT-E unit (the sequence for SEPT-NS is easily deducted).

Step	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010010	First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configuration of PDFE 2
2	cConfFiltr	00111010		Set the filter mode for PDF2 in FPGA
3	cInitCntr	10101010		Initialize counter for PDFE 2
4	cConfPDFE	10010011	First byte:100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
5	cConfFiltr	00111110		Set the filter mode for PDF3 in FPGA
6	cInitCntr	10101011		Initialize counter for PDFE 3
7	cSetTimer	11010000	ACC_TIME	
8	cGetSingle	01001010		Selection of the single counter for PDFE2, main channel
9	cClearIrq	01110000		Interrupt register

9.10 Telescope A reset sequence

Step	Command	Bit pattern	Description
1	cEnPDFE	10001001	reset mode for PDFE 0 and PDFE1
2	cEnPDFE	10001011	Both PDFE operational
3	cClearIrq	01110000	Interrupt register

Table 24 Telescope A reset sequence

This sequence can be used if both telescopes are ON or if only A is ON.

9.11 Telescope B reset sequence

Step	Command	Bit pattern	Description
1	cEnPDFE	10001001	reset mode for PDFE 0 and PDFE1
2	cEnPDFE	10001011	Both PDFE operational
3	cClearIrq	01110000	Interrupt register

Table 25 Telescope B reset sequence

This sequence can be used if both telescopes are ON or if only B is ON.

9.12 Emergency power-off Sequence

No command sent, LVPS power lines switched off immediately. Bias voltages should stay ON since they are common to two SEPT units. The bias voltages should only be powered off if both SEPT units are powered-off. Then the proper time constant should be used to decrease the voltage.

9.13 Telescopes power-off Sequence

The following sequence shall be used prior to switch-off the power lines of the SEPT unit in normal operation.

Step	Command	Bit pattern	Description
1	cEnPDFE	10001000	Low power mode for both telescope
2	cDrvPDFE	10000100	outputs to PDFEs in high impedance
3	cPwrPDFE	10000000	Power off both telescopes PDFEs

Table 26 PDFE power-off sequence

After the power-off sequence the SEPT power lines can be switched off.

10 Status word

A status word will be sent together with the data and HK values. This status word will consist of 10 bytes :

- Field A (bytes 1 and 2): bit to bit OR of the interrupt register obtained via the cClearIrq commands during the 1 minute cycle when in operation. In pre/post operation sequences or com1a to com1d, this field is the interrupt register issued by each cClearIrq.
- Field B (bytes 3 to 5): telescope A: time of the counter saturation, PDFE configuration error or latchup (valid only during accumulation) when occurred (see section 11.1).
- Field C (bytes 6 to 8): telescope B: time of the counter saturation, PDFE configuration error or latchup (valid only during accumulation) when occurred (see section 11.1).
- Field D (byte 9):
    - Single counter address (3 bits):
        - PDFE 0, CS: 000
        - PDFE 0, GR: 001
        - PDFE 1, CS: 010
        - PDFE 1, GR: 011
        - PDFE 2, CS: 100
        - PDFE 2, GR: 101
        - PDFE 3, CS: 110
        - PDFE 3, CS: 111
    - Current operational mode or sequence (5 bits)
        - See identifiers in Table 32 and Table 33
- Field E (byte 10): Calibration configuration
    - Calibration pattern
        - Bit 0: set to 1when CS0/CS2 are stimulated
        - Bit 1: set to 1 when G0/G2 are stimulated
        - Bit 2: set to 1 when CS1/CS3 are stimulated
        - Bit 3: set to 1 when G0/G3 are stimulated
    - Calibration amplitude: 2 bits
    - 2 bits spare.

One status word should be issued:

- **per minute in normal operation**
- **per pre/post operation sequence**

During the commissioning mode the available identifiers should be used accordingly.

11 Interrupt register modifications handling

The following paragraph list the actions to be taken whenever a bit of the interrupt register has been set to 1.

11.1 Time stamp and priority

During an accumulation, it is possible to read the timer value at the occurrence of an interrupt such as latchup, PDFE configuration error or event counter saturation. Irrespectively of the type of event, only the first one will lead to the dating by the FPGA, one per telescope.
Since the SEP DPU doesn't react immediately to an interrupt it is possible that more than one interrupt may be recorded for a unique telescope between two cClearIrq requests. The timer should still be read knowing that it will be difficult to identify which of the interrupt has occurred first. However, the interruption should be treated with the following priorities (decreasing priority):

- digital latchup
- analogue latchup
-
- counter saturation
- timer interrupt
- configuration error

11.2 Timer interrupt (bit 2 of the IR)

The timer will only be used to obtain an accurate accumulation period. Consequently any timer interrupt will signify the correct end of the current accumulation (in any modes). The Fields B and C of the status word shall then be set by default to ACC_TIME, if no other interruption has occurred.

11.3 Counter Saturation (bit 3 or 4 of the IR)

The counters are such that an interrupt is issued whenever a counter reaches its maximum. If such an interruption occurs (it can only be during ACC_TIME), then the cReadDate command shall be immediately sent to the SEPT unit. If no other interruption has occurred before on the same telescope and if a counter saturation has occurred on PDFE 0 or 1 (telescope A) then the bytes 1 to 3 of the response should be used for the field B of the current status word. The bytes 4 to 6 should be placed in field C if the telescope B is concerned.
The current command sequence should then continue according to normal operation.

11.4 PDFE configuration error (bit 8 to 11 of the IR)

The cReadDate command shall be sent to the SEPT unit. If no other interruption has occurred before on the same telescope and if a configuration error has occurred on PDFE 0 or 1 (telescope A) then the bytes 1 to 3 of the response should be used for the field B of the current status word. The bytes 4 to 6 should be placed in field C if the telescope B is concerned.
Three cases have to be distinguished:

- The error has occurred during ACC_TIME, then following the cReadDate and depending on the PDFE pair affected, then normal operation resumes (after each ACC_TIME, the configuration of each PDFE is refreshed).
- The error occurs during the dead time of a measurement cycle: the error is not reported in the current status word. However the configuration error may have lead to erroneous HK values, consequently special care should be taken for the interpretation of the temperature values.

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* In case a configuration error is detected on both telescopes then Telescope A reset sequence AND telescope B reset sequence should be applied consecutively.

- The error occurs in all the other situations: the telescope A reset sequence or Telescope B reset sequence should be carried out immediately and then normal operation resumed

11.5 Latchup (Bit 12 to 15 of IR)

Upon a latchup detection, the affected telescope is powered down automatically by the SEPT FPGA and all signals going to this telescope (from the FPGA) are put in high impedance to avoid damages. The FPGA and SRAM are not sensitive to latchup.

11.5.1 Latchup in telescope A during the accumulation

The cReadDate command shall be sent to the SEPT unit. If no other interruption has occurred before on the same telescope then the bytes 1 to 3 of the response should be used for the field B of the current status word. The current sequence should stop after the counters have been read (e.g. step 7 in nominal mode). Then the B alone configuration sequence should be applied (whatever the previous mode was). At the beginning of the next 1-minute cycle, the instrument should run into the B alone mode until further notification.

Note: this scenario implies that HK will not be available for 1 cycle.

11.5.2 Latchup in telescope B during the accumulation

The cReadDate command shall be sent to the SEPT unit. If no other interruption has occurred before on the same telescope then the bytes 4 to 6 of the response should be used for the field C of the current status word.. The current sequence should stop after the counters have been read (e.g. step 7 in nominal mode). Then the A alone configuration sequence should be applied (whatever the previous mode was). At the beginning of the next 1-minute cycle, the instrument should run into the A alone mode until further notification.

Note: this scenario implies that HK will not be available for 1 cycle.

11.5.3 Latchup during the dead time

The error is not reported in the current status word. A flag should be raised in the SEP DPU so that during the next 1-minute cycle, the error is handled after the first cClearIrq command has been issued during accumulation.

11.5.4 All other cases

11.5.4.1 Telescope Power ON sequence

If a latchup occurs during the telescope power On sequence, the sequence should be stopped and if only one telescope is affected, A alone power ON sequence or B alone power on sequence should be started after a power-off telescope sequence has been performed. The instrument should run into the A or B alone mode until further notification

11.5.4.2 Nominal configuration/ test generator configuration/ calibration configuration sequences

If a latchup occurs during one of the 3 configuration sequences, the sequence should be stopped and if only one telescope is affected, A alone configuration sequence or B alone configuration sequence should be applied. The instrument should run into the A or B alone mode until further notification.

11.5.4.3 Comissionning mode:

If a latchup occurs during the commissioning mode, then the emergency power-off sequence is applied.

11.5.4.4 Other cases

In any other circumstances the Telescopes power-off sequence should be applied.

12 SEP health monitor

Apart from LVPS current and voltage monitor values that will be available directly to the SEP DPU, each SEPT unit provides temperature and detector leakage current measurement.
The emergency switch-off sequence should be used in the followings cases:

- Temperature out of range (limits TBD)
- Over consumption: only the 5.6 Volt analog power supply is limited in the instrument by the sensing switch used for latchup protection. For the 2.6 digital and 5.3 digital, no limiting device is implemented for the FPGA, consequently SEP has to react to any over current on one of these two lines during more than 100 ms (TBC) by switching off the LVPS voltage (some interface tests are needed there). It has to be noted that the FPGA is controlling the antilatchup system. When the latchup occurs, a transient overcurrent (less than 10 ms TBC, SEPT team) might occur before the latchup is stopped (on the 5.3 digital line or the 5.6 Analog line), the SEP should not react to this transient by switching off the LVPS.

13 Instrument operation

In this section, we show how the different sequences and operational modes should be organized as well as the error handling.

13.1 Instrument Power ON

It is assumed that the bias voltage is already applied.

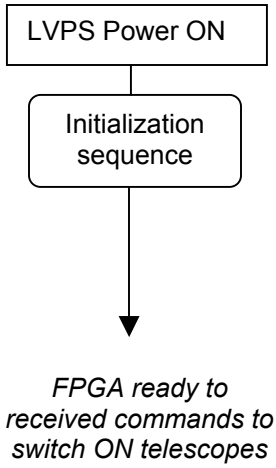


Figure 7 Instrument power-on flow chart

Rem: The first part of the commissioning mode should be carried with bias voltage to zero.

13.2 Normal operation

13.2.1 Nominal mode

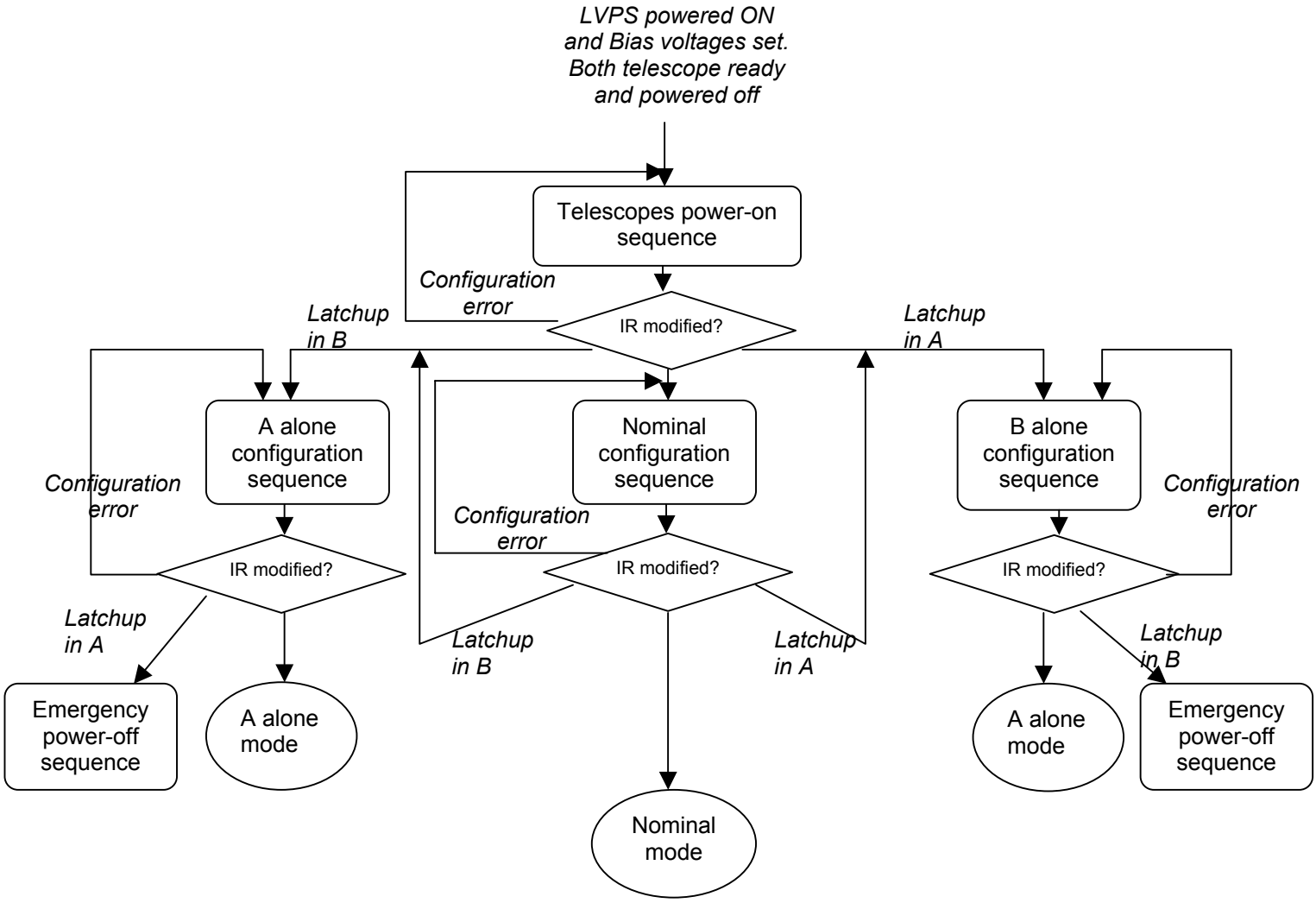


Figure 8 Nominal operation flow chart

13.2.2 Calibration mode

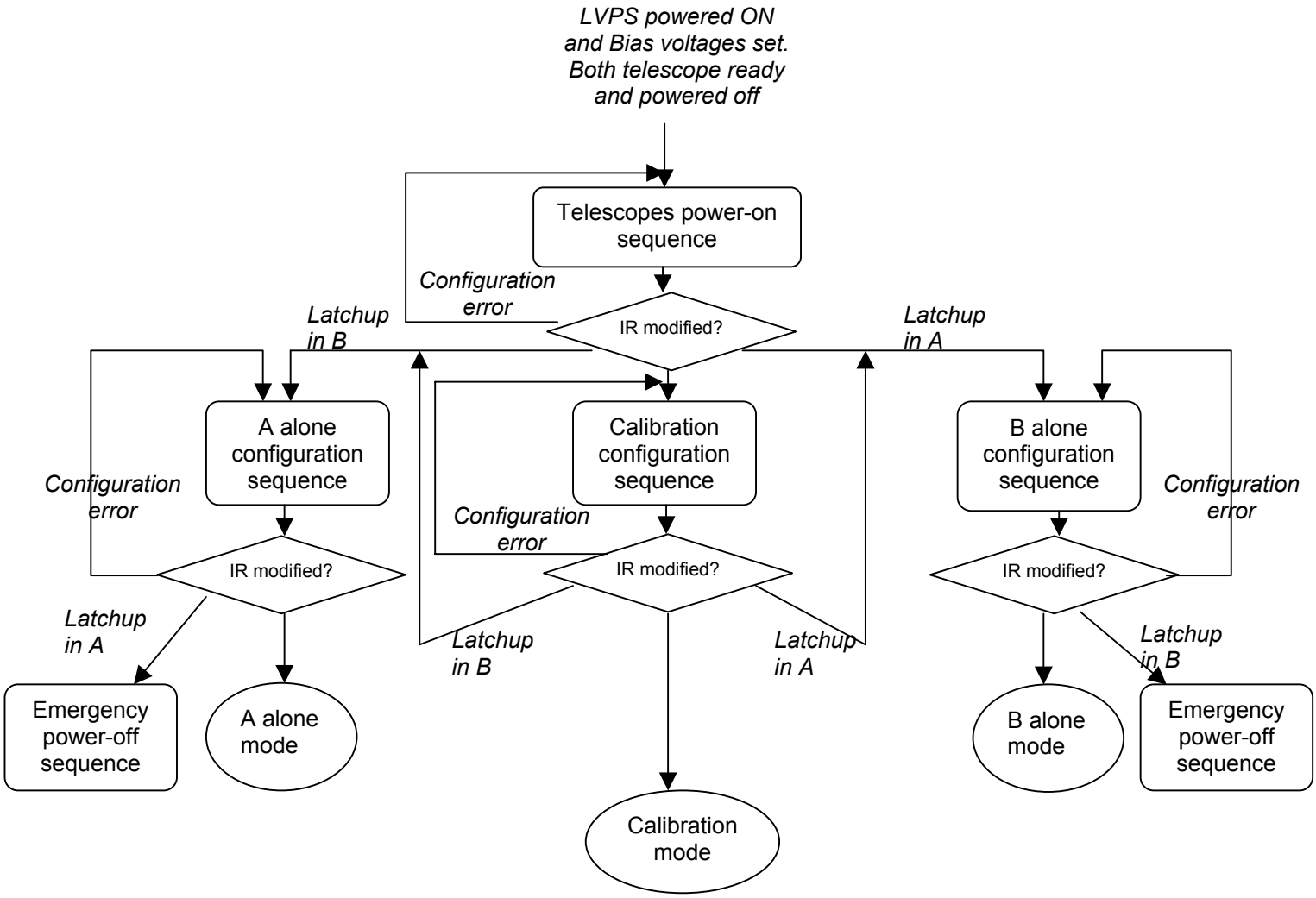
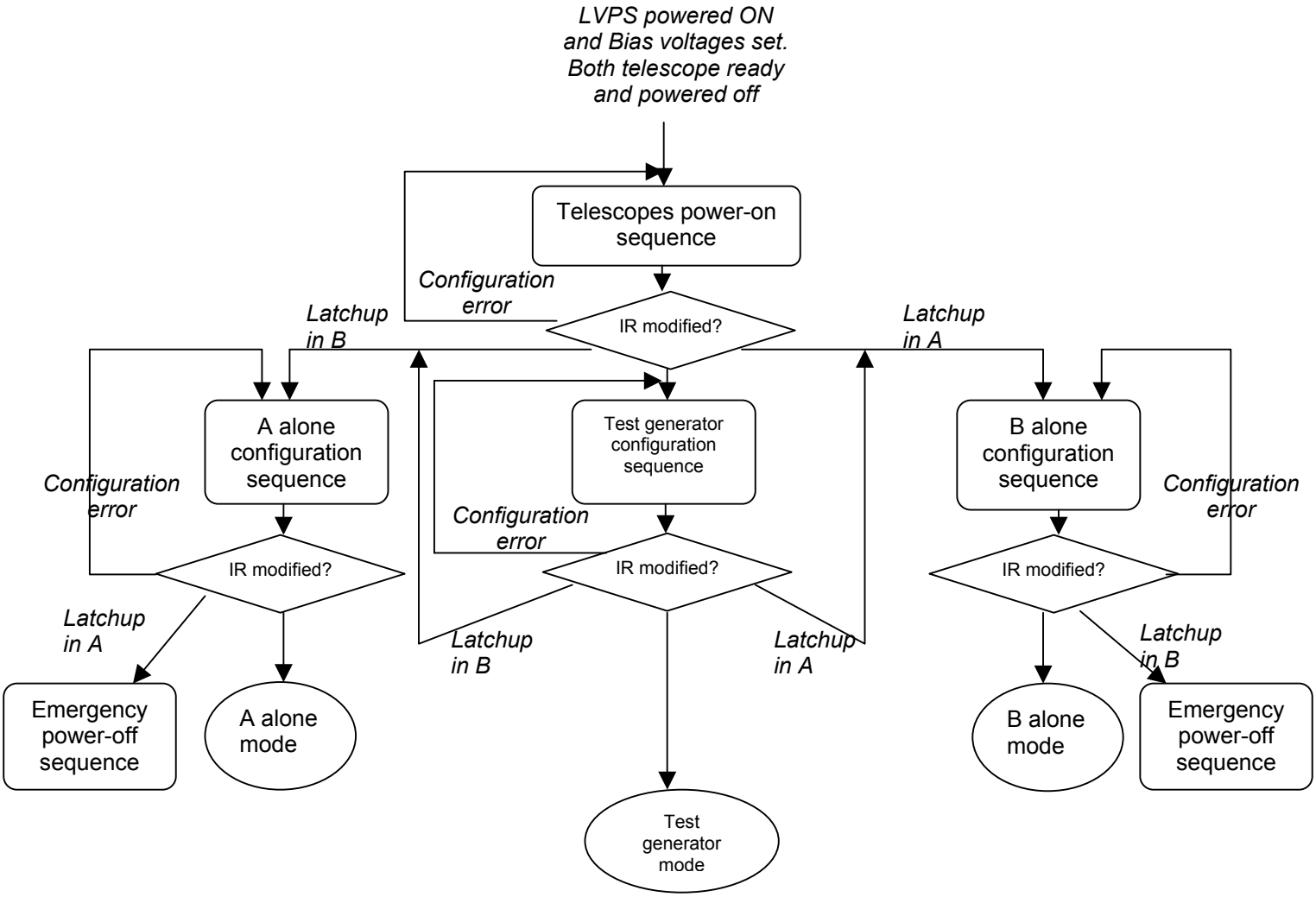


Figure 9 Calibration mode operation flow chart

13.2.3 Test generator mode



13.2.4 Commissioning mode

See section 8.10 for the detailed sequencing. If a latchup occurs during the commissioning mode, the emergency power-off sequence should be applied.

13.3 Communication error

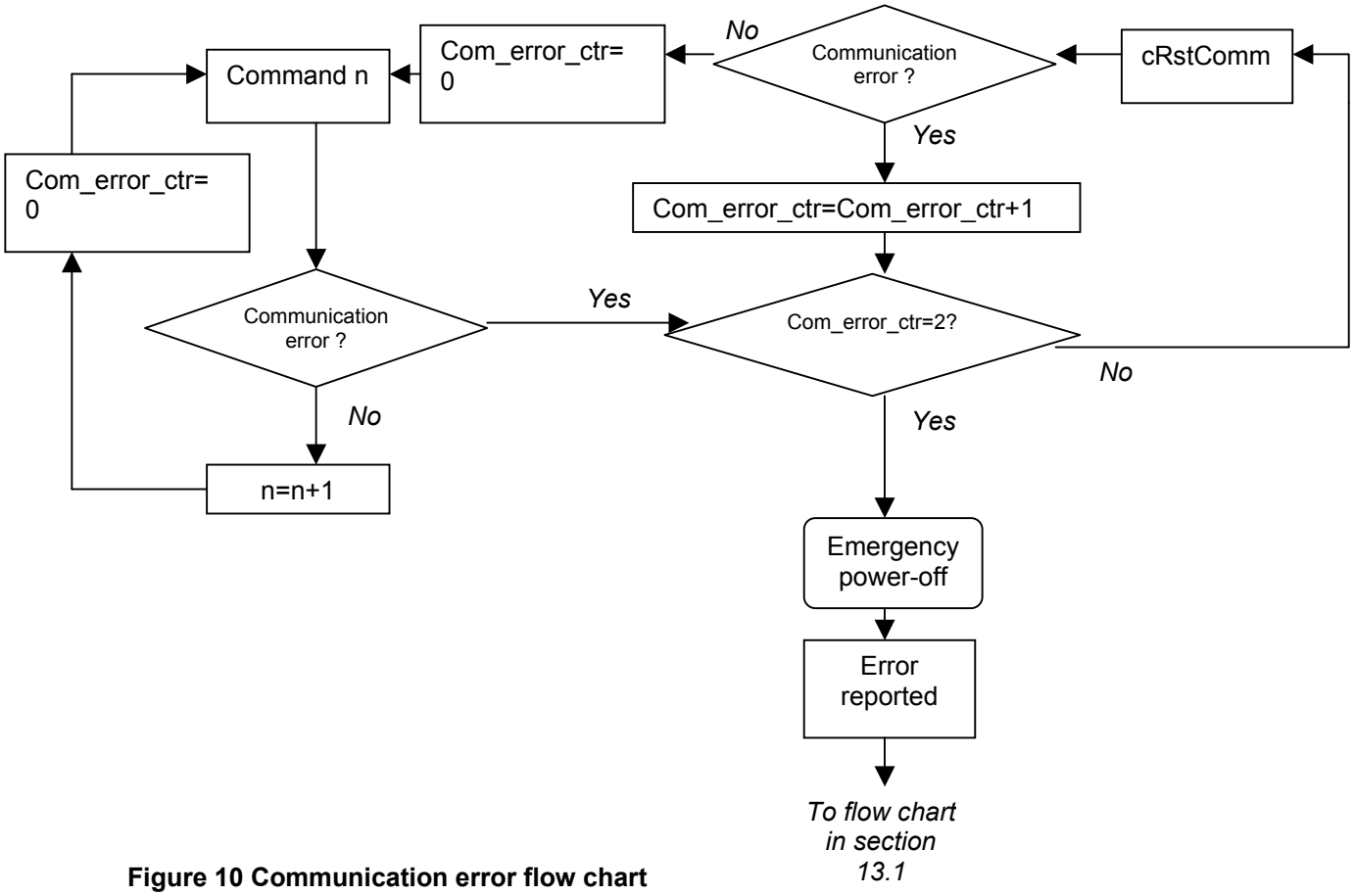


Figure 10 Communication error flow chart

13.4 SEP health monitor

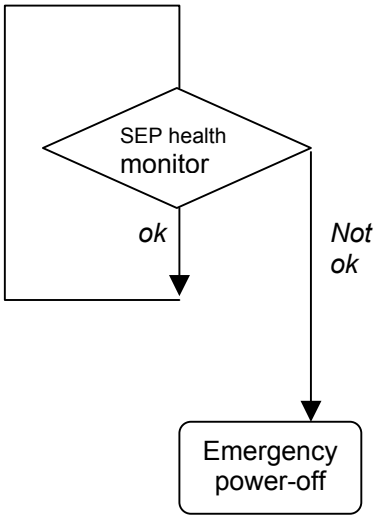


Figure 11 SEP health monitor flow chart

14 Data Processing requirements

14.1 Nominal mode/Calibration mode/Test generator mode

In these three modes, the data received by the SEP processor are in the form of 32 counters of 24 bits per PDFE. Each 24 bits value should be compressed to a 12-bit representation (logarithm representation with mantissa in 8 bits, “Hidden Leading One Notation” and exponent on 4 bits). Besides, HK_T should be extracted from the housekeeping stream and averaged or snapshot[6] for operational heater control[7].

14.2 Beacon mode

The data received by the SEP processor are in the form of 32 counters of 24 bits per PDFE. The different channel (energy/particle type/direction) should be summed up as shown in Table 27. The different values should then be compressed on a 16 bit word (format TBD).

Species	Energy window				Directions
	E1	Index	E2	Index	
Electrons (PDFE 0 and 2)	0.02	1	0.05	4	4 separate
	0.05	5	0.1	7	4 summed
	0.1	8	0.2	12	4 summed
	0.2	13	0.4	17	4 separate
Ions (PDFE 1 and 3)	0.02	1	0.1	7	4 separate
(mostly	0.1	8	0.5	19	4 summed
protons)	0.5	20	1.9	30	4 summed
	1.9	30	31	NA	4 separate

Table 27 Beacon mode channels definition

The indexes refer to the bins . Each channel shall have a 1-bit status to signify invalid data (1 when overflow or non-nominal status).

[6] The 4 values of the temperature are derived from FPGA hardware constraints. Only one can be taken or the average of the four.
[7] The format of HK_T will be specified later.

15 Data rate

The following figures are valid for one set of SEPT-E and SEPT-NS, they are based on a 60 seconds time resolution (ACC_TIME=60s-ε, ε TBD, SEPT team & SEP team) for a normal operation.

15.1 Nominal mode

Data	Total Number of bits
8 x 32 bins, 12 bits per bin	3072
18 Housekeeping values, 8 bits	144
2 single counters, 24 bits each	48
LUT_SETTINGS (one per unit)	384
Status word, 80 bits per unit	160

Table 28 Data rate for the nominal mode

The total is 3808 bits, so 63.4 bit/s.

15.2 Calibration mode

Same as nominal mode.

15.3 Test generator mode

Same as nominal mode.

15.4 Commisionning mode

To be discussed with SEP team.

15.5 Beacon mode

Data	Total Number of bits
20 channels, 16 bit each	320
1 status bit per channel	20

Table 29 Data rate for the beacon mode

The total is 340 bits, so 5.7 bit/s

16 Temperature format

TA and TB are linearly over 8 bits. As an example are shown below the preliminary calibration curves for the Engineering Model.

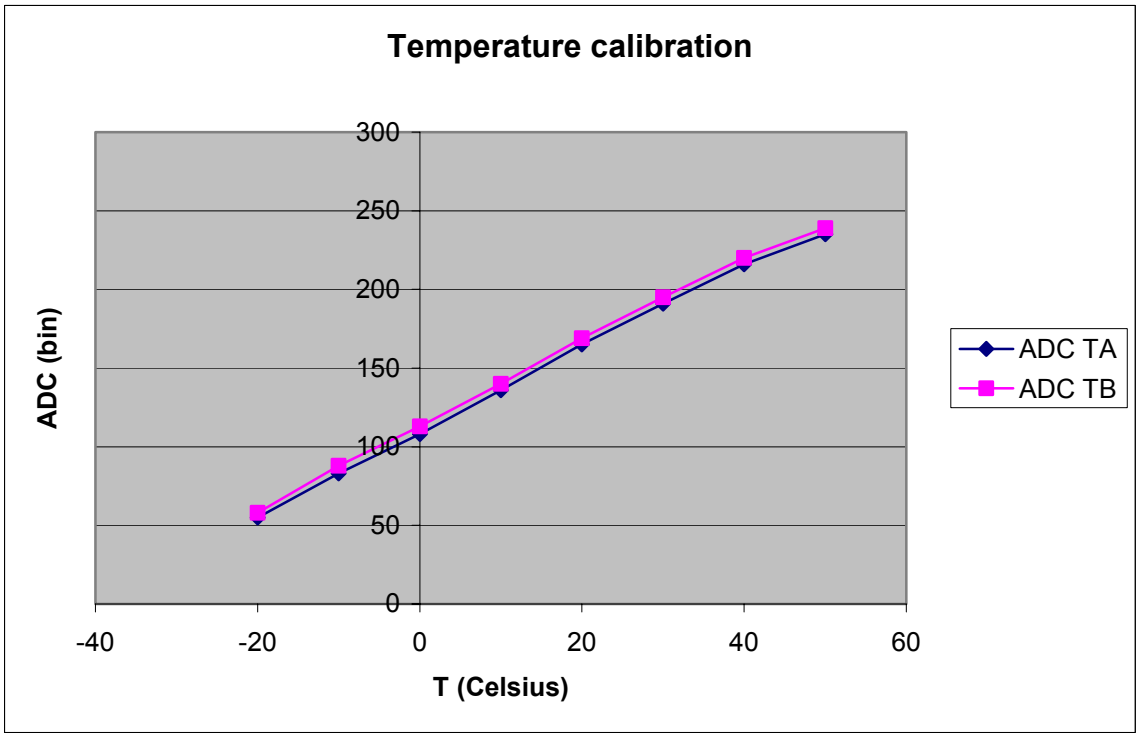


Figure 12 Preliminary temperature calibration curves

or

T	ADC TA	ADC TB
-20	55	58
-10	83	88
0	108	113
10	136	140
20	165	169
30	191	195
40	216	220
50	235	239

Table 31 Preliminary temperature calibration figures

17 Differences between Engineering Model and FM

- cGetSingle: in the engineering model, the issue of the command start a 30 second internal timer during which all the events on a specific channel are recorded, the returned counter is 23 bits.
-

18 List of modes and sequences

18.1 Modes

Mode	Status word identifier
Nominal mode	00000
Calibration mode	00001
Test generator mode	00010
A alone mode	00011
B alone mode	00100
Commissioning mode Com1a to Com1c	00101
Com1da	00110
Com1db	00111
Com1dd	01000

Table 32 List of operational mode identifiers

18.2 Sequences

Sequence	Status word identifier
Initialization sequence	10000
Telescopes power-on sequence	10001
Nominal configuration sequence	10010
Calibration configuration sequence	10011
Test generator configuration sequence	10100
A alone power on sequence	10101
B alone power on sequence	10110
A alone configuration sequence	10111
B alone configuration sequence	11000
Emergency power-off sequence	11001
Telescopes power-off sequence	11010
Telescope A reset sequence	11011
Telescope B reset sequence	11100

Table 33 List of pre/post operation sequence identifiers

19 FPGA details

19.1 Command parameter definition

Symbol	Meaning	Examples
UU	PDFE Index	00 -> PDFE0 01 -> PDFE1 10 -> PDFE2 11 -> PDFE3
PP	Telescope	00 -> No telescope 01 -> Telescope B 10 -> Telescope A 11 -> Telescope A + B
-	Configuration bits	0 -> disable 1 -> enable

Table 34 FPGA commands convention

The following tables list the existing commands, the parameters are represented according to the definition given in previous table

19.2 Commands without arguments

Command	**Bit Pattern**	**Description**
cGetId	00010100	Get part identification
cRstComm	00010010	Reset communication
cRstFPGA	00010001	Reset FPGA
cClearIrq	01110000	Read & Clear Interrupt
cStatPDFE	10010100	Read PDFE status
cReadTimer	11010001	Read Timer value (3 bytes)
cReadDate	11011000	Read dating value
cGetHK	010000UU	ADC Housekeeping (the ADC of each PDFE is used to digitise HK signals)
cConfFiltr	0011UU--	Configure event filters
cGetSingle	01001-UU	Single counter: all detected counts on the addressed PDFE
cRead256	101101UU	Read & clear the counter of the corresponding addressed PDFE with linear binning
cRead32	101100UU	Read & clear the counter of the corresponding addressed PDFE with

		32 log binning
cStartRun	01100---	Start measurements
cPwrPDFE	100000PP	Power PDFE
cGetSingle	01001-UU	Returns the value of the single counter used for measuring all events on the detector
cCtrlPDFE	100011PP	Control PDFEs
cEnPDFE	100010PP	Enable PDFEs
cDrvPDFE	100001PP	Drive outputs of PDFE
cInitCntr	10101-UU	Initialise 256 bin counters
cStopRun	01101000	Stop measurements

Table 35 FPGA commands without arguments

19.3 Commands with arguments

Command	Bit Pattern	Argument(s)	Description
cConfPDFE	100100UU	3 configuration bytes	Configuration of the PDFEs
cConfCntr	101000--	1 byte	Set mode & page
cConfCal	11100000	1 byte	Configuration for the test generator mode
cSetTimer	11010000	3 bytes	Set timer value
cConfLatch	1111----	1 byte	Set the prescale division rate and threshold for latchup detection counter.

Table 36 FPGA commands with arguments

19.4 FPGA 32 bin table

The following table shows the exponential bin boundaries used in the FPGA and the corresponding energy values for a maximum energy of 2.2 MeV. The 32 counters of 24 bits are related to this energy binning. The counter 0 gathers all the counts with energy between 0 and 17.25 keV, counter 1 gathers all the counts with energy between 17.25 and 25.88 and so on….

Index	Energy (keV)
-1	0
0	17.2549
1	25.88235
2	34.5098
3	43.13726

4	51.76471
5	60.39216
6	77.64706
7	94.90196
8	112.1569
9	129.4118
10	155.2941
11	181.1765
12	207.0588
13	241.5686
14	276.0784
15	310.5882
16	353.7255
17	405.4902
18	457.2549
19	517.6471
20	586.6667
21	664.3137
22	741.9608
23	836.8627
24	949.0196
25	1069.804
26	1199.216
27	1354.51
28	1518.431
29	1708.235
30	1915.294
31	>2200

Table 37 Exponential binning table

19.5 FPGA full datasheet

Gaisler Research

Solar Electron and Proton Telescope (SEPT)

FPGA Data Sheet
First Flight Release Document (Version 100_b)
Prepared by Sandi Habinc

SEPT-001-04
Version Draft C
April 2003

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1 INTRODUCTION

This document defines the functionality of the *Solar Electron and Proton Telescope (SEPT)* FPGA device to be used in the *Solar Electron and Proton Telescope (SEPT)* instrument. SEPT is part of the *Solar Energetic Particles Package (SEP)* in the *In-situ Measurements of Particles And CME Transients (IMPACT)* payload on the spacecraft pair on the NASA *Solar-Terrestrial Relations Observatory (STEREO)* mission.

1.1 Applicable documents

AD1 Particle Detector Front-End (PDFE) Data Sheet, PDFE-DS-IMEC-JW-3, 28 November 2000, IMEC
AD2 CCSDS 301.0-B-2: Recommendation: Time Code Formats, Blue Book, Issue 2, April 1990, *http://www.ccsds.org*
AD3 RS-232 EIA/TIA Standard
AD4 RS-422 EIA/TIA Standard

1.2 Reference documents

RD1 In-situ Measurements of Particles And CME Transients (IMPACT), University of California, Berkeley, USA, *http://sprg.ssl.berkeley.edu/impact*
RD2 Power-Up and Power-Down Behaviour of 54SX, Application Note, 5192674-0/1.01, January 2001, Actel Corporation, *http://www.actel.com*
RD3 Prototyping for the RT54SX-S Enhanced, 5192672-0/1.01, January 2001, Actel Corporation, *http://www.actel.com*
RD4 Using Schmitt Triggers for Low Slew-Rate Input, Application Note, 5192697-0/5.02, May 2002, Actel Corporation, *http://www.actel.com*
RD5 Actel eX, SX-A and RTSX-S I/Os, Application Note, 5192699-1/7.02, July 2002, Actel Corporation, *http://www.actel.com*
RD6 Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications, Application Note, 5192687-0/12.01, December 2001, Actel Corporation, *http://www.actel.com*
RD7 SX to SX-A Design Migration, Application Note, 5192658-2/4.02, April 2002, Actel Corporation, *http://www.actel.com*
RD8 Package Characteristics and Mechanical Drawings, 5193068-1/2.01, v3.0, February 2001, Actel Corporation, *http://www.actel.com*
RD9 EIA Standard Board Layout of Soldered Pad for QFP Devices (PQ/RQ208/CQ208), Actel Corporation, *http://www.actel.com*
RD10 Design Migration from the RT54SX32 to the RT54SX32S Device, Technical Brief, 5192679-0/8.01, August 2001, Actel Corporation, *http://www.actel.com*
RD11 Testing and Burn-In of Actel FPGAs, Application Note, 5192662-0/4.00, April 2000, Actel Corporation, *http://www.actel.com*
RD12 IEEE Standard 1149.1 (JTAG) in the SX/RTSX/SX-A/eX/RT54SX-S Families, Application Note, October 2002, Actel Corporation, *http://www.actel.com*

1.3 Reference data sheets

RD13 RT54SX-S RadTolerant FPGAs for Space Applications - Data Sheet, Advanced, 5172151-6/11.02, version 1.4, November 2002, Actel Corporation, *http://www.actel.com*

RD14 CMOS Low Voltage 4 Omega, 4-Channel Multiplexer, ADG704, C3383a-0.6/99, Revision A, 1999, Analog Devices, Inc., *http://www.analog.com*

RD15 CMOS Low Voltage 4 V Quad SPST Switches, ADG711/ADG712/ADG713, C3385-8-10/ 98, Revision 0, 1998, Analog Devices, Inc., *http://www.analog.com*

RD16 SX-A Family FPGAs - Data Sheet, 5172147-5/6.01, version 3.0, June 2001, Actel Corporation, *http://www.actel.com*

RD17 32k x 8 Static RAM, HC6856, 900049, February 1996, Honeywell, *http://www.ssec.honeywell.com*

RD18 RT54SX-S Tr/Tf Experiment, June 2002, Actel Corporation, *http://www.actel.com*

RD19 RT54SX Tr/Tf Experiment, July 2002, Actel Corporation, *http://www.actel.com*

RD20 eX, SX-A and RT54SX-S Power Estimator, Actel Corporation, *http://www.actel.com*

RD21 54SX Family FPGAs Errata, Errata v2.0, 5172137E-3/3.02, March 2002, Actel Corporation, *http://www.actel.com*

1.4 Acronyms and abbreviations

ADC	Analogue to Digital Converter
ASIC	Application Specific Integrated Circuit
CCSDS	Consultative Committee for Space Data Systems
CME	Coronal Mass Ejection
CMOS	Complementary Metal-Oxide Semiconductor
CQFP	Ceramic Quad Flat Package
CUC	CCSDS Unsegmented Code
DPU	Data Processing Unit
ESA	European Space Agency
FPGA	Field Programmable Gate Array
I/F	Interface
IMPACT	In-situ Measurements of Particles And CME Transients
JTAG	Joint Test Action Group
NASA	National Aeronautics and Space Administration
N/C	Not Connected
PC	Personal Computer
PDFE	Particle Detector Front-End
PQ	Plastic Quad Flat Package
SEL	Single Event Latchup
SEP	Solar Energetic Particles Package
SEPT	Solar Electron Proton Telescope
SEU	Single Event Upset
SRAM	Static Random Access Memory
STEREO	Solar-TErrestrial RElations Observatory
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits

2 FUNCTIONAL DESCRIPTION

2.1 Summary of operation

The SEPT (Solar Electron Proton Telescope) FPGA device implements the centralised control, data processing and interfacing functions in the Solar Electron and Proton Telescope (SEPT) instrument. Two SEPT instruments are foreseen per STEREO spacecraft. The SEPT FPGA device interfaces the instrument controller of the Solar Energetic Particles Package (SEP) (also referred to as the user in this document) with two solar electron and proton telescopes through four Particle Detector Front-End (PDFE) ASICs (two PDFEs per telescope). It provides nominal services such as particle event data collection, filtering and binning; and auxiliary services such as operational settings, voltage adjustments, calibration, housekeeping and monitoring. All communication with the user is done through an asynchronous bit serial command interface.

The SEPT FPGA device can operate in several modes, depending on the configurable settings of the device itself as well as the configuration of the individual PDFE devices it interfaces with. The PDFE devices can be configured individually through a synchronous bit serial interface. The configuration is done by user commands and is transparent to the SEPT FPGA device which only provides the necessary communication infrastructure. In addition to the serial configuration of the PDFE devices some discrete configuration pins on each PDFE can be controlled through the SEPT FPGA device. The user can also observe the error status of each PDFE via the asynchronous bit serial command interface.

Each PDFE has two analogue silicon detector interfaces; one main channel (called detector) on which particle charges are detected and converted to digital values; and a secondary channel (called guard or coincidence detector) on which particle charges are only detected and used for anti/coincidence detection w.r.t. the main channel. The anti/coincidence detection can lead to the cancellation of the main channel event, depending on the configuration of the device. Each PDFE has a digital event interface connected to the SEPT FPGA device, through which particle detections are communicated. Two signal groups on this interface need to be noted especially. Each channel (main and secondary) has an event detection output that is connected to the SEPT FPGA device and to which no filtering is applied by the PDFE. The main channel has also a parallel data interface with a valid signal which is asserted depending on the anti/coincidence filtering (or cancellation) in the PDFE. The filtering in the PDFE is either done by directly comparing the timing of the event detection of the main channel with that of the secondary channel (called internal anti/coincidence); or by comparing the former with an external digital input (called external anti/coincidence). The valid signal on the parallel data interface is thus only asserted after successful filtering in the PDFE. Filtering can be effectively disabled by selecting external filtering and keeping the external digital input de-asserted.

The event detection signals for the main and secondary channel on two PDFEs belonging to the same telescope are used in the SEPT FPGA device to provide additional filtering options to those implemented in the PDFE. The result from the filtering in the SEPT FPGA device is fed back to the external digital anti/coincidence input of each PDFE, letting the PDFE perform the final filtering and masking of the data valid signal.

The SEPT FPGA device provides different programmable filtering combinations for generating the external digital anti/coincidence input of each PDFE. Global event filtering is provided for

the telescopes based on either direct user control or through causes internal to the SEPT FPGA device such as expiration of a timer or saturation of the event counters. This carters different types of measurement sessions.

After a particle event has been detected, passing the above filtering in the PDFE, it will be counted as an event in one specific counter. Since each event can have a data value of 8 bits, there are 256 possible values that can be taken into account. The SEPT FPGA device provides therefore 256 counters per PDFE, allowing the user to have one counter for each digital value. Each counter is 24 bit wide. To reduce the amount of data, the values can be compressed in different bins using a boundary scheme. The SEPT FPGA device provides 32 bins with 33 boundary values, two being implicit, which will compress the data. The usage of 32 or 256 counters is selectable per telescope.

The counters are implemented in an external volatile memory, one memory device for each telescope that is shared between the two corresponding PDFEs. The counters can be read and reset via user commands, reading 32 or 256 counter values in one go via the asynchronous bit serial command interface. Each counter will not wrap around, instead it will stop counting when reaching its highest possible value. When the counter saturates, as just described, an internal interrupt is generated and can be used for controlling the measurement session. For each telescope, there are four sets or pages of counters, allowing for up to four consecutive measurement sessions without the need for reading out the counter values. One counter page can be read and/or cleared while another is being used and written to during a session. The page selection is configurable per telescope. It takes nine system clock periods for a read-modify-write operation to each counter. To allow for redundancy and low operating frequency, the SEPT FPGA device comprises separate memory interfaces for each telescope.

For housekeeping purposes, the main or secondary channel event detection outputs can be used for direct counting of events on detector or guard. For the detector, no charge information is stored as for nominal measurement, only the occurrence of an event is counted. The PDFE discriminators can be used for setting threshold levels for the events.

The SEPT FPGA device comprises a timer function to allow the SEPT instrument to operate under precise timing constrains posed by the measurement session. The timer acts simultaneously as an alarm facility, stopping the measurement and generating an internal interrupt when a desired time period has elapsed; and as a datation facility, latching the elapsed time on an interrupt such as the saturation of a counter mentioned above, an external error condition or on the detection of a electrical latchup of a telescope. The alarm facility is used simultaneously for both telescopes. The datation facility is duplicated and is used per telescope. The timer function can be set and read via user commands.

In addition to the PDFE devices, the SEPT instrument hosts two analogue multiplexers which are used for multiplexing analogue observation points towards dedicated analogue inputs on the PDFE devices. By configuring the corresponding PDFE and commanding the SEPT FPGA device, the output of the analogue multiplexer can be read through the PDFE, which performs the analogue to digital conversion, and be reported to the user through the asynchronous bit serial command interface.

The SEPT instrument hosts analogue devices for calibration purposes, to which the SEPT FPGA device provides the necessary communication infrastructure.

To avoid damaging any components surrounding the SEPT FPGA device, it will disable its output signals when a latchup status pin is asserted. This is done by putting outputs that are interfacing sensitive devices, such as the PDFE devices, in a high impedance state. In this way it is possible to implement latchup detection and protection circuitry that can cut the power supply to a PDFE without risking that it will be damaged through the interfacing signals of the SEPT FPGA device. (Re-)Enabling of the interface signals is done by user commands via the asynchronous bit serial command interface.

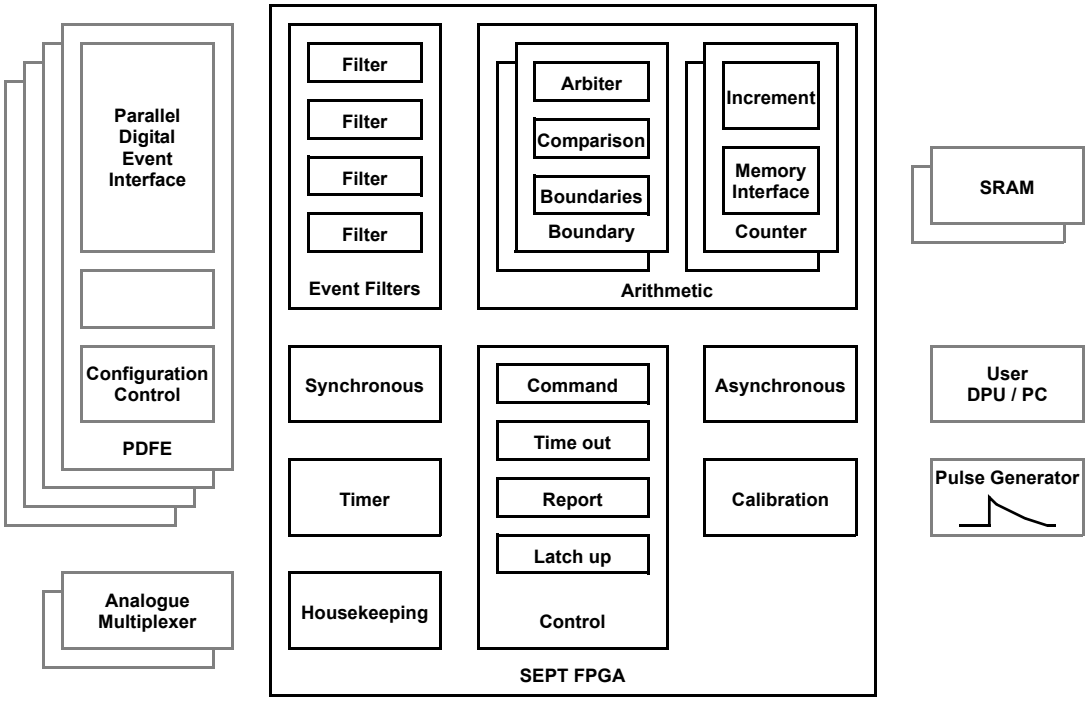

Figure 1: *Simplified block diagram of SEPT FPGA device*

2.2 Functions not included

The SEPT FPGA device does not perform automatic configuration of the individual PDFE devices. It only provides the infrastructure for configuring the PDFEs by user commands via the asynchronous bit serial commanding interface. It cannot read a counter value stored in the external memory without clearing it. It cannot preset the timer, it can only reset it and preset the alarm time.

2.3 Description of the foreseen system using the device

The SEPT FPGA device is foreseen to be used in the SEPT instrument onboard the STEREO spacecraft. It will interface four PDFEs, two SRAMs, two analogue multiplexers, a calibration pulse generator, power regulators, latchup detection and an asynchronous bit serial interface. For the sake of simplicity, the block diagram in figure 2 shows a configuration with only one telescope, although the instrument includes two.

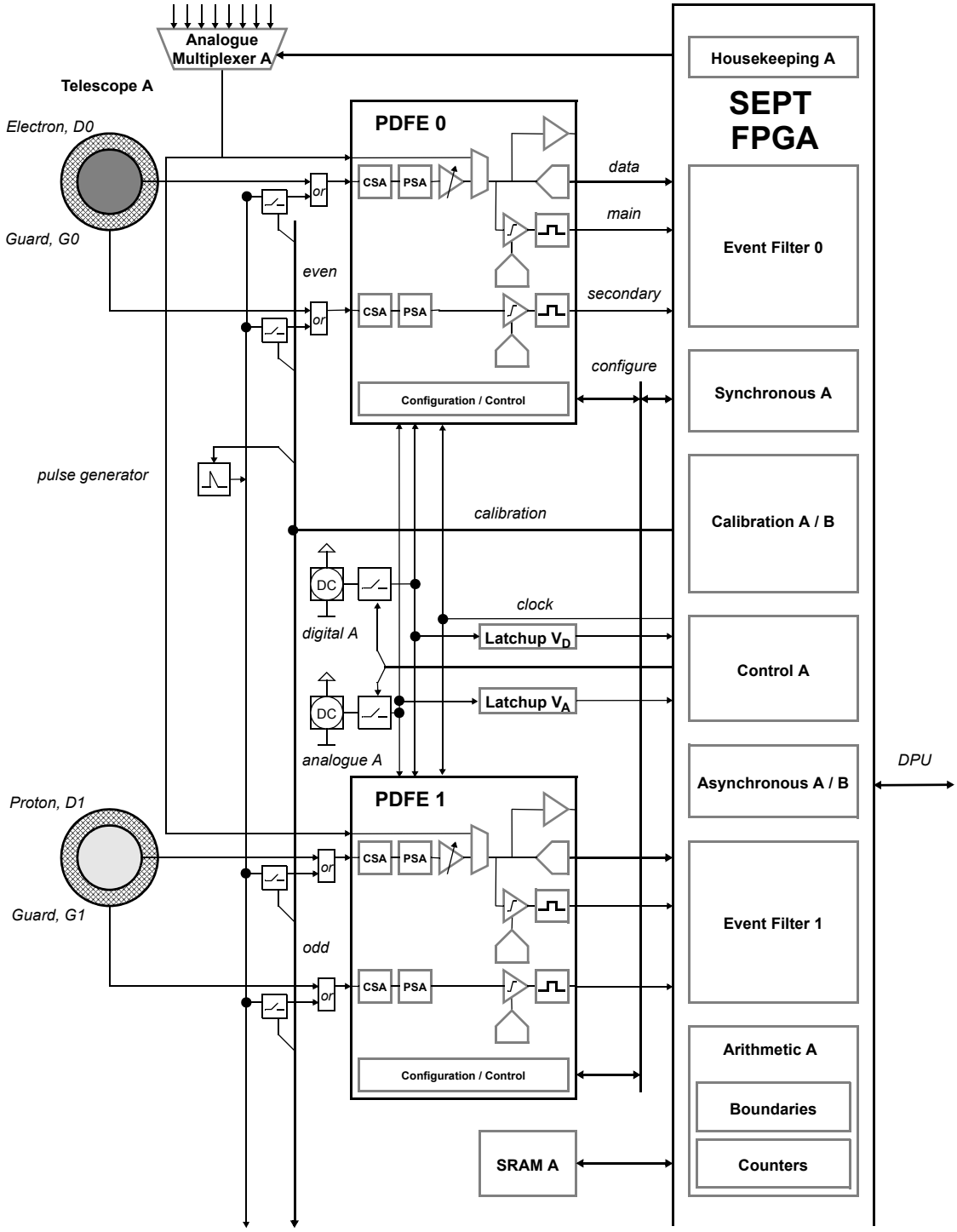

Figure 2: *Block diagram of the SEPT instrument with the SEPT FPGA device*

2.4 Numbering and naming conventions

In general, bit indexed number 0 is the most significant in all data and address formats, placed to the left in bit arrays and is transferred first in a serial bit stream if not mentioned otherwise. The exception is the asynchronous bit serial interface defined in table 1.

Signals with the suffix "*_N*" are active low, i.e. asserted at logical 0.

The SEPT instruments hosts two telescopes which are named A and B. Each telescope interfaces two PDFEs, numbered 0 and 1 for telescope A, and 2 and 3 for telescope B. Interface signals common to a telescope have the letters A or B attached to their names. Signals belonging to a single PDFE have the numbers 0 to 3 attached to their names.

2.5 Data formats

2.5.1 Asynchronous bit serial data format

The asynchronous bit serial interface complies to the data format defined in AD3. It also complies to the data format and waveform shown in table 1 and figure 3. The interface is independent of the transmitted data contents. Positive logic is considered for the data bits. The conversion between the bit order for the asynchronous bit serial interface and the general bit order used in other tables in this document is provided in table 1.

Asynchronous RS-232 type format	start	D0	D1	D2	D3	D4	D5	D6	D7	stop	stop
	first	*lsb*							*msb*		*last*
General data format ***i* = {0, *n-1*}**		8**i*+7	8**i*+6	8**i*+5	8**i*+4	8**i*+3	8**i*+2	8**i*+1	8**i*		
		last							*first*		

Table 1: *Asynchronous bit serial data format (RS-232 type)*

2.5.2 CCSDS Unsegmented Code data format

The timer is compliant to the Time Field (T-Field) of the CCSDS Unsegmented Code (CUC), defined in AD2. The T-Field consists of two octets of *coarse* time (seconds) and one octet of *fine* time (sub seconds). The coarse time code elements are a count of the number of seconds elapsed from an epoch. Two octets of coarse time results in a maximum ambiguity period of approximately 18 hours. The single fine time octet provides a resolution of 3,90 milliseconds.

CCSDS Unsegmented Code - Time Field	**Coarse time**		**Fine Time**
Bit weight:	2^{15} - 2^{8}	2^{7} - 2^{0}	2^{-1} - 2^{-8}
Bit numbering:	0 - 7	8 - 15	16 - 23
RS-232 type correspondence	D7 - D0	D7 - D0	D7 - D0

Table 2: *CCSDS Unsegmented Code T-Field definition*

2.5.3 PDFE serial interface protocol data format

The serial interface protocol of the PDFE complies to the data format defined in AD1. It also complies to the data format and waveform shown in table 3, table 4 and figure 4. The interface is dependent on the transmitted data contents. The PDFE input AOutSel is described further in table 7 (*cCtrlPDFE*), section 3.5.1 and section 3.5.2.

Index		Description	Comment	RS-232 type correspondence
Octet 0:		Status	read only octet	
	bit 0	0, fixed	transmitted/received first	D7
	bit 1	Analogue output	digital output when 0	D6
	bit 2	Latching parallel output	non-latching when 0	D5
	bit 3	Parity error in octet 1 to 3	no error when 0	D4
	bit 4	Voting error in bit 2	no error when 0	D3
	bit 5	Voting error in bit 8	no error when 0	D2
	bit 6	Voting error in bit 9	no error when 0	D1
	bit 7	Voting error in bit 10	no error when 0	D0
Octet 1:		Control	read and write octet	
	bit 8-10	Operating mode	See table 4, default = 000	D7-D5
	bit 11-15	Conversion gain level	Sign-magnitude format, default = 00000	D4-D0
Octet 2:		Control	read and write octet	
	bit 16-23	Main detection level	Default is mid-rage = 10000000	D7-D0
Octet 3:		Control	read and write octet	
	bit 24-31	Coincidence detection level	Default is mid-rage = 10000000	D7-D0

Table 3: *PDFE serial interface protocol*

AOutSel	Bit 8-10	Mode	Correlation	Output	Comment	
0	000	Coincidence detection	anti-coincidence	digital	coincidence channel active	internal coincidence
	001	Coincidence detection	coincidence			
	010	Charge amplification	anti-coincidence		coincidence channel inactive	external coincidence
	011	Charge amplification	coincidence			
	100	Charge amplification	anti-coincidence		coincidence channel active	
	101	Charge amplification	coincidence			
	110	Analogue to digital	-		used for housekeeping	
	111	Quiet mode	-	-	low power mode	
1	00X	Charge amplification	-	analogue	coincidence channel active	
	01X	Charge amplification	-		coincidence channel inactive	
	1XX	Buffer-only mode	-		analogue buffering only	

Table 4: *PDFE operating modes*

2.5.4 Exponential bin boundaries table

Bin boundaries											
Index	**Value**	**Index**	**Value**	**Index**	**Value**	**Index**	**Value**	**Index**	**Value**	**Index**	**Value**
-1	*0*	5	7	11	21	17	47	23	97	29	198
0	2	6	9	12	24	18	53	24	110	30	222
1	3	7	11	13	28	19	60	25	124	*31*	*255*
2	4	8	13	14	32	20	68	26	139		
3	5	9	15	15	36	21	77	27	157		
4	6	10	18	16	41	22	86	28	176		

Table 5: *Exponential bin boundaries table (indexes -1 and 31 implicit)*

2.5.5 Counter memory mapping

PDFE	Page	Counter number	Byte	Address, hexa-decimal	Counter bits	Weight	RS-232 type correspondence	Comment
0 / 2	0	0	0	0000h	0 - 7	msb		unused
			1	0001h	8 - 15		D7 - D0	
			2	0002h	16 - 23		D7 - D0	
			3	0003h	24 - 31	lsb	D7 - D0	
		1	0	0004h	0 - 7	msb		unused
			1	0005h	8 - 15		D7 - D0	
			2	0006h	16 - 23		D7 - D0	
			3	0007h	24 - 31	lsb	D7 - D0	
0 / 2	1	0	0	0400h	0 - 7	msb		unused
			1	0401h	8 - 15		D7 - D0	
			2	0402h	16 - 23		D7 - D0	
			3	0403h	24 - 31	lsb	D7 - D0	
0 / 2	3	0	0	0C00h	0 - 7	msb		unused
			1	0C01h	8 - 15		D7 - D0	
			2	0C02h	16 - 23		D7 - D0	
			3	0C03h	24 - 31	lsb	D7 - D0	
		255	0	0FFCh	0 - 7	msb		unused
			1	0FFDh	8 - 15		D7 - D0	
			2	0FFEh	16 - 23		D7 - D0	
			3	0FFFh	24 - 31	lsb	D7 - D0	
1 / 3	0	0	0	1000h	0 - 7	msb		unused
			1	1001h	8 - 15		D7 - D0	
			2	1002h	16 - 23		D7 - D0	
			3	1003h	24 - 31	lsb	D7 - D0	
1 / 3	3	0	0	1C00h	0 - 7	msb		unused
			1	1C01h	8 - 15		D7 - D0	
			2	1C02h	16 - 23		D7 - D0	
			3	1C03h	24 - 31	lsb	D7 - D0	
		255	0	1FFCh	0 - 7	msb		unused
			1	1FFDh	8 - 15		D7 - D0	
			2	1FFEh	16 - 23		D7 - D0	
			3	1FFFh	24 - 31	lsb	D7 - D0	

Table 6: *Memory mapping of counters (as per PDFE pair) (incomplete)*

2.5.6 Command set data format

Note: The bit numbering in table 7 is according the general numbering convention and not according to asynchronous bit serial protocol. For bit order conversion, see table 1.

Mnemonic	**Operation**	**Description**	**Parameters**			**Comment**
	01234567		**Bit**		**Function**	
cRstFPGA	00010001	Reset FPGA	no parameters			no arguments
		Response:	Bit 0-7:		00010001	
		Description:	Resets all internal registers of the FPGA, aborting any activities and powering down all PDFEs. Note that the memories are not effected. This specified response is also transmitted after power up on completion of internal reset.			
cRstComm	00010010	Reset communication	no parameters			no arguments
		Response:	Bit 0-7:		received command	
		Description:	Resets the communication interface, stopping all asynchronous or synchronous transmission, clearing all communication with memory, housekeeping etc.			
cGetId	00010100	Get part identification	no parameters			no arguments
		Response:	Bit 0-2:		Version number:	
				000	First Prototype Model	
				001	Second Prototype Model	
				010	Third Prototype Model	
				011	Fourth Prototype Model	
				100	**Fifth Prototype Model**	
				other	Reserved	
			Bit 3-4:		Model type:	
				00	Breadboard Model	
				01	Engineering Model	
				10	Qualification Model	
				11	**Flight Model**	
			Bit 5-7:		Identifier number:	
				5:	taken from input pints	***Id0***
				6:		***Id1***
				7:		***Id2***
			Bit 8-15:		received command	
		Description:	Returns identification values.			

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

Mnemonic	Operation	Description	Parameters			Comment
	01234567		Bit		Function	
cConfFiltr	0011UU--	Configure filters	Bit 4-5:		PDFE addressing	no arguments
			Bit 6-7:		Filter mode:	
				00	Disabled: no event is propagated	
				01	Independent: no correlation with pair detector or guard	
				10	Observation: anti-coincidence with guard and pair detector and guard	
				11	Calibration: coincidence with pair detector, anti-coincidence with guard and pair guard	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 6-7:		00	
		Description:	The individual PDFE (anti-)coincidence filtering should be set to match the SEPT FPGA filtering: mode 01: unconstrained filtering selection, mode 10: anti-coincidence filtering, mode 11: coincidence filtering.			
cGetHK	010000UU	ADC housekeeping	Bit 6-7:		ADC Addressing	no arguments
		Response:	Bit 0-7:		ADC Mux # 3 value:	bits 0 to 7
			...			
			Bit 24-31:		ADC Mux # 0 value:	bits 0 to 7
			Bit 32-39:		received command	
		Description:	Cycles through all eight possible inputs to the addressed analogue multiplexer which are converted to digital values by the PDFE.			
cGetSingle	01001-UU	Single counter	Bit 5:		Detector:	no arguments
				0	main	
				1	guard	
			Bit 6-7:		PDFE addressing	
		Response:	Bit 0-7:		Detector single counter	bits 0 to 7
			Bit 8-15:			bits 8 to 15
			Bit 16-23:			bits 16 to 23
			Bit 24-31:		received command	
		Default value:	Bit 5-7:		000	
		Description:	Returns the value of the single counter used for measuring all events on a detector. If a measurement is not ongoing, selection of PDFE and detector occurs. If a measurement is ongoing, the momentary value of the counter is still returned, but the PDFE and detector selection is cancelled not to disturb the ongoing measurement.			

Table 7: *SEPT command set with parameters, arguments and responses {0/1 = logical values, U = numeric value, - = parameter, X = don't care}*

Mnemonic	Operation	Description	Parameters		Comment
	01234567		Bit	Function	
cStartRun	01100---	Start measurement	Bit 5:	Timer alarm:	no arguments
			0	disabled	
			1	enabled	
			Bit 6:	Counter saturation:	
			0	disabled	
			1	enabled	
			Bit 7:	Calibration:	
			0	disabled	
			1	enabled	
		Response:	Bit 0-7:	received command	
		Default value:	Bit 5-7:	000	
		Description:	Configures the measurement mode and starts the measurement. The timer, datation and single counter values are cleared before timer is started. Event propagation is enabled. Interrupt register is cleared. An immediate response is generated. A measurement is completed either by a command, an alarm when enabled, a timer saturation when enabled, PDFE configuration error or latchup when not masked. All the above events will complete the measurement per affected telescope, except for the time alarm which will complete the measurement on both telescopes. On the completion of the measurement, event propagation will be disabled on affected telescopes. The single counter measurement will only be completed by a command or a timer saturation.		
cStopRun	01101000	Stop measurement	no parameters		no arguments
		Response:	Bit 0-7:	received command	
		Description:	Stops timer and triggers datation on both telescopes (will only occur if no datation has yet taken place). Disables event propagation. Stops the calibration if ongoing. Stops the single counter if ongoing.		

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

Mnemonic	Operation	Description	Parameters		Comment
	01234567		Bit	Function	
cClearIrq	01110000	Read & clear interrupt	no parameters		no arguments
		Response:	Bit 0:	Event propagation enabled on 0 and 1	
			Bit 1:	Event propagation enabled on 2 and 3	
			Bit 2:	Time alarm interrupt, latched	
			Bit 3:	Saturation interrupt on 0 and 1, latched	
			Bit 4:	Saturation interrupt on 2 and 3, latched	
			Bit 5:	Unused, returns logical zero	
			Bit 6:	PDFE 0 or 1 error or latchup during measurement	
			Bit 7:	PDFE 2 or 3 error or latchup during measurement	
			Bit 8:	PDFE 0 configuration error, latched	
			Bit 9:	PDFE 1 configuration error, latched	
			Bit 10:	PDFE 2 configuration error, latched	
			Bit 11:	PDFE 3 configuration error, latched	
			Bit 12:	PDFE 0 or 1 analogue latchup, latched	
			Bit 13:	PDFE 0 or 1 digital latchup, latched	
			Bit 14:	PDFE 2 or 3 analogue latchup, latched	
			Bit 15:	PDFE 2 or 3 digital latchup, latched	
			Bit 16-23:	received command	
		Description:	Reports the contents of the interrupt register where the interrupt source is latched and stored till read out. Clears interrupt register and interrupt signal. Timer alarm and counter saturation occurrences will always be report in the interrupt register, but will not be propagated to the external interrupt when masked. Configuration error occurrences or latchup detection will neither be reported nor propagated when masked. Measurement related configuration and latchup occurrences will be cleared on the start of a measurement. A latchup will only terminate the measurement on the related telescope. Reporting of event propagation enabling will never propagate to an external interrupt and is directly readable through the interrupt registers. Only one BREAK response is sent per interrupt cause until the interrupt registers is cleared. Interrupt source detection is edge sensitive.		

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

Mnemonic	Operation	Description	Parameters			Comment
	01234567		Bit		Function	
cPwrPDFE	100000--	Power PDFE	Bit 6:		PDFE 0 and 1:	no arguments
				0	power off	
				1	power on	
			Bit 7:		PDFE 2 and 3:	
				0	power off	
				1	power on	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 6-7:		00	
		Description:	Controls power to PDFE pairs. If a pair is powered down, the error and latchup inputs are masked, outputs are not driven and resets are asserted. Controls also the PDFE clock.			
cDrvPDFE	100001--	Drive outputs to PDFE	Bit 6:		PDFE 0 and 1:	no arguments
				0	high impedance output	
				1	drive outputs	
			Bit 7:		PDFE 2 and 3:	
				0	high impedance output	
				1	drive outputs	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 6-7:		00	
		Description:	Enables the drive of SEPT FPGA outputs to PDFE pairs when corresponding pair is powered. If outputs are not driven, the error and latchup inputs are masked and resets are asserted. Controls also the PDFE clock.			
cCtrlPDFE	100011--	Control PDFEs	Bit 6:		PDFE 0 and 1 output:	no arguments
				0	digital	
				1	analogue	
			Bit 7:		PDFE 2 and 3 output:	
				0	digital	
				1	analogue	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 6-7:		00	
		Description:	Selecting analogue or digital PDFE output.			
cEnPDFE	100010--	Enable PDFEs	Bit 6:		PDFE 0 and 1:	no arguments
				0	reset, low-power mode	
				1	operational	
			Bit 7:		PDFE 2 and 3:	
				0	reset, low-power mode	
				1	operational	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 6-7:		00	
		Description:	PDFE reset and low-power mode. When a pair is enabled, the error and latchup inputs are unmasked. When disabled, errors are masked, but not latchup.			

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

Mnemonic	Operation	Description	Parameters		Comment
	01234567		Bit	Function	
cConfPDFE	100100UU	Configure PDFE	Bit 6-7:	PDFE addressing	
		Arguments:	Bit 8-15:	PDFE serial control interface, see AD1 section 5:	bits 8 to 15
			Bit 16-23:		bits 16 to 23
			Bit 24-31:		bits 24 to 31
		Response:	Bit 0-7:	PDFE response according to serial status interface, see AD1 section 5:	bits 0 to 7
			Bit 8-15:		bits 8 to 15
			Bit 16-23:		bits 16 to 23
			Bit 24-31:		bits 24 to 31
			Bit 32-39:	received command	
		Default value:	Refer to AD1 for default start-up values.		
		Description:	Individual programming of each PDFE via the serial control interface. The first byte of the PDFE control message is not used by the device and the actually transmitted value to the PDFE is the command byte received by SEPT. The subsequent arguments are transmitted unaltered to the PDFE. The four bytes received by the SEPT from the PDFE are transmitted unaltered as a response. The addressed PDFE needs to be powered, the corresponding SEPT FPGA outputs must be driven and the PDFE must be enabled for the programming to take an effect.		
cStatPDFE	10010100	Read PDFE status	no parameters		no arguments
		Response:	Bit 0:	PDFE 0 internal configuration error	
			Bit 1:	PDFE 1 internal configuration error	
			Bit 2:	PDFE 2 internal configuration error	
			Bit 3:	PDFE 3 internal configuration error	
			Bit 4:	PDFE 0 or 1 analogue latchup	
			Bit 5:	PDFE 0 or 1 digital latchup	
			Bit 6:	PDFE 2 or 3 analogue latchup	
			Bit 7:	PDFE 2 or 3 digital latchup	
			Bit 8-15:	received command	
		Description:	Returns immediate value of unmasked PDFE error status and latchup detection inputs.		

Table 7: *SEPT command set with parameters, arguments and responses {0/1 = logical values, U = numeric value, - = parameter, X = don't care}*

Mnemonic	Operation	Description	Parameters			Comment
	01234567		Bit		Function	
cConfCntr	101000--	Set mode & page	Bit 6:		PDFE 0 and 1:	
				0	256 bins	
				1	32 bins	
			Bit 7:		PDFE 2 and 3:	
				0	256 bins	
				1	32 bins	
		Argument:	Bit 8-9:		Active page PDFE 0 and 1	
			Bit 10-11:		Read page PDFE 0 and 1	
			Bit 12-13:		Active page PDFE 2 and 3	
			Bit 14-15:		Read page PDFE 2 and 3	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 6-7:		00	
		Description:	Selects number of counters, active page for measurement and page for read out.			
cInitCntr	10101-UU	Initialise 256 counters	Bit 5:		Initialisation value:	no arguments
				0	all zero (nominal)	
				1	PDFE number; page; counter address	
			Bit 6-7:		PDFE addressing	
		Response:	Bit 0-7:		received command	
		Default value:	Bit 5-7:		000	
		Description:	Initialises 256 read counters.			
cRead32	101100UU	Read & clear counters	Bit 6-7:		PDFE addressing	no arguments
		Response:	Bit 0-7:		Counter # 31:	bits 8 to 15
			Bit 8-15:			bits 16 to 23
			Bit 16-23:			bits 24 to 31
			...			
			744-751		Counter # 0:	bits 8 to 15
			752-759			bits 16 to 23
			760-767			bits 24 to 31
			768-785		received command	
		Description:	Read and clear 32 read counters.			
cRead256	101101UU	Read & clear counters	Bit 6-7:		PDFE addressing	no arguments
		Response:	Bit 0-7:		Counter # 255:	bits 8 to 15
			Bit 8-15:			bits 16 to 23
			Bit 16-23:			bits 24 to 31
			...			
			6120-6127		Counter # 0:	bits 8 to 15
			6128-6135			bits 16 to 23
			6136-6143			bits 24 to 31
			6144-6151		received command	
		Description:	Read and clear 256 read counters.			

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

Mnemonic	Operation	Description	Parameters		Comment
	01234567		Bit	Function	
cSetTimer	11010000	Set alarm time	no parameters		
		Arguments:	Bit 8-15:	Alarm Coarse Time:	bits 0 to 7
			Bit 16-23:		bits 8 to 15
			Bit 24-31:	Fine Time:	bits 16 to 23
		Response:	Bit 0-7:	received command	
		Description:	Presets the alarm time and clears the timer and datation values. The timer tasks are not enabled until a start measurement command is received (see *cStartRun*).		
cReadTimer	11010100	Read timer value	no parameters		no arguments
		Response:	Bit 0-7:	Timer Coarse Time:	bits 0 to 7
			Bit 8-15:		bits 8 to 15
			Bit 16-23:	Fine Time:	bits 16 to 23
			Bit 24-31:	received command	
		Description:	The current timer value is read. Note that an inaccurate value could be reported since the read out rate of the timer is governed by the baud rate of the asynchronous bit serial command interface. This is only the case if measurement is ongoing at the moment of the read out.		
cReadDate	11011000	Read datation value	no parameters		no arguments
		Response:	Bit 0-7:	Datation A Coarse Time:	bits 0 to 7
			Bit 8-15:		bits 8 to 15
			Bit 16-23:	Fine Time:	bits 16 to 23
			Bit 24-31:	Datation B Coarse Time:	bits 0 to 7
			Bit 32-39:		bits 8 to 15
			Bit 40-47:	Fine Time:	bits 16 to 23
			Bit 48-55:	received command	
		Description:	The current datation values are read. Note that an inaccurate value could be reported since the read out rate of the timer is governed by the baud rate of the asynchronous bit serial command interface. This is only the case when a datation occurs at the moment of the read out during a measurement.		
rUnKnown	N/A	Unknown command			
		Response:	Bit 0-7:	00000011	
		Description:	Response pattern when an unknown command is received. Can be used for echoing.		
rTimeOut	N/A	Time-out response			
		Response:	Bit 0-7:	00001111	
		Description:	Response pattern when a time-out has occurred while waiting for an argument. It is recommended to reset the SEPT FPGA device after the occurrence of a time-out to assure correct operation.		

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

Mnemonic	Operation	Description	Parameters		Comment
	01234567		Bit	Function	
cConfCal	11100000	Calibration setting	no parameters		
		Arguments:	Bit 8-9:	Unused	
			Bit 10:	A1, most significant	Addressing of pulse generator
			Bit 11:	A0, least significant	
			Bit 12:	Cal_M_Even	
			0	disabled	
			1	enabled	
			Bit 13:	Cal_G_Even	
			0	disabled	
			1	enabled	
			Bit 14:	Cal_M_Odd	
			0	disabled	
			1	enabled	
			Bit 15:	Cal_G_Odd	
			0	disabled	
			1	enabled	
		Response:	Bit 0-7:	received command	
		Default value:	Bit 2-7:	0000000	
		Description:	Calibration will only commence on the reception of a start measurement command (see *cStartRun*) upon which the event interface will be enabled. A command response will be issued at the end of the programming. The pulse target enabling and pulse generation is automatically disabled on the detection of a latchup and the measurement stops on the affected telescope		
cConfLatch	1111----	Set latchup threshold	Bit 4-7:	Prescaler, 1/16 to 1/256 division of fCK	
		Argument:	Bit 8-15:	Threshold, 0 to 255 prescaler cycles	
		Response:	Bit 0-7:	received command	
		Default value:	Bit 4-15:	0000 00000000	
		Description:	Sets the prescaler division rate and the threshold value for latchup detection counters. The latchup detect input has to be continuously asserted for at least the threshold period to be taken into account. Note that a zero value for the threshold results in no guaranteed minimum time. The setting is 00000000b for 0 and 11111111b for 255. Note that the programmed prescaler value must be seen as a jitter for the detection. The setting is 0000b for 1/16 to 1111b for 1/256. Each latchup detector input has its own counter that is clocked by the prescaler and compared with the threshold.		

Table 7: *SEPT command set with parameters, arguments and responses*
{0/1 = logical values, U = numeric value, - = parameter, X = don't care}

2.6 Waveform formats

The SEPT FPGA device accepts and generates the waveform formats shown in figure 3, figure 4 and figure 5. Note that the bit order listed in the figure is related to the asynchronous bit serial interface only, and differs to what is used else were in the document. A conversion table between the different bit orderings is provided in table 1.

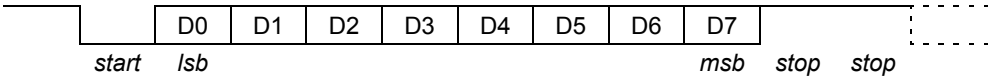

Figure 3: *Asynchronous bit serial waveform (non-inverted), the inverted waveform is observed on the pins of SEPT FPGA device*

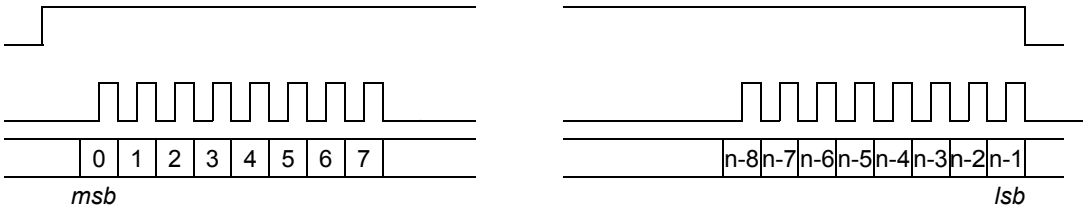

Figure 4: *Synchronous bit serial waveform for PDFE*

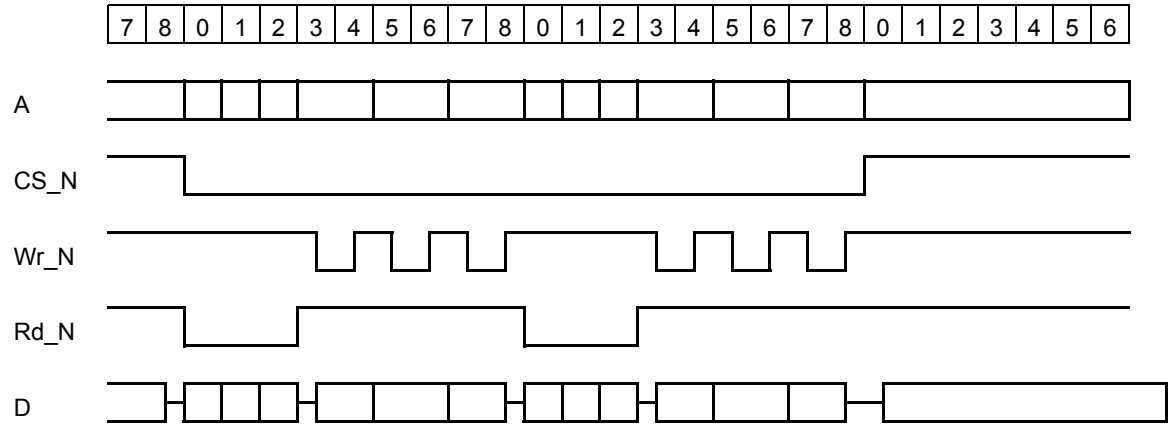

Figure 5: *Two consecutive nine clock period cycles on the memory interface*

2.7 Functional specification

The SEPT FPGA architecture can be seen as a group of separate functions controlled by a central control unit which is being commanded by a single user interface. The architecture is separated as far as possible into two logical domain, one for each telescope. This is specifically true for the interfaces towards the PDFEs and the memories. Common parts are the centralised control and communications functions, calibration function and timer. The two telescopes can be operated simultaneously or one at the time providing power saving.

2.7.1 Control

The control block provides command decoding and response generation as defined in table 7. In most cases a command response is generated after a complete command action has been performed and all data is transmitted (table 7 for exceptions).

The *PdfeA_Clk* and *PdfeB_Clk* output clocks are generated from the *Clk18* input clock frequency, dividing it every even cycle with 4 and every odd cycle with 5, giving a mean frequency $f_{CK4} = f_{CK18}/4.5$, or 4 MHz at $f_{CK18} = 18$ MHz. There is no long term drift, but the jitter is +/- T_{CK18} / 2. The PDFE internal charge event detection and handling cycle is an even number of T_{CK18} periods, thus not affected by the asymmetric clock division.

2.7.2 Filters

The event detection signals of the main and secondary channels of the two PDFEs belonging to the same telescope are used in the SEPT FPGA device to provide additional filtering options to those implemented in the PDFE. The result from the purely combinatorial signal filtering in the SEPT FPGA device is fed back to the external digital anti/coincidence input of each PDFE, letting the PDFE perform the final filtering and masking of the data valid signal. The filtering in the PDFE is done according to a window of opportunity principal as described in AD1.

The filtering settings in the SEPT FPGA device are done individually per PDFE without any constraints between PDFEs. See table 7 (*cConfFiltr*) for details on the configuration of the filtering in the SEPT FPGA device. The filtering is done on a programmable anti/coincidence basis. Note that the SEPT FPGA device only provides a signal pattern for the external digital anti/coincidence input of each PDFE, no event filtering is actually done in the SEPT FPGA device itself.

The PDFE should be set in coincidence or anti-coincidence mode corresponding to the settings in table 7. For the configuration of the PDFE filtering see AD1 and table 4 for details. The only constraint between PDFEs of the same telescope are the discriminator settings of the main and secondary channels that could affect the outcome of the filtering.

A final stage of global filtering is provided for both telescopes based on either direct user control or through causes internal to the SEPT FPGA device such as expiration of the alarm timer, saturation of the event counters, configuration error or latchup detection. See table 7 (*cStartRun*) for details on the configuration of the overall measurement setup supported by the SEPT FPGA device.

2.7.3 Arithmetic

After a particle detection event has been filter as described here above it will be counted as an event in one specific counter. The arithmetic function comprises a boundary function to decide to which counter an event should be attributed to and a counter function implementing the increment of said counter which is stored in external memory. To separate the external interface between the two telescopes, each telescope has its own memory for counter storage. The arithmetic implementation is divided in two functional blocks: the binning boundary comparison function and the event counter function.

2.7.3.1 Boundary

Since each event can have a data value of 8 bits, there are 256 possible values that are taken into account. The SEPT FPGA device provides therefore 256 counters per PDFE, allowing the user to have one counter for each digital value. To facilitate data compression, the data space can be reduced to 32 bins bound by 33 boundary values, two being implicit. The usage of 32 or 256 counters is selectable per telescope. Each of the two boundary function provides two type of interfaces. Two event interfaces, one for each PDFE, handshake based and one counter increment interface, also handshake based. The boundary implementation is divided in three functional blocks: the arbiter function, the comparison function and the boundary table storage.

2.7.3.1.1 Arbiter

Since there are only two physical implementations of the boundary table storage, one for each telescope, these resources need to be shared between the PDFEs. The arbitration is done between two PDFEs in a telescope. Arbitration of the first boundary table is performed between PDFE 0 and PDFE 1. Arbitration of the second boundary table is performed between PDFE 2 and PDFE 3. Note that all functions of the arithmetic function are implemented per telescope. The arbitration is implemented not to introduce any bandwidth limitation with respect to incoming events, although a latency is introduced due to the pipelined architecture.

2.7.3.1.2 Boundaries

There are 33 boundary values, two being implicit, to which an incoming event data value is compared to. The boundaries are indexed from -1 to *n*-1, where *n*=32. The lower boundary is limited by the implicit boundary value of 2^0-1=0, indexed as number -1. The upper boundary is limited by the implicit boundary value of 2^8-1=255, indexed as number *n*-1. The boundaries table memory is indexed from 0 to *n*-2, containing all explicit boundary values. The incoming event data value is compared to the boundary values and the comparison is done on a smaller-or-equal-to basis. The boundary width is eight bits. The default boundary values at power-on are selectable at design time. There is one exponential table for both type of detector, i.e. an identical table for electron and proton data. The boundary table is listed in table 5.

2.7.3.1.3 Comparison

The comparison between an incoming event data value and the boundary table entries is performed according to the algorithm outlined hereafter. All 8 bits of each incoming event data value is compared to the boundary values. The output of each comparison is a value indicating the index of the counter to be incremented. The width of this value is 8 bits. Note that since there are 33 boundaries, thus 32 bins, the boundary comparison result will be bound between 0 and 31, only using 32 out of the $2^8 = 256$ counters.

The comparison begins with assuming a default result value of 31, corresponding to the last bin. The incoming event data value is then compared with the boundaries beginning at index 0 and continuing to index 30. If the event data value is less-or-equal-to the compared boundary, the comparison is aborted and the resulting value is the index number of the boundary.

2.7.3.2 Counters

Each telescope has several counters which are implemented in an external memory. There is one memory device per telescope. The counters are divided in pages, since being stored and addressed as pages in the external memory. Each page contains one set of counters for each of the two PDFE belonging to the telescope. Each set of counters can be used in two different ways, either as 256 counters or as 32 counters when compression (or binning) is applied. Only one page can be used at a time for counting events. It is not possible to use counters sets from different pages for two PDFEs in the same telescope.

Simultaneously while counting events, the counters can be read via the bit asynchronous command interface. Only one page can be read at the time, and it can be either the one being used for counting the events or one of the three others. Note that if reading the same page as being used for counting events, some results may be incorrect since each read actually clears the counter value. The setting of the pages for event counting and read out is controlled via the asynchronous bit serial command interface. The clear and read out possibilities for the counters are described further in table 7 (*cConfCntr*). The counter implementation can be divided in two functional blocks: the increment function and the memory interface.

2.7.3.2.1 Increment

The generic counter bit numbering is from 0 to 31, where 0 is the most significant and 31 is the least significant. Note that in the current 24 bit counter width configuration, bit number 8 is most significant. The individual counter will not wrap around, instead it will stick at its largest possible value when saturating. When this occurs, an internal interrupt will be generated which can be used to latch the timer value and to finish an measurement session as described in section 2.7.8. An interrupt on the external interrupt signal will also be generated on the first aforementioned occurrence in a measurement session or until the interrupt registers is cleared (table 7, *cClearIrq*).

2.7.3.2.2 Memory interface

The counters are stored in the external static memory with at least 8192 8 bit wide words per telescope. They are stored as four pages of 256 counters per PDFE. Each telescope has its own memory. The baseline memory is the 60 ns access time HC6256, RD17. There is no memory protection. For each 24 bit wide counter access, three byte reads are performed, followed by three byte writes. Note that the counter will always be written after being read. The counters can be read via the asynchronous bit serial command interface, after which they are automatically cleared. Either 32 or 256 counters can be read out (table 7, *cRead32* and *cRead256*). Note that the counter memory is not initialised at power up or after a reset and needs to be cleared before usage (table 7, *cInitCntr*).

The memory is accessed on a strict 9 Clk clock period cycle derived from the system clock, providing sufficient memory bandwidth for each PDFE. Slots in the memory clock period cycle that are unused will not result in unnecessary memory accesses. When the memory is not accessed, the SEPT FPGA device will de-assert strobe signals. This scheme provides the following bandwidth per PDFE:

$$\text{events / second} = f_{CK} / 9_{cycles} / 2_{PDFEs}$$

In case of simultaneous read out of one page while a measurement is ongoing on a second page of the same telescope, the bandwidth per PDFE will be decreased proportionally to the transmitting data rate of the asynchronous bit serial interface (57600 baud):

$$\text{events / second} = ((f_{CK} / 9_{cycles}) - (57600/ 11_{bits} / 3_{bytes}))_{events} / 2_{PDFEs}$$

The two most significant address bits on the memory are tied permanently to zero on the board. The counters are stored page wise in memory, with the most significant bit of the address being occupied by the bit selecting between PDFE 0 and 1 for telescope A, and PDFE 2 and 3 for telescope B. The two following bits are occupied by the page address. The eight following bits are occupied by counter selection and the last two by the individual byte selection within a counter.

The counter values are stored in 32 bit word aligned address. To give an example, assuming PDFE 1 and a page address of 3, counter numbered 0 is stored in addresses 0C00h to 0C03h, counter numbered 1 is stored in addresses 0C04h to 0C07h, and so forth until counter numbered 255 which is stored in address 0FFCh to 0FFFh. The most significant byte of a counter is stored in address 01b and the least significant byte is stored in 11b within the counter address. See table 6 for more detailed information.

The order of reading and writing of a counter value is from the least to the most significant byte. The least significant byte of a counter is thus read first, i.e. bits 24 to 31, followed by the next byte, i.e. bits 16 to 23, followed by the most significant byte in case of 24 bit wide counters, i.e. bits 8 to 15, and finally followed by the most significant byte in case of 32 bit wide counters, i.e. bits 0 to 7. For each byte, the left most bit is most significant. The most significant byte of each counter is transmitted first over the bit asynchronous command interface (table 7, *cRead32* and *cRead256*).

2.7.4 Asynchronous interface

The asynchronous bit serial interface adheres to the bit protocol defined in AD3 and depicted in table 1 and figure 3. The interface support hardware handshake and will not begin a transmission of a byte until the request to send input signal *RsRequest* is asserted. Since the interface is always ready to receive, the clear to send output signal *RsClear* will be asserted as soon as the *RsRequest* input is observed asserted. The handling of received bytes is described in detail in table 7. The *RsRequest* input can be asserted permanently.

In addition to transmitting and receiving bytes, the interface also generates a `BREAK` code on the occurrence of an interrupt. This is done be transmitting a zero start bit, one byte with the data field all zero, two stop bits also being zero and an additional zero bit in order to violate the nominal protocol. This is done nearly simultaneously with the assertion of the external interrupt signal, only delayed by any ongoing byte transmission.

The receiving and transmitting data rate is 57600 baud. The communication interface can be reset via a user command, see table 7 (*cRstComm*).

It is assumed that there is at most 1,8 ms (at 4,5 MHz) between the reception of a command byte and subsequent argument(s) on the input interface. Otherwise a time out response will be generated (table 7, *rTimeOut*) and the access will be aborted.

2.7.5 Synchronous interface

The synchronous bit serial interface provides a means for individual programming of the four PDFEs in the SEPT instrument. The programming is fully controlled via the asynchronous bit serial command interface, the SEPT FPGA device only providing the transparent data transport between the two interfaces. While the PDFE is programmed, the pervious status of the PDFE is read back and transmitted on the asynchronous bit serial command interface. The SEPT instrument does not have the capability to program a PDFE on its own.

The synchronous bit serial interface adheres to the protocol defined in AD1 and depicted in table 3 and figure 4. The data rate is the system clock frequency divided by 16, but data are transmitted in bursts since regulated by the asynchronous bit serial command interface. Note that any usage of hardware handshake on the asynchronous bit serial command interface could result in loss of data since the ready signalling from the interface is not taken into account during this operation although the external communication protocol is respected.

Although there is only one synchronous interface implemented in the SEPT FPGA device, a separation between interface signals is done for the telescopes and to some extent between the PDFEs within a telescope. However, only one PDFE can be programmed at the time. For each telescope there is a common data clock and a common data output from the SEPT FPGA device for the PDFE pair. For each PDFE there is an individual message delimiter (or chip select) and a data input (to the SEPT FPGA device). In this way a failure on one of the PDFE outputs will not affect the other devices.

2.7.6 Housekeeping

The SEPT instrument hosts two analogue multiplexers which are used for multiplexing analogue observation points towards a dedicated analogue input on the PDFE devices. By configuring the corresponding PDFE and commanding the SEPT FPGA device, the output of the analogue multiplexer can be read through the PDFE, which performs the analogue to digital conversion, and be reported to the user through the asynchronous bit serial command interface. Housekeeping cannot be performed while event measurements are taking place on the PDFE addressed for housekeeping. The operating measurement mode of the SEPT FPGA device must thus be disabled as defined in table 7 (*cConfPDFE*).

To facilitate the housekeeping function, PDFE in question needs to be configured in the analogue to digital mode as defined in AD1 and table 4. The housekeeping gathering can be done via either PDFE on each telescope. Housekeeping reporting can only be performed on one telescope at a time and will prevent any simultaneous event measurements on the effected PDFE. The order in which the analogue inputs of the multiplexer are sampled during housekeeping is defined in table 7 (*cGetHK*). The time between samples is 3,64 ms (at 4,5 MHz Clk frequency), to allow input to settle properly.

It is also possible to measure the rate of events on the main and guard detectors of the different PDFEs. The selection of which detector to measure is done via a user command as defined in table 7 (*cGetSingle*). The selection can only be made between measurements to have an effect. The single counter measurement is started simultaneously with a measurement session when enabled (table 7, *cStartRun*). The measurement will commence until the alarm time expires when enabled, or by means of a stop measurement command, see table 7 (*cStopRun*). The 24 bit value of the single counter can be read out by means a command defined in table 7 (*cGetSingle*). This non-intrusive diagnostic single counter mode measurement can be performed during nominal measurement mode and calibration. The counter width of 24 bits covers 60 seconds of worst case event detection on a detector (at 4,5 MHz Clk frequency). The counter saturates on the *all ones* value. The single counter can be read out at any time, but might give corrupted results if read during a measurement. The single counter in unaffected by latchup or PDFE errors.

2.7.7 Calibration

Calibration is supported by means of test pulse generation on main and secondary channels (guard or anti/coincidence channel). Test pulses are generated for both telescopes simultaneously. It is possible to enable pulses on only on the even numbered channels, or on only the odd numbered channels (table 7, *cConfCal*). It is thus possible to target any PDFE channel on a telescope individually, but exactly the same events will occur on the other telescope as well. The amplitude of the test pulses is controllable per measurement session (table 7, *cConfCal*). One of four output address values can be selected.

The output pulse will have a width of 56 ns (at 18 MHz Clk18 oscillator frequency). The time between any two pairs of test pulses is about 910 µs (at 4,5 MHz Clk frequency).

The calibration is started by means of the start measurement command, see table 7 (*cStartRun*), clearing and starting the timer, and will continue until a timer alarm occurs. The calibration is disabled on completion or by means of the stop measurement command, see table 7 (*cRstFPGA, cStopRun*).

The calibration output signals will only be asserted at the beginning of the measurement session, with the pulse amplitude and enable outputs being asserted, simultaneously, only during the actual pulse occurrence. At the end of a measurement session, all calibration output signals will be automatically deasserted. A new calibration setting will not have any affect until the next measurement session.

2.7.8 Timer

The SEPT FPGA device comprises a multi function timer to allow the SEPT instrument to operate under precise timing constrains posed by the measurement session. The timer acts simultaneously as an alarm facility, generating an interrupt when a desired time period has elapsed; and as a datation facility, latching the elapsed time on an interrupt such as the saturation of an event counter. The format of the timer is described in section 2.5.2.

The timer is mainly used for keeping track and controlling the duration of a measurement session. It can either be used for limiting the measurement duration by means of a programmable alarm time or to note the actual duration of the measurement. The alarm time is programmable via the asynchronous bit serial command interface, see table 7 (*cSetTimer*). The timer is always stopped and reset to zero upon the programming of the alarm time.

The timer is always cleared and starts upon the reception of the start measurement command, see table 7 (*cStartRun*), by which incoming events are allowed to propagate to the event counters, which also starts the calibration when enabled. The measurement will commence until the alarm time expires when enabled, or by means of a stop measurement command, see table 7 (*cStopRun*), upon which all incoming events will be prevented from propagating to the counters.

The timer can be read out instantaneously via the asynchronous bit serial command interface. Note that this might lead to reading an incorrect value due to lack of synchronisation between the time counter and the command interface, if the measurement is ongoing at that time.

In addition to controlling or noting the measurement time, it is possible to capture the timer value at the occurrence of an external interruption such as latchup or PDFE configuration error, or due to an event counter saturation. Only the first such event will lead to a time datation, one per telescope. If enabled (table 7, *cStartRun*), the occurrence of a counter saturation will also stop the overall measurement on the effected telescope. A latchup or PDFE configuration error will always stop the overall measurement on the effected telescope.

The datation registers are readable via the asynchronous bit serial command interface. The value will be all zero before the occurrence of a datation. At the end of an measurement, due to reaching the alarm timer, calibration completion or by commanding, the current timer value is copied to the datation registers if no other event has caused a previous datation during the measurement. This allows the user to determine the measurement duration and to correlate it with the captured event data.

The counter in the timer is based on a synthesizer to generate an internal binary clock frequency. The obtained synthesized frequency with a 32 bit wide frequency synthesizer is $f_{synth\ obtained} = f_{CK} * 244335 / 2^{32}$. The resulting static drift caused by the ration between the ideal and obtained synthesized frequency is 225 microseconds per minute, or 0,25 seconds over the full length of the counter, for a system frequency f_{CK} = 4,5 MHz. The increment value in the above equation is fixed by design and needs to be modified for other system frequencies than mentioned here.

2.7.9 Interrupt

An external interrupt is generated when the alarm timer reaches the preset alarm time, on the saturation of an event counter (for each telescope), on the detection of a configuration error in a PDFE, and on the detection of a latchup on the analogue or digital power supply to a PDFE pair. The external interrupt signal is asserted and a BREAK response is issued on the asynchronous command interface. The interrupt is generated only once per such occurrence until the interrupt register is cleared by a user command (table 7, *cClearIrq*). Any subsequent interrupt occurrences after the initial one will be registered in the interrupt register. The different sources are masked under certain conditions to avoid incorrect generation of interrupts.

A timer alarm can only generate an interrupt during a measurement session when enabled (table 7, *cStartRun*). The corresponding bit in the interrupt register will however always be set by an occurrence during a measurement.

A counter saturation can only generate an interrupt during a measurement session when enabled (table 7, *cStartRun*). The corresponding bit in the interrupt register will however always be set by an occurrence during a measurement, providing the possibility to check for counter saturation without analysing all counter data.

A PDFE configuration error can only generate an interrupt when the PDFE is powered, the SEPT FPGA device outputs are driven towards the PDFEs, the PDFE is enabled (not in reset mode) and when no PDFE configuration is ongoing (table 7, *cConfPDFE*). The detection of the external interrupt source is edge sensitive. The corresponding bit in the interrupt register will only be set when the interrupt source is unmasked. The PDFE error inputs can however always be observed directly via the asynchronous command interface (table 7, *cStatPDFE*).

A latchup detection can only generate an interrupt when the corresponding PDFE pair is powered and the SEPT FPGA device outputs are driven towards the PDFEs. The detection of the external interrupt source is edge sensitive with a minimum programmable duration for the time the input is asserted (table 7, *cConfLatch*). The corresponding bit in the interrupt register will only be set when the interrupt source is unmasked. The external latchup inputs can however always be observed directly via the asynchronous command interface (table 7, *cStatPDFE*). Upon a latchup detection, both PDFEs of the affected telescope are powered down automatically and all signals going to these devices are put in high impedance state to avoid damages. The timer is also latched for the corresponding telescope at that time provided that a datation has not already occurred during a measurement session. The detection of a latchup during a measurement session when calibration is enabled (table 7, *cStartRun*), will be registered in the interrupt register.

In addition to the above interrupts, it is possible to observe the status of the global event propagation for each telescope during an ongoing measurement. Any configuration error or latchup detection during a measurement will be registered for each telescope in the interrupt register to allow for distinction between events during or after a measurement.

2.7.10 Operational modes

The SEPT FPGA devices provides four main operating modes. Configuration of the SEPT FPGA device and the PDFE devices is performed before a measurement, which also includes

the clearing of the event counter memory. Measurement is started by means of a command (*cStartRun*) after which only some of the available commands are useful. For each measurement session there are four measurement completion parameters that need to be specified: single counter measurement, timer alarm completion, counter saturation completion, and calibration. Any combination of the parameters is permitted. The overall measurement can be completed by the timer alarm, but counter saturation will only complete the measurement on the affected telescope. The detection of a PDFE configuration error or a latchup will complete the measurement on the affected telescope only. The overall measurement can also be stopped by direct commanding (*cStopRun*). Housekeeping can be performed in two ways, either by using one PDFE for analogue to digital conversion of the input of the analogue multiplexer, or by observing the main and guard events on a dedicated single counter. The former does not allow measurement on the used PDFE, but the latter does. Read-out of event counter and timer data can be performed during or after a measurement session, but some precaution must be taken (see section 2.7.3.2 and section 2.7.8). A session can thus be stopped by the different events listed hereafter.

Timer alarm expires, when enabled:
- measurement stops on both telescopes, events are not propagated any more
- forced datation on timer datation latches if not already triggered
- timer is stopped and is available for read out
- interrupt is generated

Counter saturation occurs, when enabled:
- measurement stops on affected telescope, events are not propagated any more
- datation on timer datation latch if not already triggered
- interrupt is generated

Latchup during calibration, when enabled and when not masked:
- measurement stops on affected telescope, events are not propagated any more
- forced datation on timer datation latch if not already triggered
- interrupt is generated

PDFE configuration error or latchup detection, when not masked:
- measurement stops on affected telescope, events are not propagated any more
- forced datation on timer datation latch if not already triggered
- interrupt is generated

Stop measurement command:
- measurement stops on both telescopes, events are not propagated any more
- forced datation on timer datation latches if not already triggered
- timer is stopped and is available for read out

2.7.11 Initialisation, state after reset and error handling

When the *Reset_N* input is asserted, the complete SEPT FPGA device is reset, including the configuration registers for which default values are specified in table 7. All registers are reset with an internally synchronised reset signal. All registers in the SEPT FPGA device can be reset by a user command, see table 7 (*cRstFPGA*).

All PDFE inputs to the SEPT FPGA are internally gated to remove their effect on the FPGA when the corresponding PDFE is not powered. The only exception is the PDFE error and the latchup detection signals, which are gated to avoid interrupt generation, but can still be observed via a user command, see table 7 (*cStatPDFE*).

2.8 Metastability

The possibility of metastability phenomena has been reduced by synchronising all asynchronous inputs or signals going between clock domains with two cascaded registers.

2.9 Radiation tolerance

The SEPT FPGA design has not been designed using explicit SEU mitigation techniques. The SEU sensitivity and total dose resistivity of the FPGA technology is specified in RD13.

2.10 Application note

This is an incomplete example of how to command and use the SEPT instrument, refer to table 7 for details. After power up a *cRstFPGA* response should be received, the SEPT FPGA device is now in its state after reset. Power the PDFEs using the *cPwrPDFE* command. Drive the SEPT FPGA device outputs, including the PDFE clocks, towards the PDFEs using the *cDrvPDFE* command. Select digital mode for the PDFE event output using the *cCtrlPDFE* command. Release the reset on PDFEs using the *cEnPDFE* command. Program the four PDFEs individually using the *cConfPDFE* command. Check the configuration error and latchup status of the PDFEs using the *cStatPDFE* command.

Configure the SEPT FPGA device event filtering using the *cConfFiltr* command. Select between 32 or 256 counters and set counter pages using the *cConfCntr* command. Clear the counters for the four PDFEs using the *cInitCntr* command. Set the alarm time using the *cSetTimer* command. Configure the calibration using the *cConfCal* command. The instrument is now ready for a measurement which can be started using the *cStartRun* command, selecting between nominal or calibration mode.

During the measurement, the event rate on the main and guard detectors can be observed using the *cGetSingle* command. Housekeeping data can only be obtained with the *cGetHK* command if the targeted PDFE is firstly put in analogue to digital mode using the *cConfPDFE* command, during which no event measurement is possible. The measurement session can be aborted using the *cStopRun* command. The measurement results are read out from the memory using either the *cRead32* or *cRead256* command. The measurement time can be received using the *cReadTimer* and *cReadDate* commands. Interrupts can be identified and cleared using the *cClearIrq* command.

3 INTERFACES AND SIGNAL DESCRIPTION

Clock divider interface		
Reset_N	in	Asynchronous reset
Clk	in	System clock, see table 10, f_{CK}
Clk18	in	Crystal oscillator clock, see table 10, f_{CK18}
Clk4_5	out	Clk18 divided by a factor of four
Identification interface		
Id[0-2]	in	Identification
Asynchronous bit serial interface (inverted)		
RsIrq	out	Interrupt
RsIn_N	in	Serial input data
RsOut_N	out	Serial output data
RsRequest	in	Request to send
RsClear	out	Clear to send
PDFE power and reset interface		
PdfeA_Pwr	out	PDFE 0 / 1 power enable
PdfeB_Pwr	out	PDFE 2 / 3 power enable
PdfeA_Reset_N	out	PDFE 0 / 1 reset and low power mode enable
PdfeB_Reset_N	out	PDFE 2 / 3 reset and low power mode enable
PDFE configuration interface		
PdfeA_AOutSel	out	PDFE 0 / 1 analogue output enable
PdfeB_AOutSel	out	PDFE 2 / 3 analogue output enable
PDFE programming interface A (for PDFE 0 / 1)		
PdfeA_SClk	out	PDFE 0 / 1 bit clock
PdfeA_SOut	out	PDFE 0 / 1 input data
Pdfe0_SEn	out	PDFE 0 configuration select
Pdfe1_SEn	out	PDFE 1 configuration select
Pdfe0_SIn	in	PDFE 0 output data
Pdfe1_SIn	in	PDFE 1 output data
PDFE programming interface B (for PDFE 2 / 3)		
PdfeB_SClk	out	PDFE 2 / 3 bit clock
PdfeB_SOut	out	PDFE 2 / 3 input data
Pdfe2_SEn	out	PDFE 2 configuration select
Pdfe3_SEn	out	PDFE 3 configuration select
Pdfe2_SIn	in	PDFE 2 output data
Pdfe3_SIn	in	PDFE 3 output data

Table 8: *Signal overview, the name suffix "_N" indicates an active low signal.*

PDFE 0 event interface		
Pdfe0_EDOut	in	PDFE 0 main event detection
Pdfe0_ICoOut	in	PDFE 0 internal coincidence
Pdfe0_PCS_N	in	PDFE 0 conversion ready
Pdfe0_XCoIn	out	PDFE 0 external coincidence
Pdfe0_PEn_N	out	PDFE 0 parallel data output enable
Pdfe0_POut[0-7]	in	PDFE 0 parallel data output
PDFE 1 event interface		
Pdfe1_EDOut	in	PDFE 1 main event detection
Pdfe1_ICoOut	in	PDFE 1 internal coincidence
Pdfe1_PCS_N	in	PDFE 1 conversion ready
Pdfe1_XCoIn	out	PDFE 1 external coincidence
Pdfe1_PEn_N	out	PDFE 1 parallel data output enable
Pdfe1_POut[0-7]	in	PDFE 1 parallel data output
PDFE 2 event interface		
Pdfe2_EDOut	in	PDFE 2 main event detection
Pdfe2_ICoOut	in	PDFE 2 internal coincidence
Pdfe2_PCS_N	in	PDFE 2 conversion ready
Pdfe2_XCoIn	out	PDFE 2 external coincidence
Pdfe2_PEn_N	out	PDFE 2 parallel data output enable
Pdfe2_POut[0-7]	in	PDFE 2 parallel data output
PDFE 3 event interface		
Pdfe3_EDOut	in	PDFE 3 main event detection
Pdfe3_ICoOut	in	PDFE 3 internal coincidence
Pdfe3_PCS_N	in	PDFE 3 conversion ready
Pdfe3_XCoIn	out	PDFE 3 external coincidence
Pdfe3_PEn_N	out	PDFE 3 parallel data output enable
Pdfe3_POut[0-7]	in	PDFE 3 parallel data output
PDFE status interfaces		
Pdfe0_Err_N	in	PDFE 0 internal error
Pdfe1_Err_N	in	PDFE 1 internal error
Pdfe2_Err_N	in	PDFE 2 internal error
Pdfe3_Err_N	in	PDFE 3 internal error
PdfeA_ASEL_N	in	PDFE 0 or 1 $VDD_{analogue}$ latchup detected
PdfeA_DSEL_N	in	PDFE 0 or 1 $VDD_{digital}$ latchup detected
PdfeB_ASEL_N	in	PDFE 2 or 3 $VDD_{analogue}$ latchup detected
PdfeB_DSEL_N	in	PDFE 2 or 3 $VDD_{digital}$ latchup detected
PDFE clock interface		
PdfeA_Clk	out	PDFE 0 / 1, 4 MHz clock
PdfeB_Clk	out	PDFE 2 / 3, 4 MHz clock

Table 8: *Signal overview, the name suffix "_N" indicates an active low signal.*

Analogue multiplexer interfaces		
AdcA_Mux[0-1]	out	
AdcB_Mux[0-1]	out	
Calibration interface		
Cal_Enable	out	General main and guard pulse on all PDFEs
Cal_A_1	out	Pulse amplitude selector, most significant address
Cal_A_0	out	Pulse amplitude selector, least significant address
Cal_M_Even	out	Enable main pulse on PDFE 0 / 2
Cal_M_Odd	out	Enable main pulse on PDFE 1 / 3
Cal_G_Even	out	Enable guard pulse on PDFE 0 / 2
Cal_G_Odd	out	Enable guard pulse on PDFE 1 / 3
Memory interface A (SRAM A for PDFE 0 / 1)		
CSA_N	out	Chip select
WrA_N	out	Write strobe
RdA_N	out	Read strobe
AddressA[0-12]	out	Address
DataA[0-7]	inout	Data
Memory interface B (SRAM B for PDFE 2 / 3)		
CSB_N	out	Chip select
WrB_N	out	Write strobe
RdB_N	out	Read strobe
AddressB[0-12]	out	Address
DataB[0-7]	inout	Data
Upward compatibility with A54SX72A		
Pin25	out	54SX72 I/O - N/C
Pin65	out	54SX72 I/O - N/C
Pin132	out	54SX72 I/O - N/C
Pin74	out	54SX72 Quadrant clock A / GND
Pin84	out	54SX72 Quadrant clock B / GND
Pin190	out	54SX72 Quadrant clock C / GND
Pin178	out	54SX72 Quadrant clock D / GND
Pin18	out	54SX72 GND
Pin19	out	54SX72 VCCA
Pin83	out	54SX72 VCCI
Pin116	out	54SX72 GND
Pin117	out	54SX72 VCCA
Pin187	out	54SX72 VCCI
Pin3	out	dummy output / N/C
SpareA - SpareG	out	always deasserted

Table 8: *Signal overview, the name suffix "_N" indicates an active low signal.*

3.1 Clock divider interface

3.1.1 *Reset_N*: Asynchronous reset (I)

This asynchronous active low input resets the SEPT FPGA device. The signal is synchronised internally to avoid metastability with respect to the different clock inputs.

3.1.2 *Clk*: System clock (I)

This input is the system clock signal for the SEPT FPGA device. Most registers are clocked on the rising Clk edge. A few registers, all related to the memory interface, are clocked on the falling Clk edge. For nominal operating frequency see section 4.12, f_{CK}.

3.1.3 *Clk18*: Crystal Oscillator clock (I)

This input is the crystal oscillator clock input for the SEPT FPGA device. A few registers are clocked on the rising Clk18 edge. For nominal operating frequency see section 4.12, f_{CK18}.

3.1.4 *Clk4_5*: Divided clock output (O)

This output carries a clock derived from the rising Clk18 input edge.

3.2 Identification interface

3.2.1 *Id[0-2]*: Identification input data (I)

This static input sets the identification value. The FPGA should be reset after a value change.

3.3 Asynchronous bit serial interface (inverted)

3.3.1 *RsIrq*: Interrupt (O)

This active high output is asserted to inform of an internal SEPT instrument event. Pulled down during power up.

3.3.2 *RsIn_N*: Serial input data (I)

This asynchronous serial data input carries the bit asynchronous data stream. The communication format is specified in section 2.6 and the baud rate is specified in section 4.12.

3.3.3 *RsOut*: Serial output data (0)

This output carries the bit asynchronous data stream. The communication format is specified in section 2.6 and the baud rate is specified in section 4.12. The output changes on rising Clk edge. Pulled up during power up.

3.3.4 *RsRequest*: Request to send (I)

This asynchronous active high input is asserted when host is requesting communication.

3.3.5 *RsClear*: Clear to send (O)

This active high output is asserted when the SEPT is enabling communication. The output changes state on rising Clk edge.

3.4 PDFE power and reset interface

3.4.1 *PdfeA_Pwr*: PDFE 0 and 1 power enable (O)

This active high output enables the power supply of PDFE 0 and 1 when asserted. The output changes state on the rising Clk edge. Pulled down during power up.

3.4.2 *PdfeB_Pwr*: PDFE 2 and 3 power enable (O)

This active high output enables the power supply of PDFE 2 and 3 when asserted. The output changes state on the rising Clk edge. Pulled down during power up.

3.4.3 *PdfeA_Reset_N*: PDFE 0 and 1 reset (O)

This active low output resets PDFE 0 and 1 when asserted, changes state on the rising Clk edge.

3.4.4 *PdfeB_Reset_N*: PDFE 2 and 3 reset (O)

This active low output resets PDFE 2 and 3 when asserted, changes state on the rising Clk edge.

3.5 PDFE configuration interface

3.5.1 *PdfeA_AOutSel*: PDFE 0 and 1 analogue output enable (O)

This active high output enables the analogue output of PDFE 0 and 1 when asserted. The output changes state on the rising Clk edge.

3.5.2 *PdfeB_AOutSel*: PDFE 2 and 3 analogue output enable (O)

This active high output enables the analogue output of PDFE 2 and 3 when asserted. The output changes state on the rising Clk edge.

3.6 PDFE status interface

3.6.1 *Pdfe0_Err_N*: Internal error (I)

This active low asynchronous input indicates an internal PDFE 0 error when asserted.

3.6.2 *Pdfe1_Err_N*: Internal error (I)

This active low asynchronous input indicates an internal PDFE 1 error when asserted.

3.6.3 *Pdfe2_Err_N*: Internal error (I)

This active low asynchronous input indicates an internal PDFE 2 error when asserted.

3.6.4 *Pdfe3_Err_N*: Internal error (I)

This active low asynchronous input indicates an internal PDFE 3 error when asserted.

3.6.5 *PdfeA_ASEL_N*: Latchup (I)

This active low asynchronous input indicates a PDFE 0 or 1 analogue latchup when asserted.

3.6.6 *PdfeA_DSEL_N*: Latchup (I)

This active low asynchronous input indicates a PDFE 0 or 1 digital latchup when asserted.

3.6.7 *PdfeB_ASEL_N*: Latchup (I)

This active low asynchronous input indicates a PDFE 2 or 3 analogue latchup when asserted.

3.6.8 *PdfeB_DSEL_N*: Latchup (I)

This active low asynchronous input indicates a PDFE 2 or 3 digital latchup when asserted.

3.7 PDFE programming interface, telescope A

3.7.1 *PdfeA_SClk*: Serial data bit clock (O)

This output carries the bit clock for the programming of PDFE 0 and 1. Data are to be sampled on the rising PdfeA_SClk edge. The clock rate is specified in section 4.12. The output changes state on the rising Clk edge.

3.7.2 *PdfeA_SOut*: Serial output bit data (O)

This output carries the serial bit data for the programming of PDFE 0 and 1. Data are to be sampled on the rising PdfeA_SClk edge. The communication format is specified in section 2.5. The clock rate is specified in section 4.12. The output changes state on the rising Clk edge.

3.7.3 *Pdfe0_SEn*: Message delimiter and chip select (O)

This active high output delimits the serial message for the programming of PDFE 0. Data are to be received by the PDFE when Pdfe0_SEn is asserted. The output changes state on the rising Clk edge.

3.7.4 *Pdfe1_SEn*: Message delimiter and chip select (O)

This active high output delimits the serial message for the programming of PDFE 1. Data are to be received by the PDFE when Pdfe1_SEn is asserted. The output changes state on the rising Clk edge.

3.7.5 *Pdfe0_SIn*: Serial input bit data (I)

This input contains the previous data from the PDFE 0 programming. Data are sampled on the rising PdfeA_SClk edge when Pdfe0_SEn is asserted.

3.7.6 *Pdfe1_SIn*: Serial input bit data (I)

This input contains the previous data from the PDFE 1 programming. Data are sampled on the rising PdfeA_SClk edge when Pdfe1_SEn is asserted.

3.8 PDFE programming interface, telescope B

3.8.1 *PdfeB_SClk*: Serial data bit clock (O)

This output carries the bit clock for the programming of PDFE 2 and 3. Data are to be sampled on the rising PdfeB_SClk edge. The clock rate is specified in section 4.12. The output changes state on the rising Clk edge.

3.8.2 *PdfeB_SOut*: Serial output bit data (O)

This output carries the serial bit data for the programming of PDFE 2 and 3. Data are to be sampled on the rising PdfeB_SClk edge. The communication format is specified in section 2.5. The clock rate is specified in section 4.12. The output changes state on the rising Clk edge.

3.8.3 *Pdfe2_SEn*: Message delimiter and chip select (O)

This active high output delimits the serial message for the programming of PDFE 2. Data are to be received by the PDFE when Pdfe2_SEn is asserted. The output changes state on the rising Clk edge.

3.8.4 *Pdfe3_SEn*: Message delimiter and chip select (O)

This active high output delimits the serial message for the programming of PDFE 31. Data are to be received by the PDFE when Pdfe3_SEn is asserted. The output changes state on the rising Clk edge.

3.8.5 *Pdfe2_SIn*: Serial input bit data (I)

This input contains the previous data from the PDFE 2 programming. Data are sampled on the rising PdfeB_SClk edge when Pdfe2_SEn is asserted.

3.8.6 *Pdfe3_SIn*: Serial input bit data (I)

This input contains the previous data from the PDFE 3 programming. Data are sampled on the rising PdfeB_SClk edge when Pdfe3_SEn is asserted.

3.9 PDFE 0 event interface

3.9.1 *Pdfe0_EDOut*: Main event detection (I)

This asynchronous active high input indicates a main event detected by PDFE 0.

3.9.2 *Pdfe0_ICoOut*: Internal coincidence (I)

This asynchronous active high input indicates a coincidence detected by PDFE 0.

3.9.3 *Pdfe0_PCS_N*: Conversion ready (I)

This asynchronous active high input indicates that a main event has been detected and that the analogue to digital data conversion has been completed by PDFE 0.

3.9.4 *Pdfe0_XCoIn*: External coincidence (O)

This active high output indicates to the PDFE 0 that an external coincidence has taken place. The output changes state on the rising Clk edge.

3.9.5 *Pdfe0_PEn_N*: Enable parallel data (O)

This active low output enables the PDFE 0 parallel data output when asserted. The output changes state on the rising Clk edge. This output is permanently asserted.

3.9.6 *Pdfe0_POut[0-7]*: Parallel data input (I)

These signals carry the parallel data output from PDFE 0 when enabled by Pdfe0_PEn_N. The inputs are sampled on the rising Clk edge, but it is assumed that the value is stable after the detection of an asserted *Pdfe0_PCS_N* input. Bit 0 is the most significant.

3.10 PDFE 1 event interface

3.10.1 *Pdfe1_EDOut*: Main event detection (I)

This asynchronous active high input indicates a main event detected by PDFE 1.

3.10.2 *Pdfe1_ICoOut*: Internal coincidence (I)

This asynchronous active high input indicates a coincidences detected by PDFE 1.

3.10.3 *Pdfe1_PCS_N*: Conversion ready (I)

This asynchronous active high input indicates that a main event has been detected and that the analogue to digital data conversion has been completed by PDFE 1.

3.10.4 *Pdfe1_XCoIn*: External coincidence (O)

This active high output indicates to the PDFE 1 that an external coincidence has taken place. The output changes state on the rising Clk edge.

3.10.5 *Pdfe1_PEn_N*: Enable parallel data (O)

This active low output enables the PDFE 1 parallel data output when asserted. The output changes state on the rising Clk edge. This output is permanently asserted.

3.10.6 *Pdfe1_POut[0-7]*: Parallel data input (I)

These signals carry the parallel data output from PDFE 1 when enabled by Pdfe1_PEn_N. The inputs are sampled on the rising Clk edge, but it is assumed that the value is stable after the detection of an asserted *Pdfe1_PCS_N* input. Bit 0 is the most significant.

3.11 PDFE 2 event interface

3.11.1 *Pdfe2_EDOut*: Main event detection (I)

This asynchronous active high input indicates a main event detected by PDFE 2.

3.11.2 *Pdfe2_ICoOut*: Internal coincidence (I)

This asynchronous active high input indicates a coincidence detected by PDFE 2.

3.11.3 *Pdfe2_PCS_N*: Conversion ready (I)

This asynchronous active high input indicates that a main event has been detected and that the analogue to digital data conversion has been completed by PDFE 2.

3.11.4 *Pdfe2_XCoIn*: External coincidence (O)

This active high output indicates to the PDFE 2 that an external coincidence has taken place. The output changes state on the rising Clk edge.

3.11.5 *Pdfe2_PEn_N*: Enable parallel data (O)

This active low output enables the PDFE 2 parallel data output when asserted. The output changes state on the rising Clk edge. This output is permanently asserted.

3.11.6 *Pdfe2_POut[0-7]*: Parallel data input (I)

These signals carry the parallel data output from PDFE 2 when enabled by Pdfe2_PEn_N. The inputs are sampled on the rising Clk edge, but it is assumed that the value is stable after the detection of an asserted *Pdfe2_PCS_N* input. Bit 0 is the most significant.

3.12 PDFE 3 event interface

3.12.1 *Pdfe3_EDOut*: Main event detection (I)

This asynchronous active high input indicates a main event detected by PDFE 3.

3.12.2 *Pdfe3_ICoOut*: Internal coincidence (I)

This asynchronous active high input indicates a coincidence detected by PDFE 3.

3.12.3 *Pdfe3_PCS_N*: Conversion ready (I)

This asynchronous active high input indicates that a main event has been detected and that the analogue to digital data conversion has been completed by PDFE 3.

3.12.4 *Pdfe3_XCoIn*: External coincidence (O)

This active high output indicates to the PDFE 3 that an external coincidence has taken place. The output changes state on the rising Clk edge.

3.12.5 *Pdfe3_PEn_N*: Enable parallel data (O)

This active low output enables the PDFE 3 parallel data output when asserted. The output changes state on the rising Clk edge. This output is permanently asserted.

3.12.6 *Pdfe3_POut[0-7]*: Parallel data input (I)

These signals carry the parallel data output from PDFE 3 when enabled by Pdfe3_PEn_N. The inputs are sampled on the rising Clk edge, but it is assumed that the value is stable after the detection of an asserted *Pdfe3_PCS_N* input. Bit 0 is the most significant.

3.13 PDFE clock interface

3.13.1 *PdfeA_Clk*: 4 MHz clock output (O)

This output carries a clock derived from the rising Clk18 input edge. Used as the 4 MHz clock for PDFE 0 and PDFE 1.

3.13.2 *PdfeB_Clk*: 4 MHz clock output (O)

This output carries a clock derived from the rising Clk18 input edge. Used as the 4 MHz clock for PDFE 2 and PDFE 3.

3.14 Analogue multiplexer interface

3.14.1 *AdcA_Mux[0-1]*: Analogue multiplexer selection (O)

These outputs indicates the selection of the analogue multiplexer. The outputs change state on the rising Clk edge.

3.14.2 *AdcB_Mux[0-1]*: Analogue multiplexer selection (O)

These outputs indicates the selection of the analogue multiplexer. The outputs change state on the rising Clk edge.

3.15 Calibration interface

3.15.1 *Cal_Enable*: General main and guard pulse enable (O)

This active high output is asserted to generate a pulse one of the main or guard detector channels on the PDFEs. The output changes state on the rising Clk edge, but is resynchronised with the rising Clk18 clock edge to generate the short pulse width. The rate is specified in section 4.12.

3.15.2 *Cal_A_1*: Pulse amplitude selector, most significant bit (O)

This active output the most significant bit of the pulse amplitude selection for the calibration interface. The output changes state on the rising Clk edge, but is resynchronised with the rising Clk18 clock edge to generate the short pulse width.

3.15.3 *Cal_A_0*: Pulse amplitude selector, least significant bit (O)

This active output the least significant bit of the pulse amplitude selection for the calibration interface. The output changes state on the rising Clk edge, but is resynchronised with the rising Clk18 clock edge to generate the short pulse width.

3.15.4 *Cal_M_Even*: Enable pulses on PDFE 0 and 2 main channels (O)

This active high output is asserted to enable pulses on the main detector channels on PDFE 0 and 2. The output changes state on the rising Clk edge.

3.15.5 *Cal_M_Odd*: Enable pulses on PDFE 1 and 3 main channels (O)

This active high output is asserted to enable pulses on the main detector channels on PDFE 1 and 3. The output changes state on the rising Clk edge.

3.15.6 *Cal_G_Even*: Enable pulses on PDFE 0 and 2 guard channels (O)

This active high output is asserted to enable pulses on the coincidence detector channels on PDFE 0 and 2. The output changes state on the rising Clk edge.

3.15.7 *Cal_G_Odd*: Enable pulses on PDFE 1 and 3 guard channels (O)

This active high output is asserted to enable pulses on the coincidence detector channels on PDFE 1 and 3. The output changes state on the rising Clk edge.

3.16 Memory interface, telescope A

3.16.1 *AddressA[0-12]*: Memory address (O)

These outputs are the addresses generated by the SEPT FPGA device for reading and writing to the external memory. The outputs change state on the rising Clk edge.

3.16.2 *DataA[0-7]*: Memory data (I/O)

These signals are used to read and write data to the external memory. The outputs are driven by the SEPT FPGA device on the rising Clk edge and are tristated on the falling Clk edge. Driven while Reset_N is asserted.

3.16.3 *CSA_N*: Memory chip select (O)

This active low Chip Select for external memory, changes state on the rising Clk edge. Pulled up during power up.

3.16.4 *WrA_N*: Memory write strobe (O)

This active low Write Strobe for external memory, changes state on the falling Clk edge. Pulled up during power up.

3.16.5 *RdA_N*: Memory read strobe (O)

This active low read Strobe for external memory, changes state on the rising Clk edge. Pulled up during power up.

3.17 Memory interface, telescope B

3.17.1 *AddressB[0-12]*: Memory address (O)

These outputs are the addresses generated by the SEPT FPGA device for reading and writing to the external memory. The outputs change state on the rising Clk edge.

3.17.2 *DataB[0-7]*: Memory data (I/O)

These signals are used to read and write data to the external memory. The outputs are driven by the SEPT FPGA device on the rising Clk edge and are tristated on the falling Clk edge. Driven while Reset_N is asserted

3.17.3 *CSB_N*: Memory chip select (O)

This active low Chip Select for external memory, changes state on the rising Clk edge. Pulled up during power up.

3.17.4 *WrB_N*: Memory write strobe (O)

This active low Write Strobe for external memory, changes state on the falling Clk edge. Pulled up during power up.

3.17.5 *RdB_N*: Memory read strobe (O)

This active low read Strobe for external memory, changes state on the rising Clk edge. Pulled up during power up.

3.18 Upward compatibility with 54SX72

3.18.1 Pin25: 54SX72 I/O (O)

54SX72 spare I/O pin configured as output. Can be connected to test point.

3.18.2 Pin65: 54SX72 I/O (O)

54SX72 spare I/O pin configured as output. Can be connected to test point.

3.18.3 Pin132: 54SX72 I/O (O)

54SX72 spare I/O pin configured as output. Can be connected to test point.

3.18.4 Pin74: 54SX72 Quadrant clock A (O)

Do not use. Do not connect. Always deasserted.

3.18.5 Pin84: 54SX72 Quadrant clock B (O)

Do not use. Do not connect. Always deasserted.

3.18.6 Pin190: 54SX72 Quadrant clock C (O)

Do not use. Do not connect. Always deasserted.

3.18.7 Pin178: 54SX72 Quadrant clock D (O)

Do not use. Do not connect. Always deasserted.

3.18.8 Pin18, Pin116: 54SX72 GND (O)

Do not use. Do not connect. Always deasserted.

3.18.9 Pin19, Pin117: 54SX72 VCCA (O)

Do not use. Do not connect. Always deasserted.

3.18.10 Pin83, Pin187: 54SX72 VCCI (O)

Do not use. Do not connect. Always deasserted.

3.18.11 Pin3: Dummy output (O)

Do not use. Do not connect. Always deasserted.

3.18.12 SpareA - SpareG: Spare output, always deasserted (O)

Spare I/O pins configured as outputs. Always deasserted.

4 ELECTRICAL DESCRIPTION

4.1 Absolute maximum ratings

According to Actel data sheet RD13.

4.2 Operating conditions

	Prototype part	Flight part
Temperature	-40°C to 85°C	-55°C to +125°C
Supply voltage V_{CCA}	+2.3V to +2.7V	+2.3V to +2.7V
Supply voltage V_{CCI}	+4,5V to +5.5V	+4,5V to +5.5V

Table 9: *Operating conditions*

4.3 Input voltages

According to Actel data sheet RD13, 5 V CMOS configuration.

4.4 Input leakage currents

According to Actel data sheet RD13, 5 V CMOS configuration.

4.5 Input capacitances

According to Actel data sheet RD13, 5 V CMOS configuration.

4.6 Output voltages

According to Actel data sheet RD13, 5 V CMOS configuration.

4.7 Output leakage currents

According to Actel data sheet RD13, 5 V CMOS configuration.

4.8 Output capacitances

According to Actel data sheet RD13, 5 V CMOS configuration.

4.9 Clock Input voltages

According to Actel data sheet RD13, 5 V PCI configuration.

4.10 Clock Input leakage currents

According to Actel data sheet RD13, 5 V PCI configuration.

4.11 Clock Input capacitances

According to Actel data sheet RD13, 5 V PCI configuration.

4.12 Timing parameters

The timing parameters in table 10 are valid under the conditions specified in table 9.

		Flight part	
Name	Description	Minimum	Maximum
T_{RES}	Reset_N asserted	4 * T_{CK}	
f_{CK18}	Clk18 frequency {nominal}	18 MHz	
f_{CK18}	Clk18 frequency {absolute}	0 Hz	25 MHz
T_{CK18}	Clk18 period {absolute}	40 ns	
T_1	Clk18 high to output stable		20 ns
T_{CK45}	Clk4_5 period	T_{CK18} / 4	T_{CK18} / 4
T_2	Clk18 high to Clk4_5 stable		20 ns
T_{CK4}	PdfeX_Clk period	T_{CK18} / 4.5	T_{CK18} / 4.5
T_{31}	Clk18 high to PdfeX_Clk stable		20 ns
f_{CK}	Clk frequency {nominal}	4,5 MHz	
f_{CK}	Clk frequency {absolute}	0 Hz	10 MHz
T_{CK}	Clk period {absolute}	100 ns	
T_3	Clk high to output stable		30 ns
f_{SCK}	PdfeX_SClk frequency		f_{CK} / 16
T_{SCK}	PdfeX_SClk period	T_{CK} * 16	
T_4	PdfeX_SEn high to PdfeX_SClk high	T_{CK} * 16	
T_5	PdfeX_SClk high to PdfeX_SEn low	T_{CK} * 8	
T_6	PdfeX_SEn width de-asserted	T_{CK} * 4	
T_7	PdfeX_SEn high to PdfeX_SOut stable		5 ns
T_8	PdfeX_SClk low to PdfeX_SOut stable		5 ns
T_9	PdfeX_SIn setup	10 ns	
T_{10}	PdfeX_SIn hold	5 ns	

Table 10: *Timing parameters*

		Flight part	
Name	Description	Minimum	Maximum
T18	Clk high to AddressX valid		20 ns
T19	Clk high to CSX_N, RdX_N valid		20 ns
T20	Clk low to WrX_N valid		20 ns
T21	Clk low to DataX write data valid		20 ns
T22	Clk high to DataX write data valid		20 ns
T23	Clk low to DataX tristate		25 ns
T24	Read data DataX setup	40 ns	
T25	Read data DataX hold	5 ns	
T26	PdfeX_EDOut or PdfeX_ICoOut to PdfeX_XCoIn propagation	20 ns	
T27	Cal_Enable periodicity	TCK * 256	
T28	Cal_Enable, Cal_A_X asserted width	TCK18	
T29	Cal_M/G_Odd/Even asserted to first Cal_Enable	TCK * 256	
T30	Last Cal_Enable to Cal_M/G_Odd/Even de-asserted	0 ns	

Table 10: *Timing parameters*

Selected baud rate	Effective baud rate	Accuracy
57 600	57 692	1.6%

Table 11: *RS-232 timing at f_{CK} = 4,5 MHz*

4.13 Waveforms

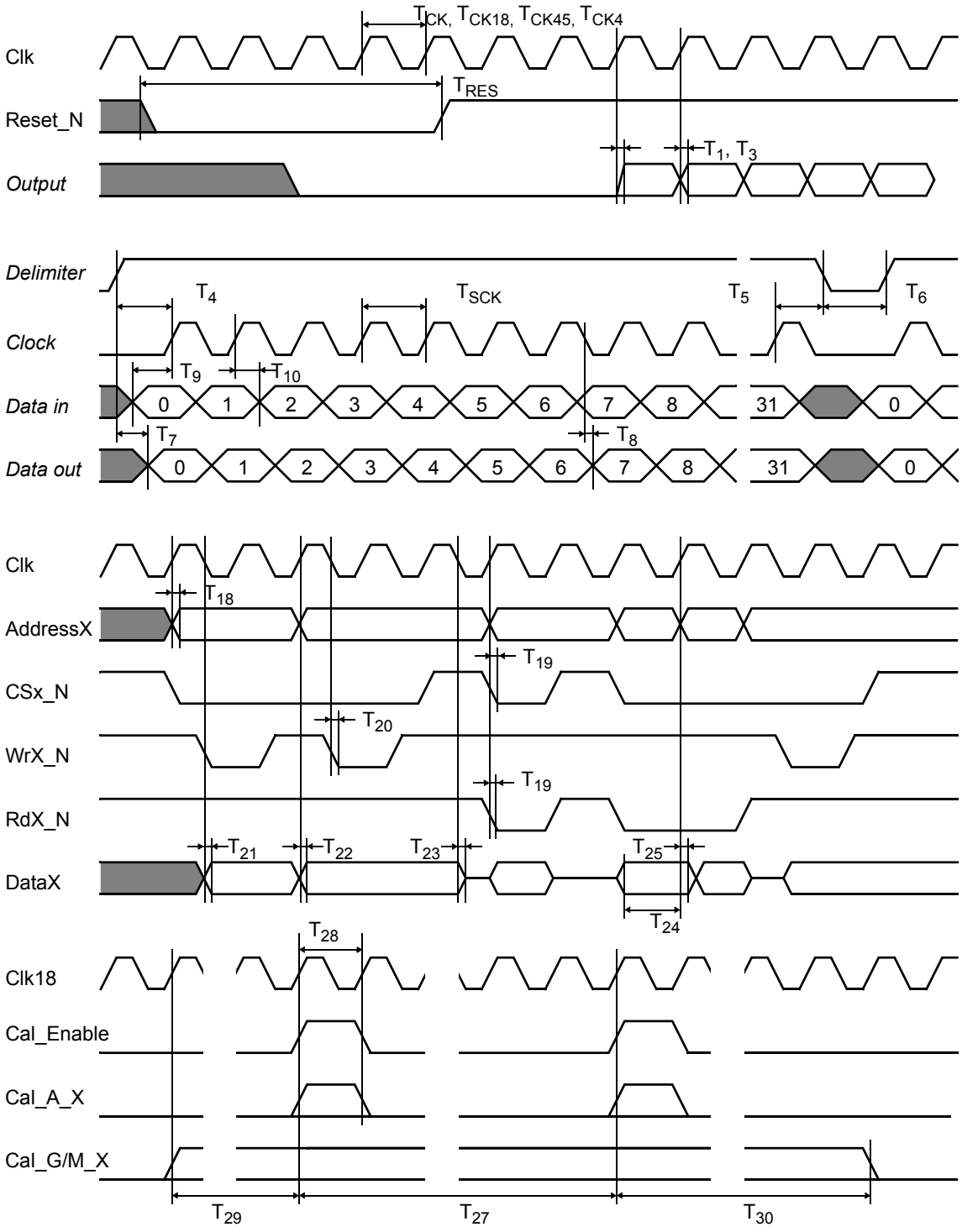

Figure 6: *Timing of various signals*

4.14 Static and dynamic power dissipation

According to Actel data sheet RD13, the power consumption can be estimated as the sum of the stand-by and active power consumption. Stand-by power is shown in table 14 for military, worst case conditions (125 °C). To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The next equation shows a piece-wise linear summation over all components.

$$\begin{aligned}\text{Power (mW)} = \; & V_{CCA}^2 * [\\ & (m_c * C_{EQCM} * f_{mc})_{CombinatorialModule} + \\ & (m_s * C_{EQSM} * f_{ms})_{SequentialModule} + \\ & (n * C_{EQI} * f_n)_{InputBuffer} + \\ & (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))R_{CLKA} + \\ & (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))R_{CLKB} + \\ & (0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1}))H_{CLK}] + \\ V_{CCI}^2 * & [(p * (C_{EQO} + C_L) * f_p)_{OutputBuffer}]\end{aligned}$$

The RT54SX32S specific parameters for the above equation are shown in table 12. The average switching frequency estimates for the SEPT FPGA device are shown in table 13. The resulting active power consumption is shown in table 14.

C_{EQCM}	3,0	C_{EQHV}	4,3
C_{EQSM}	3,0	C_{EQHF}	300
C_{EQI}	1,4	r_1	100
C_{EQO}	7,4	r_2	100
C_{EQCR}	1,9	s_1	1 080

Table 12: *RT54SX32S specific parameters*

Combinatorial Logic Modules (m_c)	2 880 [used modules]
Sequential Logic Modules (m_s)	1 080 [used modules]
Inputs Switching (n)	61
Outputs Switching (p)	31 {average}
First Routed Array Clock Loads (q_1)	13
Second Routed Array Clock Loads (q_2)	0
Load Capacitance (C_L)	35 [pF]
Average Logic Module Switching Rate (f_{mc}/f_{ms})	4,5/10 [MHz] {fCK/10}
Average Input Switching Rate (f_n)	4,5 [MHz]
Average Output Switching Rate (f_p)	4,5 [MHz]
Average First Routed Array Clock Rate (f_{q1})	18 [MHz] {fCK18}
Average Second Routed Array Clock Rate (f_{q2})	0 [MHz]
Average Dedicated Array Clock Rate (f_{s1})	4,5 [MHz] {fCK}

Table 13: *Estimated average switching frequency for the SEPT FPGA device*

Stand-by	Active	Total
68,8 mW	328,8 mW	396,6 mW

Table 14: *Power consumption for the SEPT FPGA at 2.5V / 5V supply and 125°C.*

5 MECHANICAL DESCRIPTION

5.1 Component and package specification

Flight	Actel RT54SX32S - 1, CQ208B (see RD13)	CQFP208 (see RD8)

Table 15: *Component and package specification*

See RD9 for footprint compatibility between prototype and flight parts.

5.2 Pin assignment

Pin	Type	Name	SEPT FPGA name	Connection	Remarks
1	pwr	GND		GND	
2	in	TDI		GND	JTAG {optionally pin with pull down}
3	out	I/O	Pin3	N/C	{dummy, do not use, do not connect}
4	out	I/O	Cal_Enable	Calibration	
5	in	I/O	Id0	Strap	Connect to GND or 5 V via resistor
6	out	I/O	SpareC	N/C	{spare pin}
7	out	I/O	Cal_A_0	Calibration	Least significant bit
8	out	I/O	Cal_A_1	Calibration	Most significant bit
9	out	I/O	PdfeB_SOut	PDFE 2 / 3	PDFE serial configuration data input
10	out	I/O	SpareG	N/C	{spare pin}
11	in	TMS		GND	JTAG {optionally pin with pull down}
12	pwr	VCCI		5 V	{supply for I/Os}
13	out	I/O	SpareF	N/C	{spare pin}
14	out	I/O	SpareD	N/C	{spare pin}
15	out	I/O	PdfeB_Reset_N	PDFE 2 / 3	PDFE reset
16	out	I/O	WrB_N	SRAM B	SRAM write strobe
17	in	I/O	PdfeB_ASEL_N	PDFE 2 / 3	Latchup detector
18	out	I/O	Pin18	N/C	{do not use, do not connect}
19	out	I/O	Pin19	N/C	{do not use, do not connect}
20	in	I/O	RsRequest	RS-232 I/F	RTS, inverted
21	in	I/O	Pdfe1_Err_N	PDFE 1	PDFE error signal
22	in	I/O	Pdfe0_Err_N	PDFE 0	PDFE error signal
23	out	I/O	RsClear	RS-232 I/F	CTS, inverted
24	out	I/O	PdfeB_Clk	PDFE 2 / 3	Clock
25	-	N/C	Pin25	N/C	{do not use, do not connect}
26	pwr	GND		GND	VCCA
27	pwr	VCCA		2,5 V	{supply for array}
28	pwr	GND		GND	VCCI
29	out	I/O	PdfeB_SClk	PDFE 2 / 3	PDFE serial configuration clock
30	in	TRST		GND	JTAG {directly to ground}
31	in	I/O	Pdfe3_Err_N	PDFE 3	PDFE error signal

Table 16: *Pin assignment*

Pin	Type	Name	SEPT FPGA name	Connection	Remarks
32	in	I/O	Pdfe2_Err_N	PDFE 2	PDFE error signal
33	out	I/O	SpareE	N/C	{spare pin}
34	in	I/O	PdfeA_ASEL_N	PDFE 0	Latchup detector
35	out	I/O	AdcA_Mux_1	ADC A	ADC multiplexer select, least significant
36	out	I/O	AdcB_Mux_0	ADC B	ADC multiplexer select, most significant
37	in	I/O	Pdfe0_POut_6	PDFE 0	PDFE ADC data output
38	out	I/O	AddressB_3	SRAM B	Address bit
39	in	I/O	Pdfe2_POut_0	PDFE 2	PDFE ADC data output
40	pwr	VCCI		5 V	{supply for I/Os}
41	pwr	VCCA		2,5 V	{supply for array}
42	inout	I/O	DataB_1	SRAM B	Data bit
43	inout	I/O	DataB_4	SRAM B	Data bit
44	out	I/O	RdB_N	SRAM B	Read enable
45	inout	I/O	DataB_6	SRAM B	Data bit
46	inout	I/O	DataB_7	SRAM B	Data bit, least significant
47	inout	I/O	DataB_5	SRAM B	Data bit
48	out	I/O	CSB_N	SRAM B	Chip select
49	out	I/O	AddressB_11	SRAM B	Address bit
50	inout	I/O	DataB_2	SRAM B	Data bit
51	out	I/O	RsOut_N	RS-232 I/F	Bit asynchronous data output, inverted
52	pwr	GND		GND	
53	out	I/O	AdcA_Mux_0	ADC A	ADC multiplexer select, most significant
54	out	I/O	AdcB_Mux_1	ADC B	ADC multiplexer select, least significant
55	out	I/O	AddressB_1	SRAM B	Address bit
56	out	I/O	Pdfe3_PEn_N	PDFE 3	PDFE ADC data output enable
57	inout	I/O	DataB_3	SRAM B	Data bit
58	inout	I/O	DataB_0	SRAM B	Data bit, most significant
59	out	I/O	AddressB_2	SRAM B	Address bit
60	pwr	VCCI		5 V	{supply for I/Os}
61	out	I/O	AddressB_12	SRAM B	Address bit
62	out	I/O	AddressB_0	SRAM B	Address bit, most significant
63	in	I/O	PdfeB_DSEL_N	PDFE 2 / 3	Latchup detector
64	out	I/O	AddressB_10	SRAM B	Address bit
65	-	N/C	Pin65	N/C	{do not use, do not connect}
66	in	I/O	Pdfe2_POut_5	PDFE 2	PDFE ADC data output
67	out	I/O	AddressB_4	SRAM B	Address bit
68	in	I/O	Pdfe0_POut_0	PDFE 0	PDFE ADC data output, most significant
69	out	I/O	AddressB_8	SRAM B	Address bit
70	out	I/O	AddressB_7	SRAM B	Address bit
71	out	I/O	AddressB_9	SRAM B	Address bit
72	in	I/O	Pdfe0_POut_1	PDFE 0	PDFE ADC data output
73	out	I/O	RsIrq	RS-232 I/F	Interrupt
74	out	I/O	Pin74	N/C	{do not use, do not connect}
75	in	I/O	Id2	Strap	Connect to GND or 5V via resistor
76	out	I/O	Clk4_5	Clk	Divided 4,5 MHz clock output
77	pwr	GND		GND	VCCI

Table 16: *Pin assignment*

Pin	Type	Name	SEPT FPGA name	Connection	Remarks
78	pwr	VCCA		2,5 V	{supply for array}
79	pwr	GND		GND	VCCA
80	-	N/C		N/C	
81	in	I/O	Id1	Strap	Connect to GND or 5 V via resistor
82	in	HCLK	Clk	Clk4_5	4,5 MHz system clock input
83	out	I/O	Pin83	N/C	{do not use, do not connect}
84	out	I/O	Pin84	N/C	{do not use, do not connect}
85	in	I/O	Pdfe0_POut_2	PDFE 0	PDFE ADC data output
86	in	I/O	Pdfe2_POut_7	PDFE 2	PDFE ADC data output
87	in	I/O	Pdfe2_POut_6	PDFE 2	PDFE ADC data output
88	out	I/O	AddressB_6	SRAM B	Address bit
89	in	I/O	Pdfe0_POut_5	PDFE 0	PDFE ADC data output
90	in	I/O	Pdfe2_POut_4	PDFE 2	PDFE ADC data output
91	in	I/O	Pdfe0_POut_7	PDFE 0	PDFE ADC data output
92	in	I/O	Pdfe0_POut_4	PDFE 0	PDFE ADC data output
93	in	I/O	Pdfe2_POut_3	PDFE 2	PDFE ADC data output
94	in	I/O	Pdfe2_POut_1	PDFE 2	PDFE ADC data output
95	out	I/O	AddressB_5	SRAM B	Address bit
96	out	I/O	AddressA_7	SRAM A	Address bit
97	in	I/O	Pdfe1_POut_6	PDFE 1	PDFE ADC data output
98	pwr	VCCI		5 V	{supply for I/Os}
99	in	I/O	Pdfe3_PCS_N	PDFE 3	PDFE ADC conversion ready
100	out	I/O	AddressA_9	SRAM A	Address bit
101	in	I/O	Pdfe1_POut_2	PDFE 1	PDFE ADC data output
102	in	I/O	Pdfe1_POut_1	PDFE 1	PDFE ADC data output
103	out	TDO		N/C	JTAG {optionally test pin}
104	out	I/O	AddressA_8	SRAM A	Address bit
105	pwr	GND		GND	
106	out	I/O	AddressA_5	SRAM A	Address bit
107	out	I/O	AddressA_2	SRAM A	Address bit
108	out	I/O	AddressA_4	SRAM A	Address bit
109	out	I/O	AddressA_3	SRAM A	Address bit
110	in	I/O	Pdfe1_POut_5	PDFE 1	PDFE ADC data output
111	in	I/O	Pdfe0_POut_3	PDFE 0	PDFE ADC data output
112	in	I/O	Pdfe3_POut_1	PDFE 3	PDFE ADC data output
113	in	I/O	Pdfe3_POut_7	PDFE 3	PDFE ADC data output
114	pwr	VCCA		2,5 V	{supply for array}
115	pwr	VCCI		5 V	{supply for I/Os}
116	out	I/O	Pin116	N/C	{do not use, do not connect}
117	out	I/O	Pin117	N/C	{do not use, do not connect}
118	in	I/O	Pdfe3_POut_0	PDFE 3	PDFE ADC data output
119	in	I/O	Pdfe3_POut_6	PDFE 3	PDFE ADC data output
120	in	I/O	Pdfe1_POut_0	PDFE 1	PDFE ADC data output
121	in	I/O	Pdfe1_POut_3	PDFE 1	PDFE ADC data output
122	in	I/O	Pdfe3_POut_3	PDFE 3	PDFE ADC data output
123	in	I/O	Pdfe3_POut_2	PDFE 3	PDFE ADC data output

Table 16: *Pin assignment*

Pin	Type	Name	SEPT FPGA name	Connection	Remarks
124	in	I/O	Pdfe1_POut_4	PDFE 1	PDFE ADC data output
125	in	I/O	Pdfe1_POut_7	PDFE 1	PDFE ADC data output
126	in	I/O	Pdfe3_POut_4	PDFE 3	PDFE ADC data output
127	in	I/O	Pdfe3_POut_5	PDFE 3	PDFE ADC data output
128	out	I/O	PdfeA_Clk	PDFE 0 / 1	Clock
129	pwr	GND		GND	VCCI
130	pwr	VCCA		2,5 V	{supply for array}
131	pwr	GND		GND	VCCA
132	-	N/C	Pin132	N/C	{do not use, do not connect}
133	out	I/O	AddressA_10	SRAM A	Address bit
134	out	I/O	AddressA_1	SRAM A	Address bit
135	out	I/O	AddressA_0	SRAM A	Address bit, most significant
136	out	I/O	Pdfe1_XCoIn	PDFE 1	PDFE external coincidence
137	in	I/O	Pdfe1_EDOut	PDFE 1	PDFE main event detection
138	out	I/O	Pdfe0_XCoIn	PDFE 0	PDFE external coincidence
139	out	I/O	AddressA_11	SRAM A	Address bit
140	in	I/O	Pdfe0_EDOut	PDFE 0	PDFE main event detection
141	in	I/O	Pdfe1_ICoOut	PDFE 1	PDFE internal coincidence
142	out	I/O	Pdfe3_XCoIn	PDFE 3	PDFE external coincidence
143	out	I/O	PdfeB_Pwr	PDFE 2 / 3	PDFE power enable
144	in	I/O	Pdfe3_ICoOut	PDFE 3	PDFE internal coincidence
145	pwr	VCCA		2,5 V	{supply for array}
146	pwr	GND		GND	
147	inout	I/O	DataA_5	SRAM A	Data bit
148	pwr	VCCI		5 V	{supply for I/Os}
149	inout	I/O	DataA_6	SRAM A	Data bit
150	in	I/O	Pdfe0_PCS_N	PDFE 0	PDFE ADC conversion ready
151	inout	I/O	DataA_7	SRAM A	Data bit
152	in	I/O	Pdfe2_ICoOut	PDFE 2	PDFE internal coincidence
153	inout	I/O	DataA_2	SRAM A	Data bit
154	inout	I/O	DataA_0	SRAM A	Data bit, most significant
155	inout	I/O	DataA_3	SRAM A	Data bit
156	out	I/O	WrA_N	SRAM A	SRAM write strobe
157	pwr	GND		GND	
158	in	I/O	Pdfe1_PCS_N	PDFE 1	PDFE ADC conversion ready
159	in	I/O	Pdfe2_PCS_N	PDFE 2	PDFE ADC conversion ready
160	out	I/O	AddressA_12	SRAM A	Address bit
161	in	I/O	RsIn_N	RS-232 I/F	Bit asynchronous data input, inverted
162	out	I/O	RdA_N	SRAM A	Read enable
163	inout	I/O	DataA_1	SRAM A	Data bit
164	pwr	VCCI		5 V	{supply for I/Os}
165	inout	I/O	DataA_4	SRAM A	Data bit
166	out	I/O	Pdfe2_XCoIn	PDFE 2	PDFE external coincidence
167	out	I/O	CSA_N	SRAM A	Chip select
168	in	I/O	Pdfe0_ICoOut	PDFE 0	PDFE internal coincidence
169	out	I/O	PdfeA_Pwr	PDFE 0 / 1	PDFE power enable

Table 16: *Pin assignment*

Pin	Type	Name	SEPT FPGA name	Connection	Remarks
170	out	I/O	SpareA	N/C	{spare pin}
171	in	I/O	Pdfe3_EDOut	PDFE 3	PDFE main event detection
172	out	I/O	SpareB	N/C	{spare pin}
173	out	I/O	PdfeA_AOutSel	PDFE 0 / 1	PDFE analogue output select
174	out	I/O	PdfeB_AOutSel	PDFE 2 / 3	PDFE analogue output select
175	in	I/O	Pdfe2_EDOut	PDFE 2	PDFE main event detection
176	out	I/O	PdfeA_SOut	PDFE 0 / 1	PDFE serial configuration data input
177	out	I/O	Pdfe1_SEn	PDFE 1	PDFE serial configuration enable
178	out	I/O	Pin178	N/C	{do not use, do not connect}
179	out	I/O	Pdfe0_SEn	PDFE 0	PDFE serial configuration enable
180	in	CLKA	Clk18	XTAL	18 MHz system clock input
181	in	CLKB		GND	{used internally for reset}
182	-	N/C		N/C	
183	pwr	GND		GND	VCCA
184	pwr	VCCA		2,5 V	{supply for array}
185	pwr	GND		GND	VCCI
186	out	I/O	PdfeA_SClk	PDFE 0 / 1	PDFE serial configuration clock
187	out	I/O	Pin187	N/C	{do not use, do not connect}
188	in	I/O	Reset_N	RC network	Active low power on reset
189	in	I/O	PdfeA_DSEL_N	PDFE 0 / 1	Latchup detector
190	out	I/O	Pin190	N/C	{do not use, do not connect}
191	out	I/O	Pdfe3_SEn	PDFE 3	PDFE serial configuration enable
192	in	I/O	Pdfe2_SIn	PDFE 2	PDFE serial configuration data output
193	in	I/O	Pdfe1_SIn	PDFE 1	PDFE serial configuration data output
194	out	I/O	Cal_G_Odd	Calibration	
195	out	I/O	Pdfe2_SEn	PDFE 2	PDFE serial configuration enable
196	in	I/O	Pdfe0_SIn	PDFE 0	PDFE serial configuration data output
197	out	I/O	Cal_G_Even	Calibration	
198	out	I/O	PdfeA_Reset_N	PDFE 0 / 1	PDFE reset
199	out	I/O	Pdfe2_PEn_N	PDFE 2	PDFE ADC data output enable
200	out	I/O	Cal_M_Even	Calibration	
201	pwr	VCCI		5 V	{supply for I/Os}
202	in	I/O	Pdfe3_SIn	PDFE 3	PDFE serial configuration data output
203	out	I/O	Pdfe0_PEn_N	PDFE 0	PDFE ADC data output enable
204	out	I/O	Pdfe1_PEn_N	PDFE 1	PDFE ADC data output enable
205	out	I/O	Cal_M_Odd	Calibration	
206	in	I/O	Pdfe2_POut_2	PDFE 2	PDFE ADC data output
207	out	I/O	AddressA_6	SRAM A	Address bit
208	in	TCK		GND	JTAG {optionally pin with pull down}

Table 16: *Pin assignment*